

## High Voltage PIN Diode Driver

### Ordering Information

Device	Package	
	20 Pin Ceramic DIP	28 Pin Ceramic J-Lead
HV3922	HV3922C	HV3922DJ

### Features

- ❑ Processed with HVCMOS® technology
- ❑ 5V CMOS logic – low power dissipation
- ❑ DMOS output voltage up to 220V
- ❑ Low power level shifting – 5V to 220V
- ❑ Source current 1.7mA
- ❑ Output fault detection
- ❑ Latched data output

### Absolute Maximum Ratings

Supply Voltage, $V_{CC}$	-0.5V to +7.0V
Logic Input Voltage	-0.3V to $V_{CC} + 0.3V$
Supply Voltage $V_{LL}$	-5.0V
Supply Voltage $V_{PP}$	+230V
Max Power Dissipation	0.8W
Junction Temperature	+150 °C
Storage Temperature Range	-65 °C to +150 °C
Operating Temperature Range	-55 °C to +125 °C
Lead Soldering Temperature for 10 Seconds	+300 °C

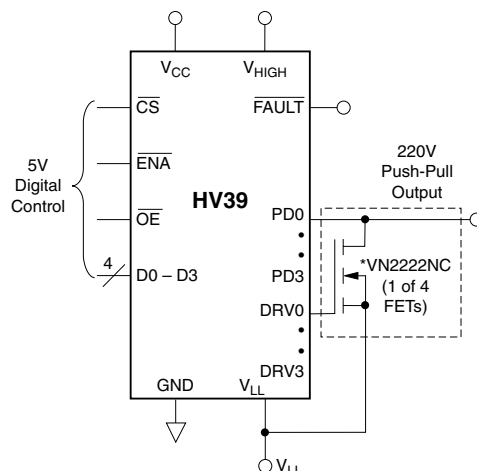
### General Description

The HV3922 is a monolithic high-voltage quad-output driver that is designed to be used in conjunction with the Supertex VN2222NC\*, a separate N-channel DMOS FET quad array, whose device characteristics are briefly described below. Together, these devices perform a 220V push-pull function that is especially suited for driving PIN diodes in applications such as frequency-hopping radios, microwave communication systems and phased array radar.

Used as a microwave or RF switch, the HV3922 has 4 high-voltage P-channel outputs: PD<sub>0</sub>, PD<sub>1</sub>, PD<sub>2</sub> and PD<sub>3</sub>. Additional controls are Chip Select ( $\overline{CS}$ ) and Output Enable ( $\overline{OE}$ ) functions. The HV3922 also has an output fault detection function that protects the outputs from damage by putting them into a high impedance state when a short is detected. The HV3922 provides 4 low-voltage outputs—DRV<sub>0</sub>, DRV<sub>1</sub>, DRV<sub>2</sub> and DRV<sub>3</sub>—that drive the gates of the 4 N-channel FETs in the VN2222NC device. See the diagram below for an example of the push-pull output structure that these two devices provide.

For detailed electrical characteristics of the VN2222NC, please see the data sheet in Chapter 8. Currently, the HV3922 is available in through-hole and surface-mount ceramic packages that are suitable for military applications, while the VN2222NC is offered in ceramic quad and discrete packages (VN2224N2 and VN2224N3). For commercial product availability, please consult the factory.

### Push-Pull Configuration



\* VN2222NC is an N-channel DMOS FET quad array recommended for use in conjunction with HV39 outputs to form four 220V push-pull outputs. Each of the four devices has a max  $R_{DS(ON)}$  of 1.25 $\Omega$ , min  $I_{D(ON)}$  of 5.0 amps, and  $BV_{DSS}$  of 220V.

## Electrical Characteristics (over recommended operating conditions unless noted)

### DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
$I_{CCQ}$	Maximum Quiescent $V_{CC}$ Supply Current		1.0	mA	$V_{CC} = 5.5V$ All outputs open
$I_{LLQ}$	Maximum Quiescent $V_{LL}$ Supply Current		4.0	mA	$V_{LL} = -3.5V$ $D_{RV(N)}$ high or low
$I_{PPQ}$	Maximum Quiescent $V_{PP}$ Supply Current		100	$\mu A$	$V_{PP} = 220V$ $P_{D(N)}$ high or low
$I_{IH}$	High-level logic current		10	$\mu A$	$H = V_{CC}$
$I_{IL}$	Low-level logic current		10	$\mu A$	$L = 0V$
$V_{FH}$	Minimum high-level logic output voltage (fault detect)	4.4		V	$V_{CC} = 4.5V$ , $I_{OH} = 20\mu A$
$V_{FL}$	Maximum low-level logic output voltage (fault detect)		0.1	V	$V_{CC} = 5.5V$ , $I_{OL} = -20\mu A$
$V_{DH}$	Minimum $P_{D(N)}$ high-level output voltage	198		V	$V_{PP} = 203V$ , $I_{OH} = 1.7mA$
$V_{DH}$	Minimum $D_{RV(N)}$ high-level output voltage	4		V	$V_{CC} = 4.5V$ , $I_{OH} = 100\mu A$
$V_{DL}$	Maximum $D_{RV(N)}$ low-output voltage		-2.3	V	$V_{LL} = -2.5V$ , $I_{DL} = -500\mu A$
$V_{TH(min)}$	Minimum fault threshold for $P_{D(N)}$ output high	$0.5 \times V_{PP}$ fault		V	$P_{D(N)} = HIGH$ , $\overline{OE} = V_{CC}$
$V_{TH(max)}$	Maximum fault threshold for $P_{D(N)}$ output high	$0.85 \times V_{PP}$ fault		V	$P_{D(N)} = HIGH$ , $\overline{OE} = V_{CC}$
$V_{TL(min)}$	Minimum fault threshold for $P_{D(N)}$ output Hi-Z	$V_{(PDN)} = 0V$		V	$P_{D(N)} = Hi-Z$ , $\overline{OE} = V_{CC}$
$V_{TL(max)}$	Maximum fault threshold for $P_{D(N)}$ output Hi-Z		$V_{(PDN)} = 25$	V	$P_{D(N)} = Hi-Z$ , $\overline{OE} = V_{CC}$

### AC Characteristics (over recommended operating conditions unless noted)

Symbol	Parameter	Min	Max	Units	Conditions
$t_{WCS}$	Minimum $\overline{CS}$ pulse to latch data	100		ns	$V_{CC} = 4.5V$ , $\overline{ENA} = 0V$
$t_{WENA}$	Minimum $\overline{ENA}$ pulse width to latch data	100		ns	$V_{CC} = 4.5V$ , $\overline{CS} = 0V$
$t_{WOE}$	$\overline{OE}$ pulse width	10	50	$\mu s$	$V_{CC} = 4.5V$ , $\overline{OE} = 0V$ , $V_{PP} = 220V$ $P_{D(N)}$ LOAD = 20K to GND
		16	50	$\mu s$	$V_{PP} = 220V$ , $P_{D(N)}$ LOAD = 20K and 3000pF to GND
TT	Input transition rise and fall times	0	200	ns	$V_{CC} = 4.5V$
$T_{SU1}$	Minimum set-up time $D_N$ and $\overline{CS}$ to $\overline{ENA}$	150		ns	$V_{CC} = 4.5V$
$T_{SU2}$	Minimum set-up time $\overline{ENA}$ to $\overline{OE}$ falling edge	150		ns	$V_{CC} = 4.5V$
TH	Minimum hold time	5		ns	$V_{CC} = 4.5V$
CIN	Maximum input capacitance		10	pF	Not tested, reference only
TO	$P_{D(N)}$ transition time from $\overline{OE}$ low to $P_{D(N)}$ high/low	1	50	$\mu s$	$V_{PP} = 220V$ $P_{D(N)}$ output loaded by 20K ohms & 3000pF to GND

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{CC}$	Logic Supply Voltage	4.5	5.5	V
$V_{IN}$	DC Logic Input Voltage	0	$V_{CC}$	V
$V_{LL}$	$V_{LL}$ Supply Voltage	-3.5	-2.5	V
$V_{PP}$	$V_{PP}$ Supply Voltage	200	220	V
$IP_{D(N)H}$	High-State Continuous $P_{D(N)}$ Source Current		1.7	mA
$T_A$	Ambient Operating Temp	-55	+125	°C
CL	$D_{RV(N)}$ Load Capacitance	0	0.006	$\mu$ F

### Notes:

- $V_{PP}$  rise time (dv/dt) should be less than 50V/ $\mu$ S.
- Power-up sequence should be the following:
  - Connect ground;
  - Apply  $V_{CC}$ ;
  - Apply  $V_{LL}$ ;
  - Apply  $V_{PP}$ ;
  - Set all inputs to a known state. Power-down sequence should be the reverse of the above.

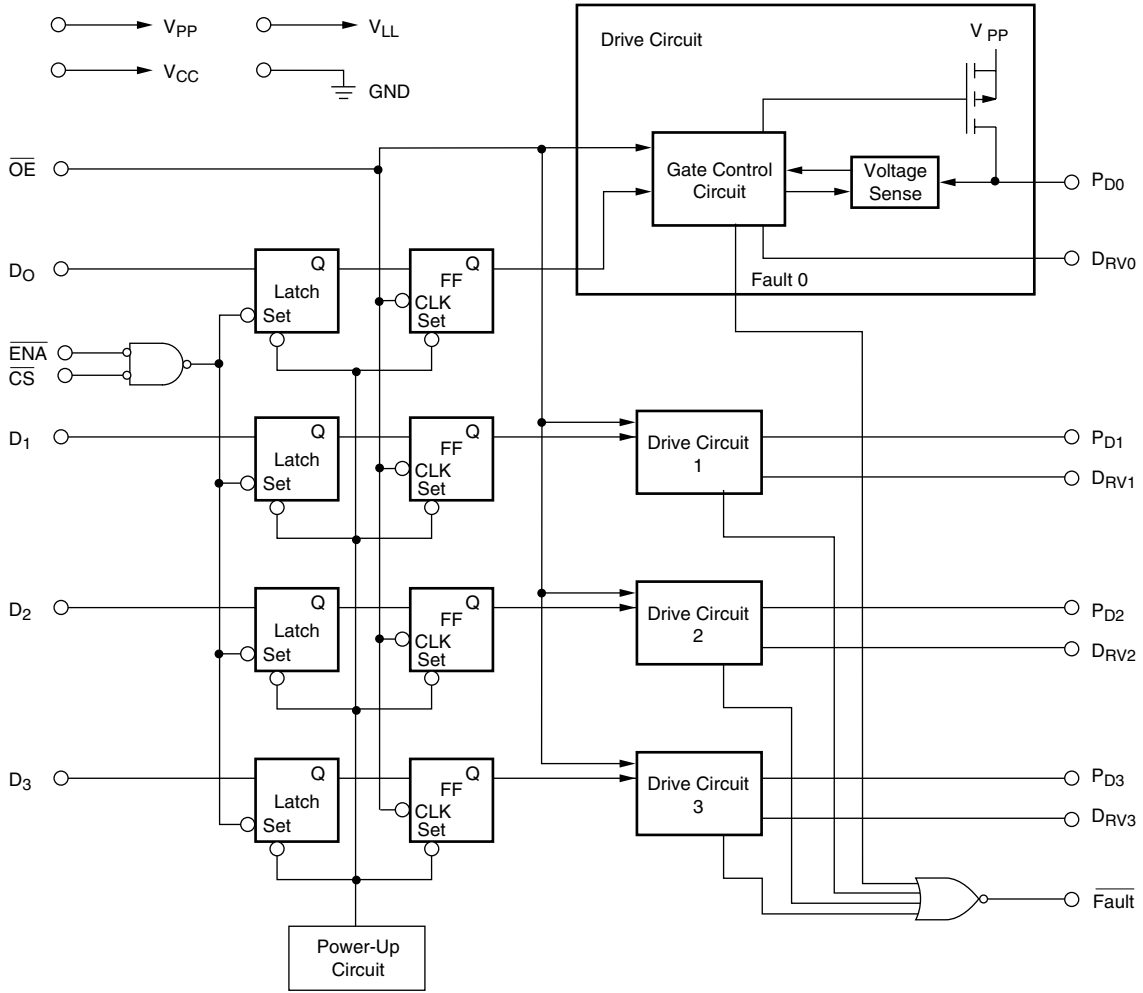
## Function Table

Input					Output			
$\overline{CS}$	$\overline{ENA}$	$\overline{OE}$	Data $D_{(N)}$	$V_{TH}$ Level <sup>2</sup>	Internal Latch Q(N)	$P_{D(N)}$	$D_{RV(N)}$	$\overline{Fault}$
H	X	H	X	Pass	Previous State	Previous State	Previous State	VFH
X	H	H	X	Pass	Previous State	Previous State	Previous State	VFH
L	L	H	H	Pass	Set	Previous State	Previous State	VFH
L	L	H	L	Pass	Reset	Previous State	Previous State	VFH
L	L	H>L	H	P/F	Set	VDH	VDL	VFH
L	L	H>L	L	P/F	Reset	HI-Z	VDH	VFH
H	X	H>L	X		Previous State			
				P/F	Set	VDH	VDL	VFH
				P/F	Reset	HI-Z	VDH	VFH
X	H	H>L	X		Previous State			
				Pass	Set	VDH	VDL	VFH
				Pass	Reset	HI-Z	VDH	VFH
X	X	H	X	Fail	—	HI-Z	VDL	VFL
(At Power Up)								
X	X	$V_{IH}$	X	P/F	Set	VDH	VDL	VFH

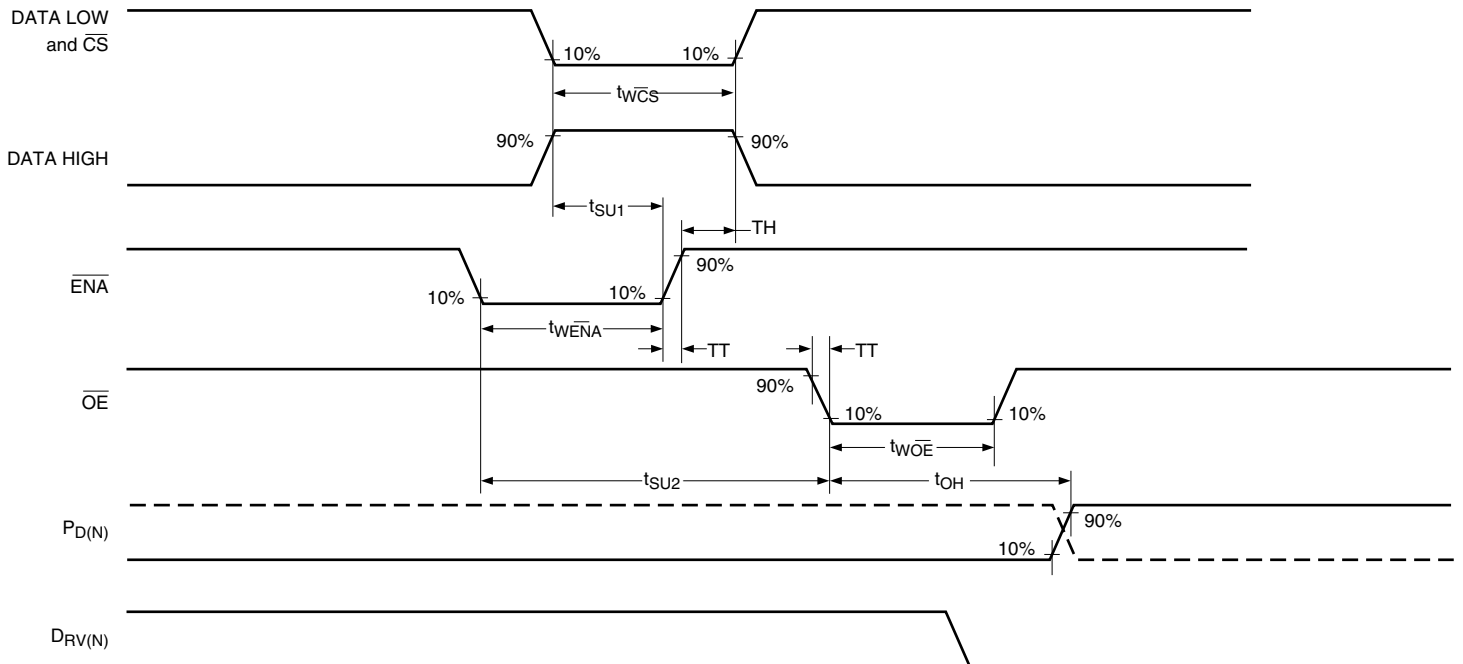
### Notes:

- X indicates "Don't Care" input state (L or H).
- The output threshold is internally tested for each  $P_{D(N)}$  output; the pass condition occurs when  $\overline{OE} = H$  and:
  - $P_{D(N)}$  driving high with output >  $V_{TH (MAX)}$ , or may occur if  $P_{D(N)}$  driving high and output >  $V_{TH (MIN)}$  and <  $V_{TL (MAX)}$ .
 OR
  - $P_{D(N)}$  driving Low with output <  $V_{TH (MIN)}$ , or may occur if  $P_{D(N)}$  driving low and output <  $V_{TH (MAX)}$  and <  $V_{TL (MIN)}$ .
 The fail condition occurs when  $\overline{OE} = H$  and conditions for "pass" are not satisfied.
- Fault output =  $V_{FL}$  indicates a fault has been detected in at least one of the  $P_{D(N)}$  output loads when  $\overline{OE} = H$ . All other outputs shall function normally when a fault condition has been detected for one of the outputs. The Fault output shall remain in the low state, regardless of the state of the output which initiated the fault status, until the next falling edge of  $\overline{OE}$ . Whenever  $\overline{OE} = L$ , the Fault output is forced to  $V_{FH}$ , and the fault latch is reset. If the fault condition persists, the fault response repeats each time the  $\overline{OE}$  input is set to H.
- H>L indicates falling edge (H to L).
- HI-Z indicates no current is sourced to output  $P_{D(N)}$ .
- P/F indicates "Pass" or "Fail" fault threshold conditions.

# Functional Block Diagram



# Timing Diagram

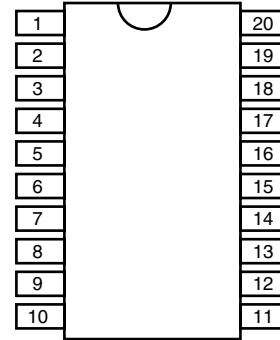


# Pin Configurations

# Package Outline

## 20 Pin, 300 Mil Wide Package

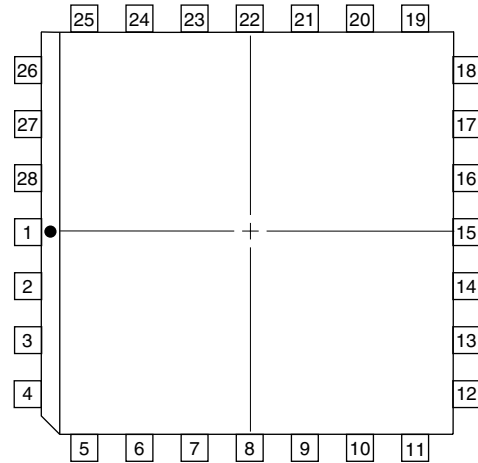
Pin	Function	Pin	Function
1	D <sub>1</sub>	11	P <sub>D0</sub>
2	D <sub>2</sub>	12	D <sub>RV1</sub>
3	D <sub>3</sub>	13	D <sub>RV0</sub>
4	V <sub>LL</sub>	14	V <sub>PP</sub>
5	GND	15	V <sub>CC</sub>
6	D <sub>RV3</sub>	16	ENA
7	D <sub>RV2</sub>	17	OE
8	P <sub>D3</sub>	18	CS
9	P <sub>D2</sub>	19	Fault
10	P <sub>D1</sub>	20	D <sub>0</sub>



20 Pin, 300 Mil Wide DIP  
**HV3922C**

## 28 Pin, J-Lead Package

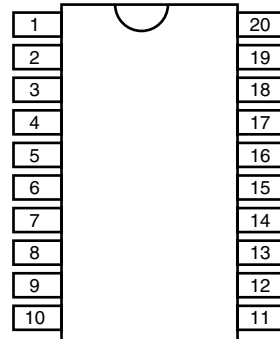
Pin	Function	Pin	Function
1	D <sub>1</sub>	15	P <sub>D1</sub>
2	D <sub>2</sub>	16	P <sub>D0</sub>
3	D <sub>3</sub>	17	N/C
4	N/C	18	D <sub>RV1</sub>
5	V <sub>LL</sub>	19	D <sub>RV0</sub>
6	GND	20	N/C
7	N/C	21	V <sub>PP</sub>
8	D <sub>RV3</sub>	22	N/C
9	D <sub>RV2</sub>	23	V <sub>CC</sub>
10	N/C	24	ENA
11	P <sub>D3</sub>	25	OE
12	N/C	26	CS
13	P <sub>D2</sub>	27	Fault
14	N/C	28	D <sub>0</sub>



28 Pin J-Lead Package  
**HV3922DJ**

## 20 Pin, 300 Mil Wide Package

Pin	Function	Pin	Function
1	S	11	S
2	S	12	S
3	S	13	N/C
4	G <sub>1</sub>	14	D <sub>4</sub>
5	G <sub>2</sub>	15	D <sub>3</sub>
6	G <sub>3</sub>	16	D <sub>2</sub>
7	G <sub>4</sub>	17	D <sub>1</sub>
8	S	18	N/C
9	S	19	S
10	S	20	S



20 Pin, 300 Mil Wide DIP  
**VN2222NC**