HARRIS Semiconductor

ICL7129

$4\frac{1}{2}$ Digit LCD, Single-Chip A/D Converter

August 1997

Features

- **±19,999 Count A/D Converter Accurate to ±4 Count**
- **10μV Resolution on 200mV Scale**
- **110dB CMRR**
- **Direct LCD Display Drive**
- **True Differential Input and Reference**
- **Low Power Consumption**
- **Decimal Point Drive Outputs**
- **Overrange and Underrange Outputs**
- **Low Battery Detection and Indication**
- **10:1 Range Change Input**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
ICL7129CPL	0 to 70	40 Ld PDIP	E40.6
ICL7129RCPL	0 to 70	40 Ld PDIP	E40.6
ICL7129CM44	0 to 70	44 Ld MQFP	Q44.10x10

NOTE: "R" indicates device with reversed leads.

Description

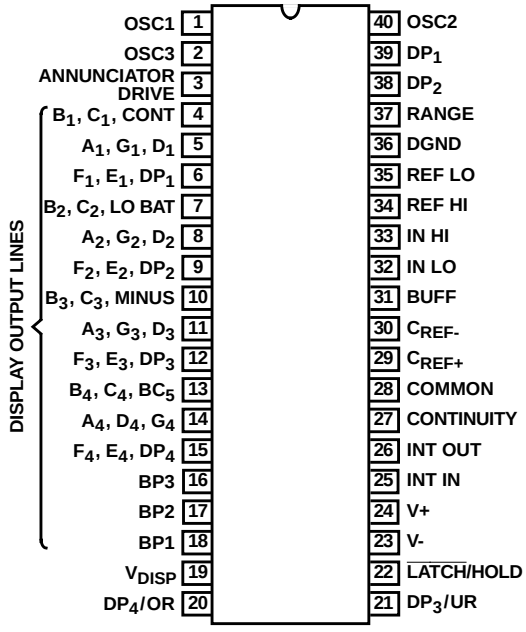
The Harris ICL7129 is a very high performance $4\frac{1}{2}$-digit, analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single chip CMOS integrated circuit requires only a few passive components and a reference to operate. It is ideal for high resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full scale and resolution down to 10μV/count.

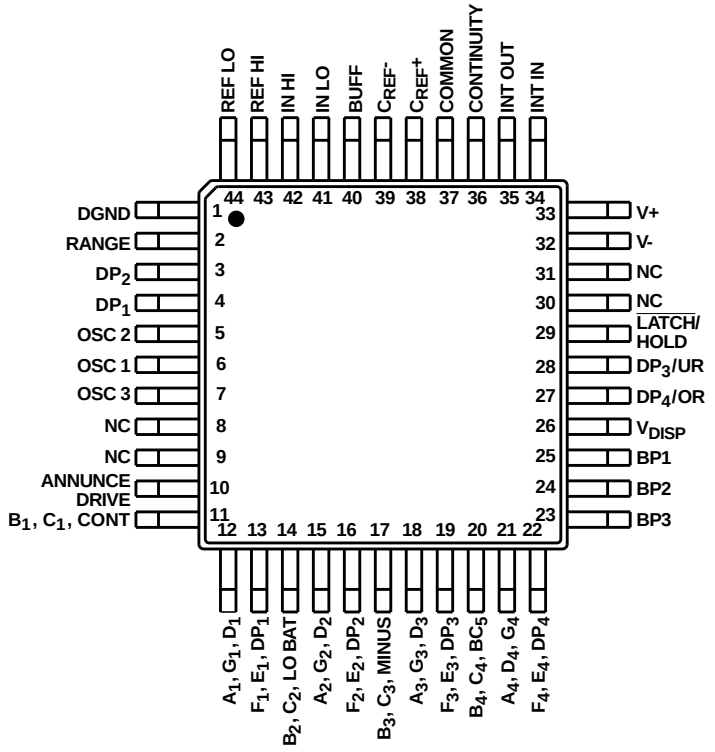
The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW/BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible transducer. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

Pinouts

ICL7129 (PDIP)
TOP VIEW



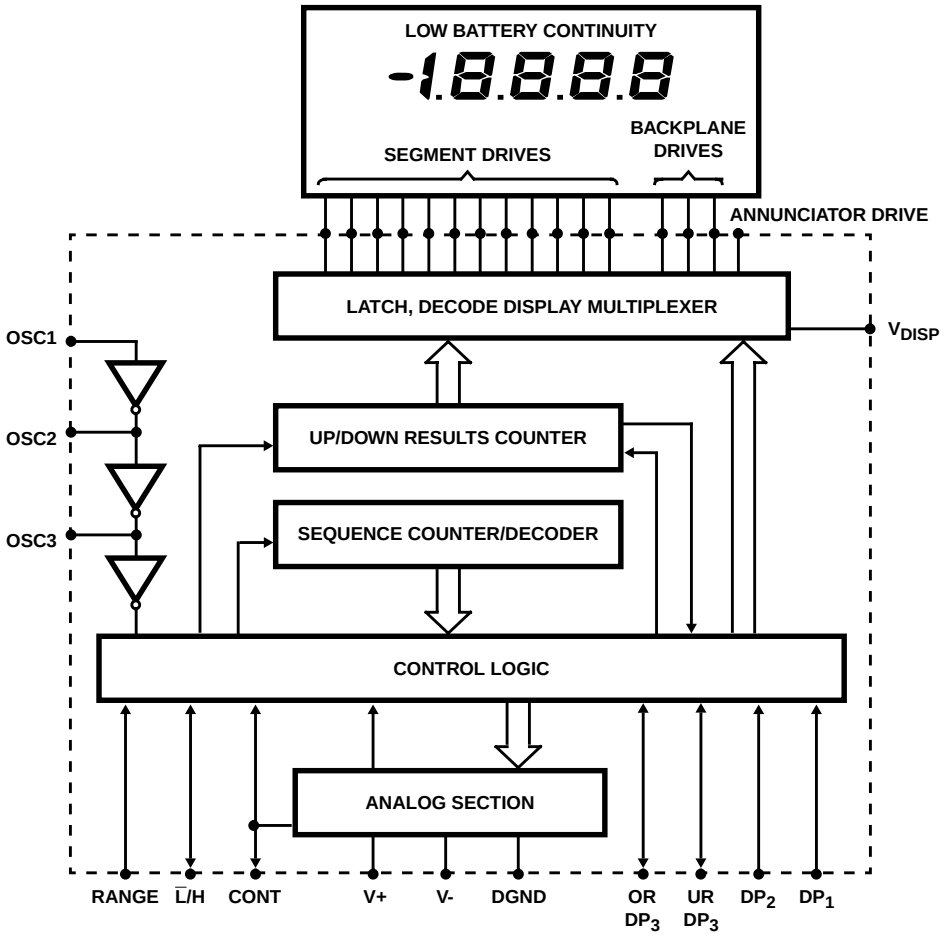
ICL7129 (MQFP)
TOP VIEW



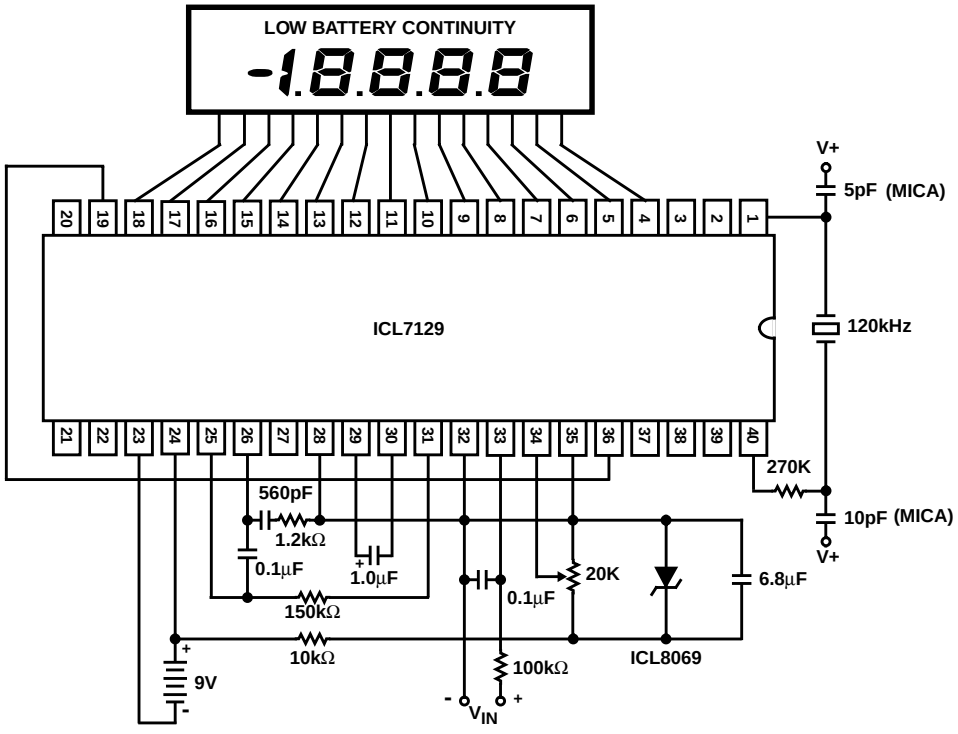
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3085.1**

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage 15V
Reference Voltage (REF HI or REF LO). . . . . V+ to V-
Input Voltage (Note 1), IN HI or IN LO . . . . . V+ to V-
V_{DISP} . . . . . .DGND -0.3V to V+
Digital Input Pins
1, 2, 19, 20, 21, 22, 27, 37, 38, 39, 40 . . . . . .DGND to V+

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{o}C/W)
PDIP Package	50
MQFP Package	80

Maximum Junction Temperature . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . .-65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input voltages may exceed the supply voltages provided that input current is limited to 1400mA. Currents above this value may result in valid display readings but will not destroy the device if limited to ±1mA.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V- to V+ = 9V, V_{REF} = 1.00V, T_A = 25^{o}C, f_{CLK} = 120kHz, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0V, 200mV Scale	-0000	0000	+0000	Counts
Zero Reading Drift	V_{IN} = 0V, 0^{o}C To 70^{o}C	-	±0.5	-	µV/^{o}C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, RANGE = 2V	9996	9999	10000	Counts
Range Change Accuracy	V_{IN} = 0.10000V on Low, Range ≈ V_{IN} = 1.0000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	-V_{IN} = +V_{IN} = 199mV	-	1.5	3.0	Counts
Linearity Error	200mV Scale	-	1.0	-	Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1V,V_{IN} = 0V, 200mV Scale	-	110	-	dB
Input Common-Mode Voltage Range	V_{IN} = 0V, 200mV Scale	-	(V-) +1.5 (V+) -1.0	-	V
Noise (Peak-To-Peak Value not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale	-	14	-	µV
Input Leakage Current	V_{IN} = 0V, Pin 32, 33	-	1	10	pA
Scale Factor Tempco	V_{IN} = 199mV 0^{o}C To 70^{o}C External V_{REF} = 0ppm/^{o}C	-	2	7	ppm/^{o}C
COMMON Voltage	V+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = + 0.1V	-	0.6	-	mA
COMMON Source Current	ΔCommon = -0.1V	-	10	-	µA
DGND Voltage	V+ to Pin 36, V+ to V- = 9V	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V	-	1.2	-	mA
Supply Voltage Range	V+ to V- (Note 3)	6	9	12	V
Supply Current Excluding COMMON Current	V+ to V- = 9V	-	1.0	1.5	mA
Clock Frequency	(Note 3)	-	120	360	kHz
V_{DISP} Resistance	V_{DISP} to V+	-	50	-	kΩ
Low Battery Flag Activation Voltage	V+ to V-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI	100	200	-	mV
	V_{OUT} Pin 27 = LO	-	200	400	mV
Pull-Down Current	Pins 37, 38, 39	-	2	10	µA
"Weak Output" Current Sink/Source	Pins 20, 21 Sink/Source	-	3/3	-	µA
	Pin 27 Sink/Source	-	3/9	-	µA
Pin 22 Source Current		-	40	-	µA
Pin 22 Sink Current		-	3	-	µA

NOTE:

3. Device functionality is guaranteed at the stated Min/Max limits. However, accuracy can degrade under these conditions.

Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	OSC_1	Input to first clock inverter.
2	OSC_3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP_3	Backplane #3 output to display.
17	BP_2	Backplane #2 output to display.
18	BP_1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{\text{LATCH}}$/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.

PIN	SYMBOL	DESCRIPTION
23	V-	Negative power supply terminal.
24	V+	Positive power supply terminal, and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V+ for DE, 10X, etc., Can be used as pre-regulator for external reference.
29	C_{REF}+	Positive side of external reference capacitor.
30	C_{REF}-	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3µA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3µA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3µA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

Detailed Description

The ICL7129 is a uniquely designed single chip A/D converter. It features a new "successive integration" technique to achieve 10µV resolution on a 200mV full-scale range. To achieve this resolution a 10:1 improvement in noise performance over previous monolithic CMOS A/D converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The ICL7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are cancelled using digital techniques instead. Savings in external parts cost are realized as well as improved noise performance and elimination of a source of electromagnetic and electrostatic pick-up.

In the overall Functional Block Diagram of the ICL7129 the heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps track of the many separate phases required for each conversion cycle. The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is de-integrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analog section block diagram shown in Figure 1 includes all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are 5 basic configurations used in the full conversion cycle. Figure 2 illustrates a typical waveform on the integrator output. INT, INT_1, and INT_2 all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

DE_1, DE_2, and DE_3 are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the de-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by 10 and DE_2 begins. Similarly DE_2's overshoot is amplified by 10 and DE_3 begins. At the end of DE_3 the results counter holds a number with $5^1/_2$ digits of resolution. This was obtained by feeding counts into the results counter at the $3^1/_2$ digit level during DE_1, into the $4^1/_2$ digit level during DE_2 and the $5^1/_2$ digit level for DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT_2 switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.02% of full scale and is sent to the display driver for decoding and multiplexing.

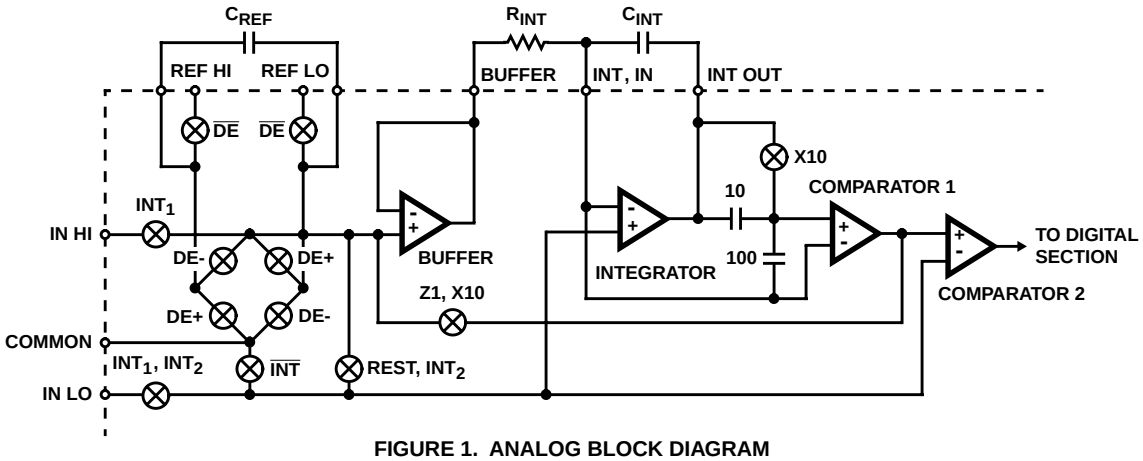


FIGURE 1. ANALOG BLOCK DIAGRAM

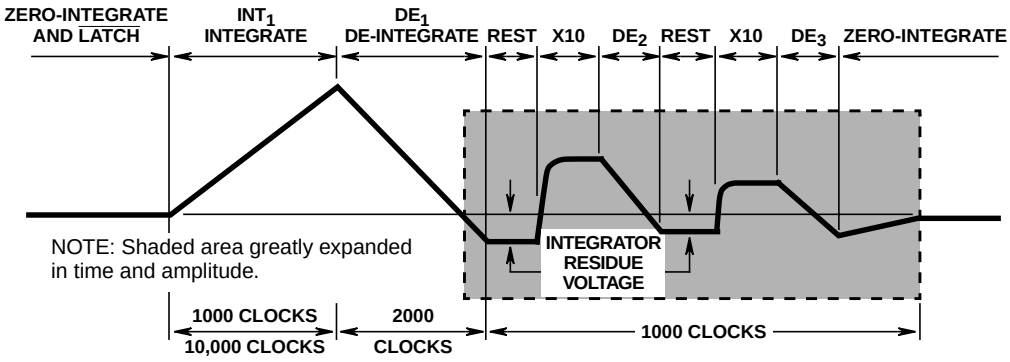


FIGURE 2. INTEGRATOR WAVEFORM FOR NEGATIVE INPUT VOLTAGE SHOWING SUCCESSIVE INTEGRATION PHASES AND RESIDUE VOLTAGE

COMMON, DGND, and "Low Battery"

The COMMON and DGND (Digital GrouND) outputs of the ICL7129 are generated from internal zener diodes (Figure 3). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V+ is the supply voltage for the logic section of the ICL7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to ensure that these outputs are not overloaded. Figure 4 shows the connection of external logic circuitry to the ICL7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 5 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12mA while DGND has no source capability.

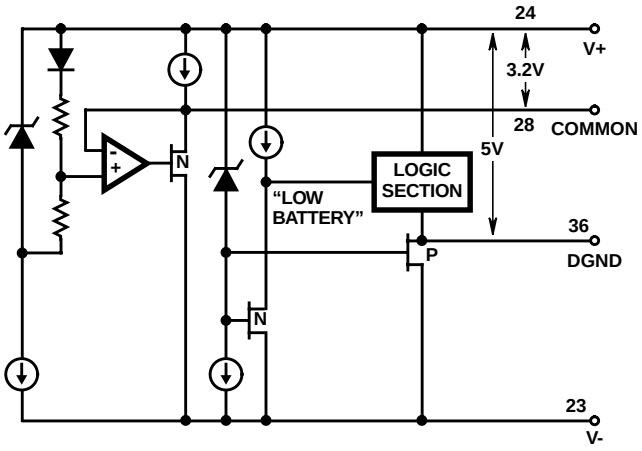


FIGURE 3. BIASING STRUCTURE FOR COMMON AND DGND

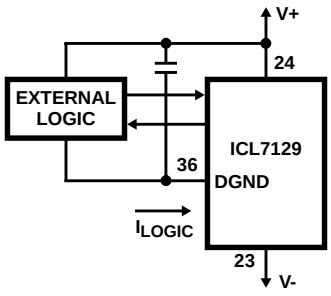


FIGURE 4. DGND SINK CURRENT

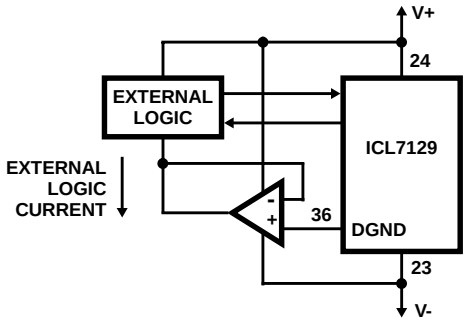


FIGURE 5. BUFFERED DGND

The "LOW BATTERY" annunciator of the display is turned on when the voltage between V+ and V- drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the N-Channel transistor connected to the V- rail in Figure 3. As the supply voltage decreases, the N-Channel transistor connected to the V-rail eventually turns off and the "LOW BATTERY" input to the logic section is pulled HIGH, turning on the "LOW BATTERY" annunciator.

I/O Ports

Four pins of the ICL7129 can be used as either inputs or outputs. The specific pin numbers and functions are described in the Pin Description table. If the output function of the pin is not desired in an application it can easily be overridden by connecting the pin to V+ (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 6. Since there is approximately 500kΩ in series with the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to 3µA, nominally, and the input switching threshold is typically DGND + 2V.

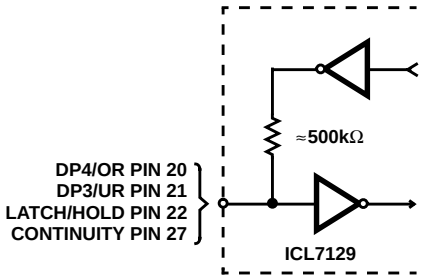


FIGURE 6. "WEAK OUTPUT"

$\overline{\text{LATCH}}$/HOLD, Overrange, and Underrange Timing

The $\overline{\text{LATCH}}$/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the ICL7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and $\overline{\text{LATCH}}$/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) and UnderRange

(UR pin 21) outputs are latched on the falling edge of $\overline{\text{LATCH}}$/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are “weak outputs” and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Description table.

Instant Continuity

A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the ICL7129 (Figure 7). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This will also turn on the “CONTINUITY” annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the ICL7129 an audible continuity checking capability.

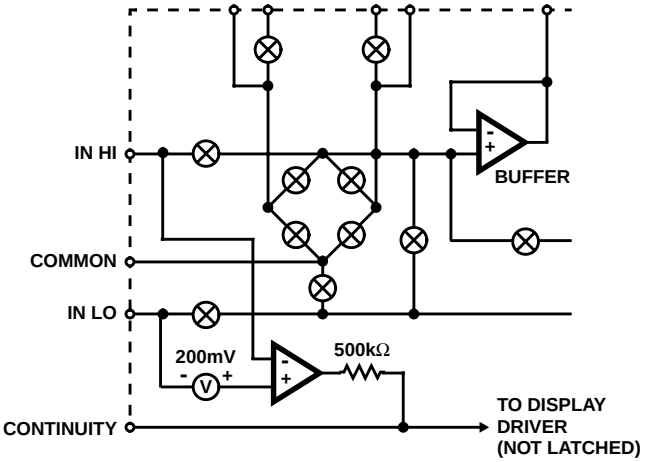


FIGURE 7. “INSTANT CONTINUITY” COMPARATOR AND OUTPUT STRUCTURE

Since the CONTINUITY output is one of the four “weak outputs” of the ICL7129, the “continuity” annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).

Display Configuration

The ICL7129 is designed to drive a triplexed liquid crystal display. This type of display has three backplanes and is driven in a multiplexed format similar to the ICM7231 display driver family. The specific display format is shown in Figure 8. Notice that the polarity sign, decimal points, “LOW BATTERY”, and “CONTINUITY” annunciators are directly driven by the ICL7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

Annunciator Drive

A special display driver output is provided on the ICL7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from V_{DISP} to V+ and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 9 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANNUNCIATOR DRIVE pin. To turn an annunciator off connect if to its backplane. An example of a display and annunciator drive scheme is shown in Figure 10.

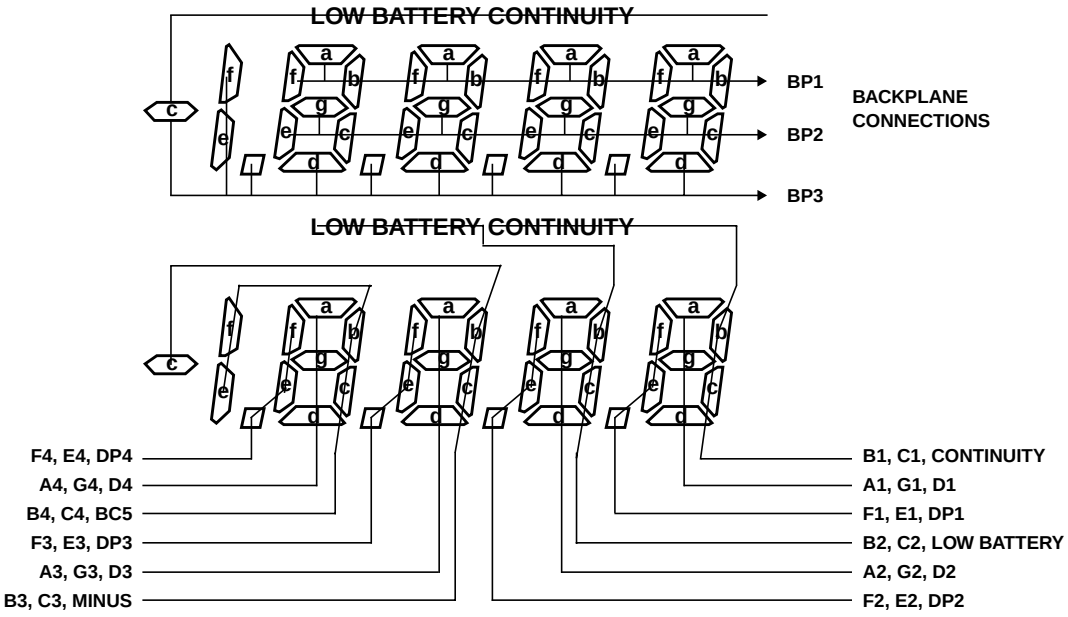


FIGURE 8. TRIPLEXED LIQUID CRYSTAL DISPLAY LAYOUT FOR ICL7129

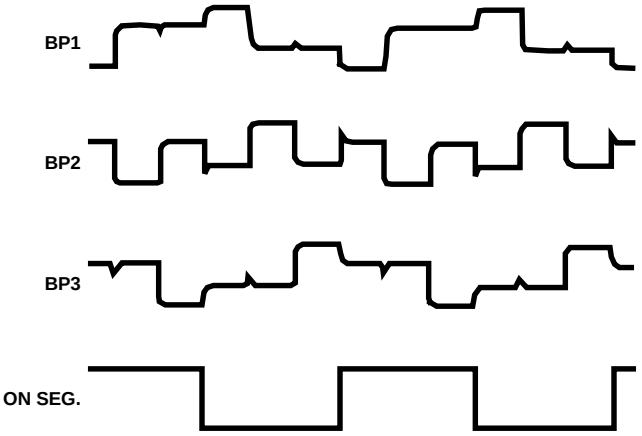


FIGURE 9. TYPICAL BACKPLANE AND ANNUNCIATOR DRIVE WAVEFORM

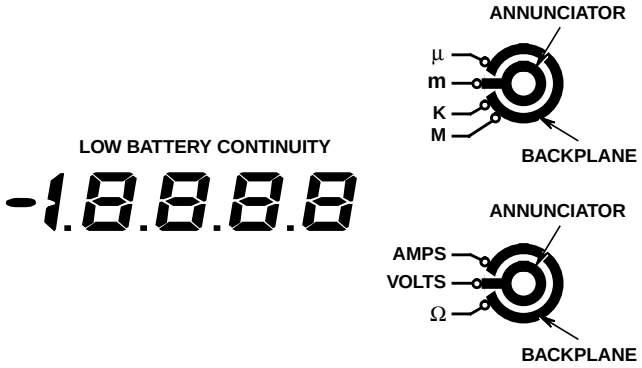


FIGURE 10. MULTIMETER EXAMPLE SHOWING USE OF ANNUNCIATOR DRIVE OUTPUT

Display Temperature Compensation

For most applications an adequate display can be obtained by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers can supply the temperature compensation requirements for their displays. Figure 11 shows two circuits that can be adjusted to give a temperature compensation of ≈ +10mV/^{o}C between V+ and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage to assure that no forward current is injected into the chip if V_{DISP} is more negative than DGND.

Component Selection

There are only three passive components around the ICL7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is no auto-zero capacitor like that found in earlier integrating A/D converter designs.

The integrating resistor is selected to be high enough to assure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of 150kΩ should be optimum for most applications. The integrator capacitor is selected to give an optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect rollover error if the swing gets too close to the positive rail (≈0.7V). This gives an optimum swing of ≈2.5V at full-scale. For a 150kΩ integrating resistor and 2 conversions per second the value is 0.1μF. For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pickup.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a 1μF value is recommended.

Clock Oscillator

The ICL7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2,000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

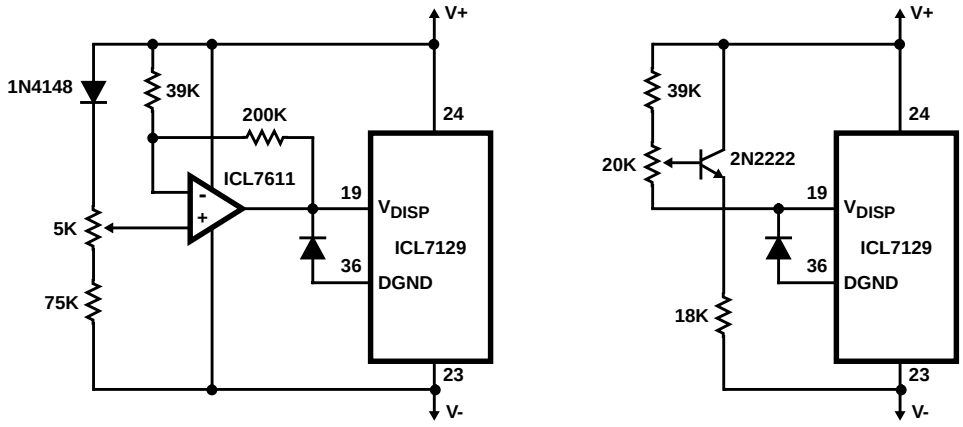


FIGURE 11. TWO METHODS FOR TEMPERATURE COMPENSATING THE LIQUID CRYSTAL DISPLAY

In low resolution applications, where the converter uses only $3^1/_2$ digits and 100µV resolution, an R-C type oscillator is adequate. In this application a C of 51pF is recommended and the resistor value selected from f_{OSC} = 0.45/RC. However, when the converter is used to its full potential ($4^1/_2$ digits and 10µV resolution) a crystal oscillator is recommended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 12.

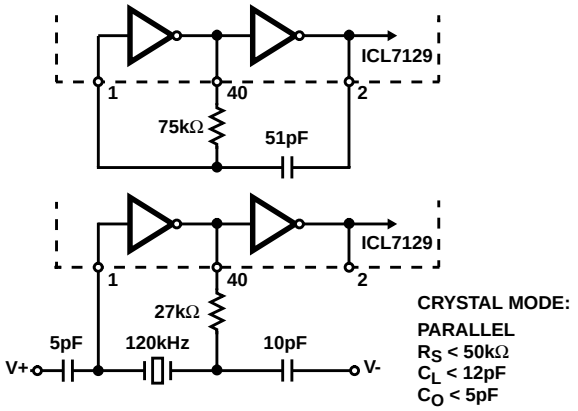


FIGURE 12. RC AND CRYSTAL OSCILLATOR CIRCUITS

Powering the ICL7129

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 13, 14, and 15 show various powering modes that may be used with the ICL7129.

The standard supply connection using a 9V battery is shown in the Typical Application Schematic.

The power connection for systems with +5V and -5V supplies available is shown in Figure 13. Notice that measurements are with respect to ground. COMMON is also tied to INLO to remove any common-mode voltage swing on the integrator amplifier inputs.

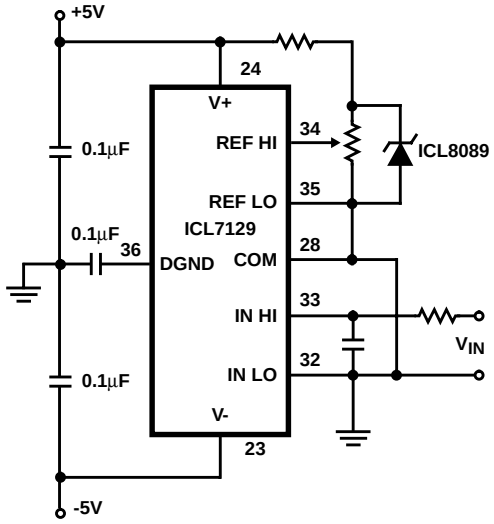


FIGURE 13. POWERING THE ICL7129 FROM +5V AND -5V

It is important to notice that in Figure 13, digital ground of the ICL7129 (DGND pin 36) is not directly connected to power supply ground. DGND is set internally to approximately 5V less than the V+ terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figure 4 and 5. In Figure 4, DGND is used as the negative supply rail for external logic provided that the supply current for the external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 5. Here, the logic supply current is shunted away from the ICL7129 keeping the load on DGND low. This treatment of the DGND output is necessary to insure compatibility when the external logic is used to interface directly with the logic inputs and outputs of the ICL7129.

When a battery voltage between 3.8V and 6V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the ICL7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 14.

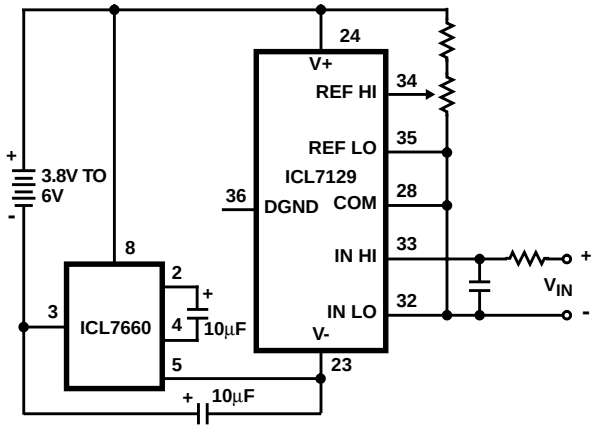


FIGURE 14. POWERING THE ICL7129 FROM A 3.8V TO 6V BATTERY

Again measurements are made with respect to COMMON since the entire system is floating. Voltage doubling is accomplished by using an ICL7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 15 where the ICL7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

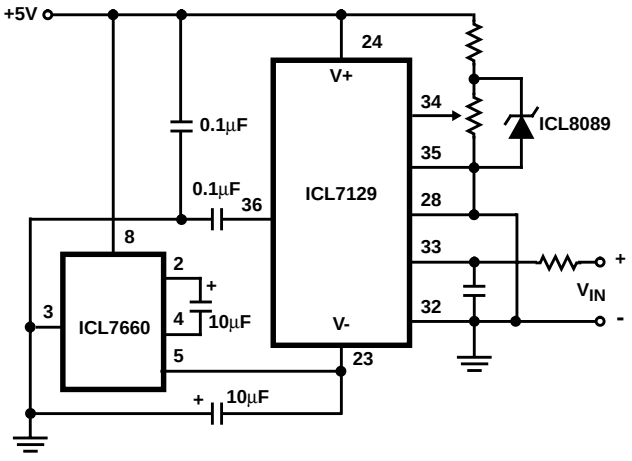


FIGURE 15. POWERING THE ICL7129 FROM A SINGLE POLARITY POWER SUPPLY

A single polarity power supply can be used to power the ICL7129 in applications where battery operation is not appropriate or convenient only if the power supply is isolated from system ground. Measurements must be made with respect to COMMON or some other voltage within its input common-mode range.

Voltage References

The COMMON output of the ICL7129 has a temperature coefficient of ±80ppm/^{o}C typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the ICL7129 is used in most environments, other voltage references should be considered. The diagram in the Typical Application Schematic and Figure 15 show the ICL8069 1.2V band-gap voltage source used as the reference for the ICL7129, and the COMMON output as its pre-regulator. The reference voltage for the ICL7129 is set to 1.000V for both 2V and 200mV full-scale operation.

Multiple Integration A/D Converter Equations

Oscillator Frequency

$f_{OSC} = 0.45/RC$
$C_{OSC} > 50pF$; $R_{OSC} > 50k\Omega$
f_{OSC} (Typ) = 120kHz
or
f_{OSC} = 120kHz Crystal (Recommended)

Oscillator Period

$t_{OSC} = 1/f_{OSC}$

Integration Clock Period

$t_{CLOCK} = 2^{*}t_{OSC}$

Integration Period

$t_{INT(2V)} = 1000^{*}t_{CLOCK}$ (Range = 1)
$t_{INT(200mV)} = 10{,}000^{*}t_{CLOCK}$ (Range = 0)

60/50Hz Rejection Criterion

t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer

Optimum Integration Current

$I_{INT} = 13\mu A$

Full Scale Analog Input Voltage

V_{INFS} (Typ) = 200mV or 2V

Integrate Resistor

$R_{INT} = V_{INFS}/I_{INT}$
R_{INT} (Typ) = 150kΩ

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

V_{INT} Maximum Swing: $(V- + 0.5V) < V_{INT} < (V+ - 0.7V)$

Display Count

$$COUNT = 10{,}000 \times \frac{V_{IN}}{V_{REF}} (Range = 1)$$
(2V Range)

$$COUNT = 10{,}000 \times \frac{V_{IN} \times 10}{V_{REF}} (Range = 0)$$
(200mV Range)

Minimum V_{REF}: 500mV

Common Mode Input Voltage

$(V- + 1V) < V_{IN} < (V+ - 0.5V)$

Auto Zero Capacitor: C_{AZ} not used

Reference Capacitor: $0.1\mu F < C_{REF} < 1\mu F$

V_{COM}

Biased Between V+ and V-.
$V_{COM} \cong V+ -2.9V$
Regulation lost when V+ to V- < ≅6.4V.
If V_{COM} is externally pulled down to (V+ to V-)/2, the V_{COM} circuit will turn off.

Power Supply: Single 9V

V+ - V- = 9V
Digital supply is generated internally
$V_{GND} \cong V+ - 4.5V$

Display: Triplexed LCD

Continuity Output On if
V_{INHI} to V_{INLO} < 200mV

Conversion Cycle (In Both Ranges)

$t_{CYC} = t_{CLOCK}$ x 30,000