SONY

ICX039BLB

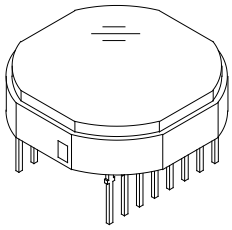
1/2-inch CCD Image Sensor for CCIR B/W Camera

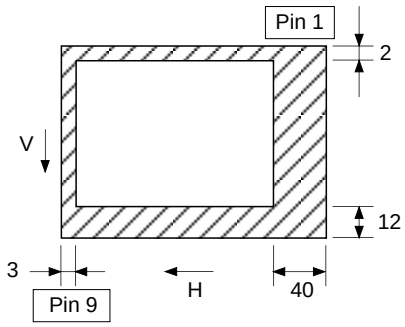
Description

The ICX039BLB is an interline transfer CCD solid-state image sensor suitable for CCIR 1/2-inch B/W video cameras. High resolution, high sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip features a field period readout system, an electronic shutter with variable charge-storage time. Also, this outline is miniaturized by using original package.

16 pin DIP (Ceramic)





Optical black position (Top View)

Features

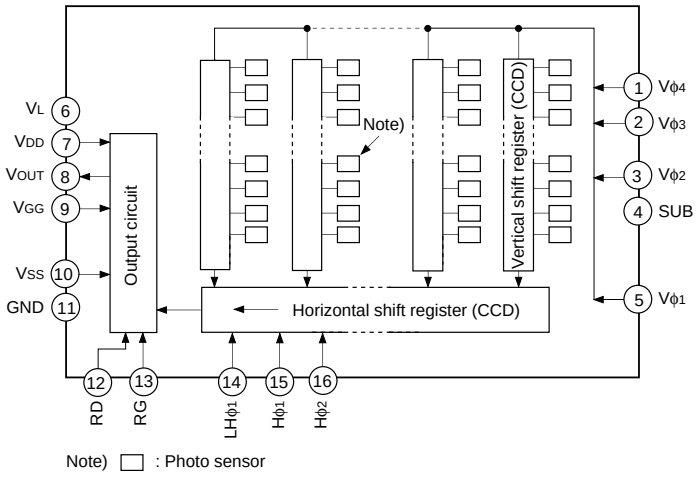
- High resolution, high sensitivity (+6dB compare with ICX039ALA) and low dark current
- Continuous variable-speed shutter
  1/50s (Typ.), 1/120s to 1/10000s
- Low smear
- High antiblooming
- Horizontal register: 5V drive
- Horizontal register final stage: 5V drive
- Reset gate: 5V drive

Device Structure

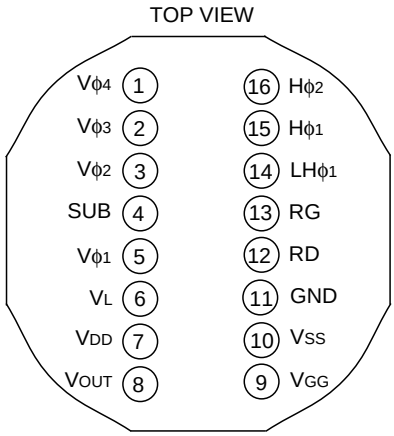
- Optical size: 1/2-inch format
- Number of effective pixels: 752 (H) × 582 (V) approx. 440K pixels
- Total number of pixels: 795 (H) × 596 (V) approx. 470K pixels
- Interline transfer CCD image sensor
- Chip size: 7.95mm (H) × 6.45mm (V)
- Unit cell size: 8.6µm (H) × 8.3µm (V)
- Optical black: Horizontal (H) direction: Front 3 pixels, Rear 40 pixels
  Vertical (V) direction: Front 12 pixels, Rear 2 pixels
- Number of dummy bits: Horizontal 22
  Vertical 1 (even field only)
- Substrate material: Silicon

E92112C6Y-PS

Block Diagram and Pin Configuration



Note) □ : Photo sensor



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ4	Vertical register transfer clock	9	VGG	Output amplifier gate bias
2	Vφ3	Vertical register transfer clock	10	VSS	Output amplifier source
3	Vφ2	Vertical register transfer clock	11	GND	GND
4	SUB	Substrate (Overflow drain)	12	RD	Reset drain bias
5	Vφ1	Vertical register transfer clock	13	RG	Reset gate clock
6	VL	Protective transistor bias	14	LHφ1	Horizontal register final stage transfer clock
7	VDD	Output amplifier drain supply	15	Hφ1	Horizontal register transfer clock
8	VOUT	Signal output	16	Hφ2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB – GND		–0.3 to +55	V	
Supply voltage	VDD, VRD, VOUT, VSS – GND	–0.3 to +18	V	
	VDD, VRD, VOUT, VSS – SUB	–55 to +10	V	
Clock input voltage	Vφ1, Vφ2, Vφ3, Vφ4 – GND	–15 to +20	V	
	Vφ1, Vφ2, Vφ3, Vφ4 – SUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*1
Voltage difference between horizontal clock input pins		to +17	V	
Hφ1, Hφ2 – Vφ4		–17 to +17	V	
LHφ1, RG, VGG – GND		–10 to +15	V	
LHφ1, RG, VGG – SUB		–55 to +10	V	
VL – SUB		–65 to +0.3	V	
Beside GND, SUB – VL		–0.3 to +30	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*1 +27V (Max.) when clock width < 10µs, duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Reset drain voltage	V_{RD}	14.55	15.0	15.45	V	$V_{RD} = V_{DD}$
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	V_{SS}	Ground through 390Ω resistor				±5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*2
Fluctuation range after substrate voltage adjustment	ΔV_{SUB}	–3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*2, *6
Fluctuation range after reset gate clock voltage adjustment	ΔV_{RGL}	–3		+3	%	
Protective transistor bias	V_L	*3				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		5		mA	
Input current	I_{IN1}			1	μA	*4
Input current	I_{IN2}			10	μA	*5

*2 Substrate voltage (V_{SUB}) · reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ±3%.

V_{SUB} code address – 1 digit display
V_{RGL} code address – 1 digit display

□ □
↑ ↑
V_{RGL} address code V_{SUB} address code

Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL} = 3.0V
V_{SUB} = 12.0V

*3 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

*4 (1) Current to each pins when 18V is applied to V_{DD}, V_{OUT}, V_{SS} and SUB pins, while pins that are not tested are grounded.
(2) Current to each pins when 20V is applied sequentially to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$ pins, while pins that are not tested are grounded. However, 20V is applied to SUB pin.
(3) Current to each pins when 15V is applied sequentially to RG, $LH\phi_1$ and V_{GG} pins, while pins that are not tested are grounded. However, 15V is applied to SUB pin.
(4) Current to V_L pin when it is grounded, while 30V is applied to all pins except pins that are not tested. However, GND and SUB pins are kept open.

*5 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

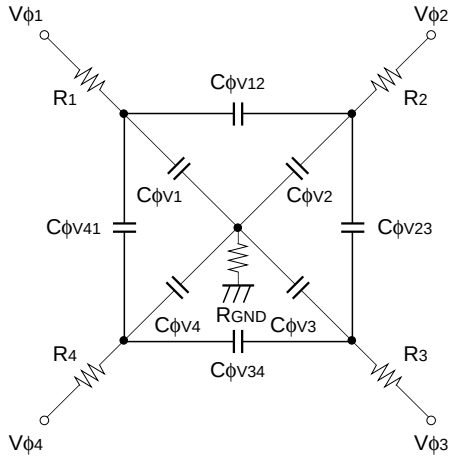
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–9.6	–9.0	–8.5	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V\phi_V$	8.3	9.0	9.65	V	2	$V\phi_V = V_{VH}n – V_{VL}n$ (n = 1 to 4)
	$\lvert V_{VH1} – V_{VH2} \rvert$			0.1	V	2	
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Horizontal final stage transfer clock voltage	$V\phi_{LH}$	4.75	5.0	5.25	V	4	
	V_{LHL}	–0.05	0	0.05	V	4	
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	5	*6
	$V_{RGLH} – V_{RGLL}$			0.8	V	5	Low level coupling
Substrate clock voltage	$V\phi_{SUB}$	23.0	24.0	25.0	V	6	

*6 No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

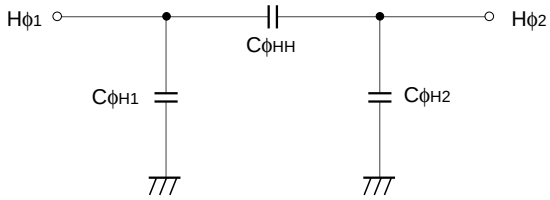
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	–0.2	0	0.2	V	5	
	$V\phi_{RG}$	8.5	9.0	9.5	V	5	

Clock Equivalent Circuit Constant

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1800		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		2200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		450		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		270		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		62		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		47		pF	
Capacitance between horizontal final stage transfer clock and GND	$C_{\phi LH}$		8		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		68		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	



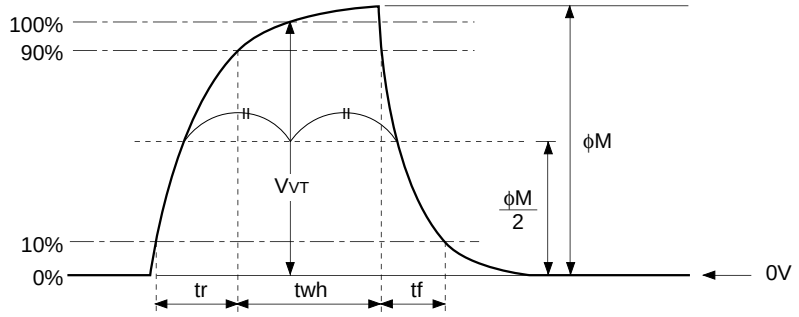
Vertical transfer clock equivalent circuit



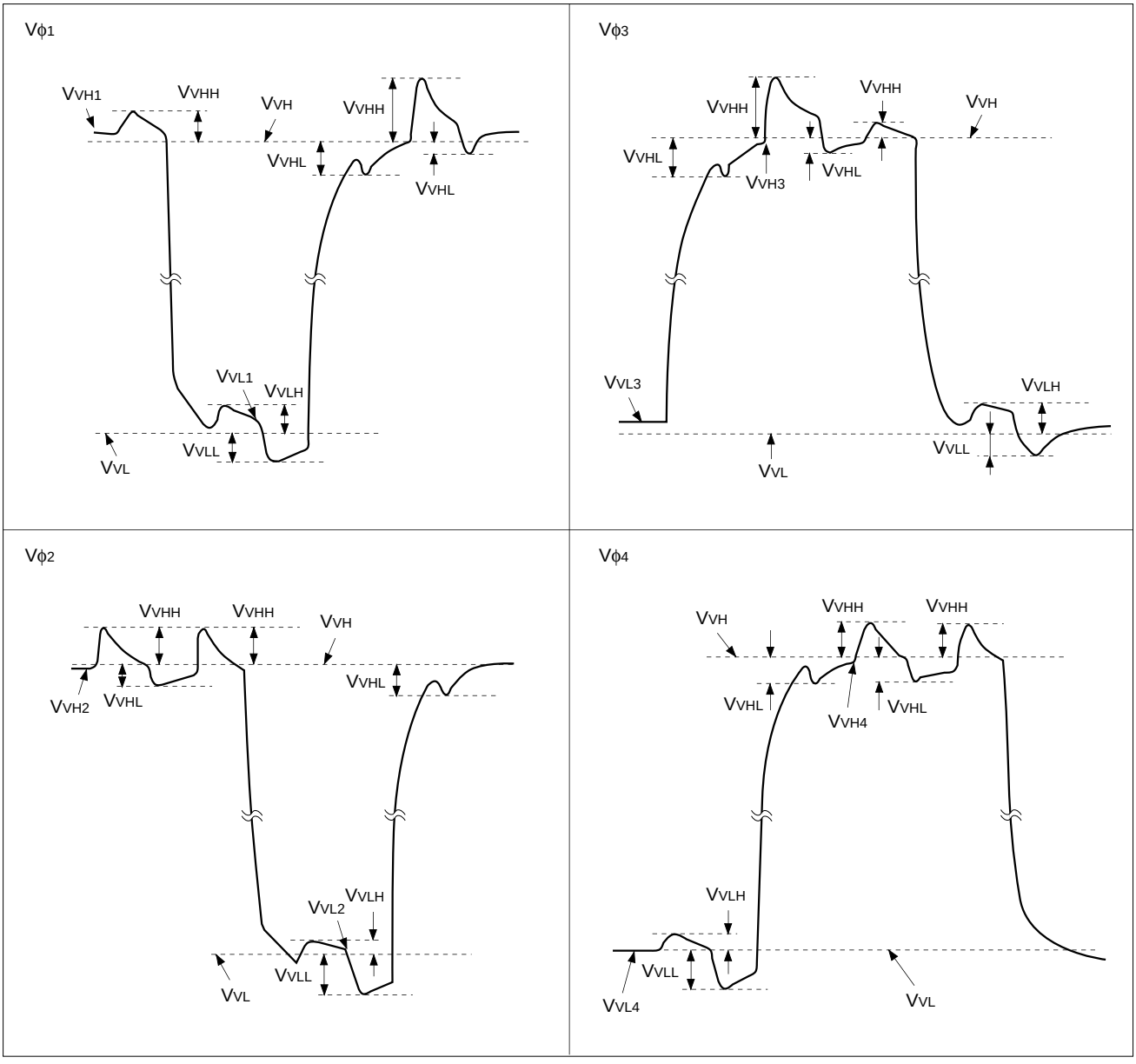
Horizontal transfer clock equivalent circuit

Drive Clock Waveform Conditions

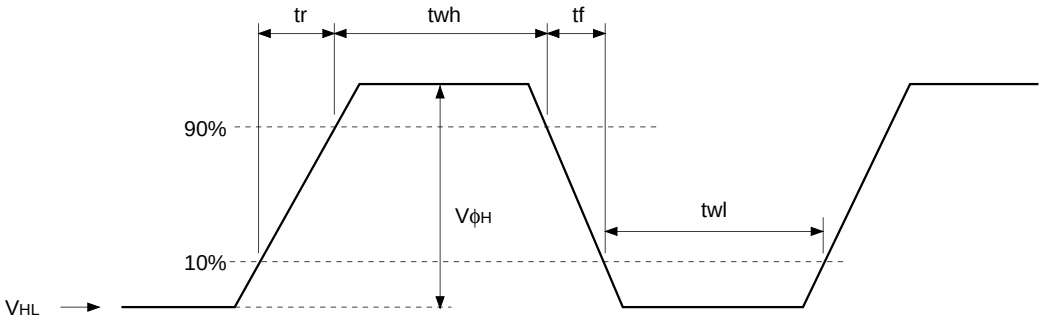
(1) Readout clock waveform



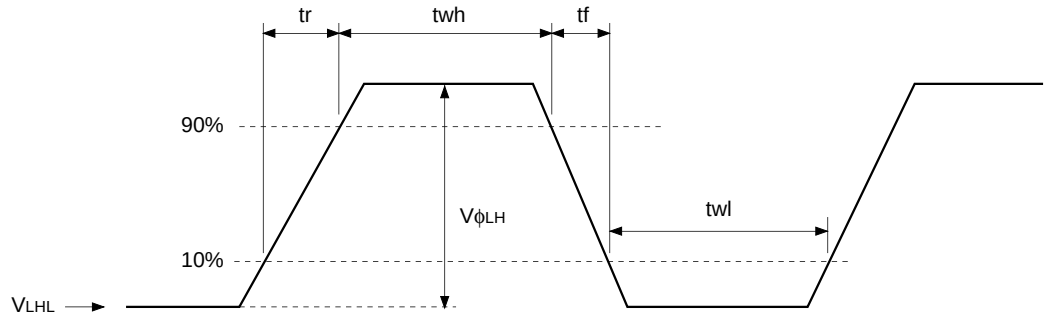
(2) Vertical transfer clock waveform



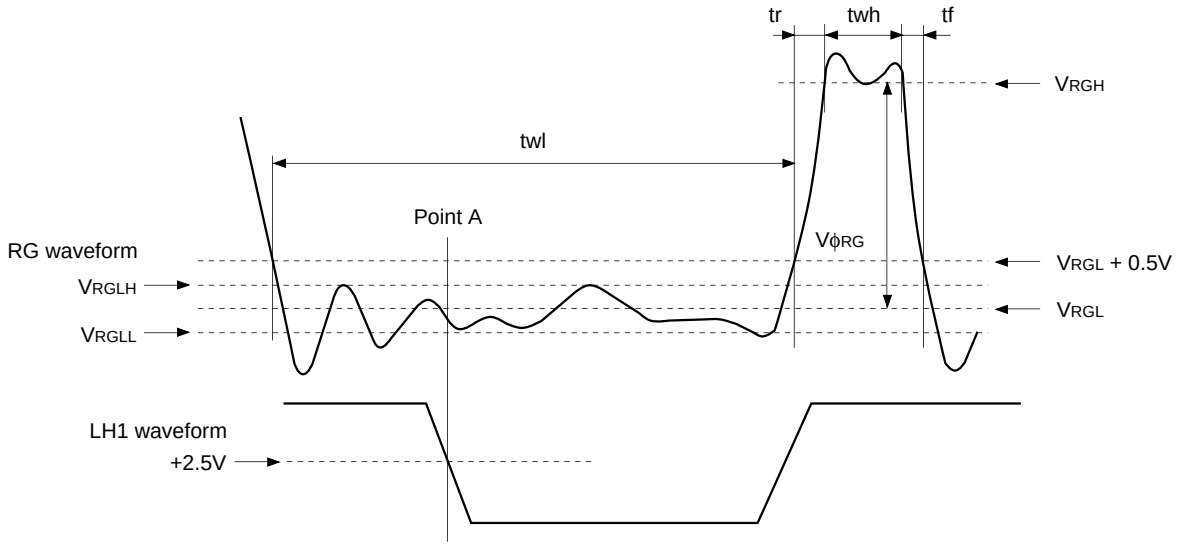
(3) Horizontal transfer clock waveform



(4) Horizontal final stage transfer clock waveform



(5) Reset gate clock waveform



V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.

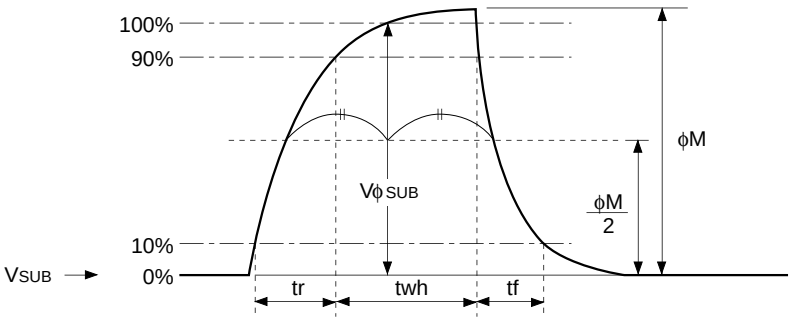
V_{RGL} is the mean value for V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

V_{RGH} is the minimum value for twh period.

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

(6) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.3	2.5						0.5			0.5		µs	During readout
Vertical transfer clock	Vϕ1, Vϕ2, Vϕ3, Vϕ4										0.015		0.25	µs	*7
Horizontal transfer clock	Hϕ		20			20			15	19	*8	15	19	ns	During imaging
Horizontal final stage clock	LHϕ		20			20			15	19	*8	15	19	ns	During imaging
Horizontal transfer/horizontal final stage clock	Hϕ1, LHϕ		5.38						0.01			0.01		µs	During parallel serial conversion
Horizontal transfer clock	Hϕ2					5.38			0.01			0.01		µs	
Reset gate clock	ϕRG	11	13			51			3			3		ns	
Substrate clock	ϕSUB	1.5	1.8							0.5			0.5	µs	During charge drain

*7 When vertical transfer clock driver CXD1250 is in use.

*8 tf ≥ tr – 2ns

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	Hϕ	16	20		ns	*9
Horizontal transfer/ horizontal final stage clock	Hϕ2, LHϕ	16	20		ns	*10

*9 "two" is the overlap period of horizontal transfer clocks Hϕ1 and Hϕ2's twh and twl.

*10 "two" is the overlap period of horizontal transfer clock Hϕ2 and horizontal final stage transfer clock LHϕ's twh and twl.

Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	280	360		mV	1	
Saturation signal	Vsat	540			mV	2	Ta = 60°C
Smear	Sm		0.009	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			2	mV	5	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	6	Ta = 60°C
Flicker	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Definition of Video Signal Shading

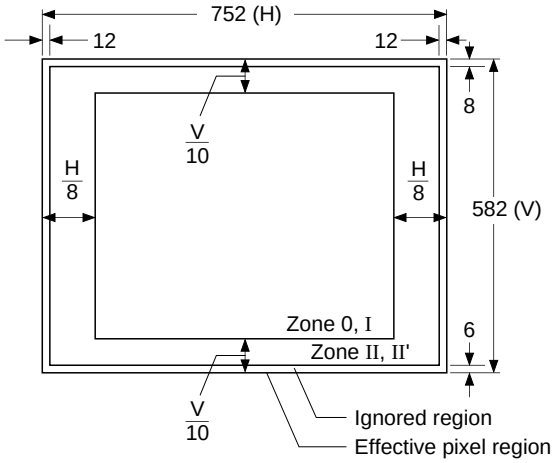


Image Sensor Characteristics Measurement Method

◎ **Measurement conditions**

1) Through the following measurements the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

2) Through the following measurements defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference, the values obtained at point [*A] in the figure of the Drive Circuit are utilized.

◎ **Definition of standard imaging conditions**

1) Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706cd/m^2, color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as IR cut filter and image at F8. At this time, light intensity to sensor receiving surface is defined as standard sensitivity testing light intensity. Signal output average value in this condition is called V_A.

2) Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (Vs) at the center of the screen and substitute in the following formula.

   $$S = Vs \times \frac{250}{50} \text{ [mV]}$$

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value V_A = 200mV, then measure the signal output munimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value V_A = 200mV. Stop readout clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, measure the maximum value VSm of signal output.

   $$Sm = \frac{VSm}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [\%] (1/10V method conversion value)}$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to signal output average value V_A = 200mV with lens diaphragm at F5.6 to F8. Then measure the maximum (Vmax) and minimum (Vmin) values of signal output.

   $$SH = (Vmax - Vmin)/200 \times 100 \text{ [\%]}$$

5. Dark signal
   Measure the signal output average value Vdt when the device ambient temperature is at 60°C and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
   Following 5, measure the maximum (Vdmax) and minimum (Vdmin) values of dark signal output.

   $$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

7. Flicker

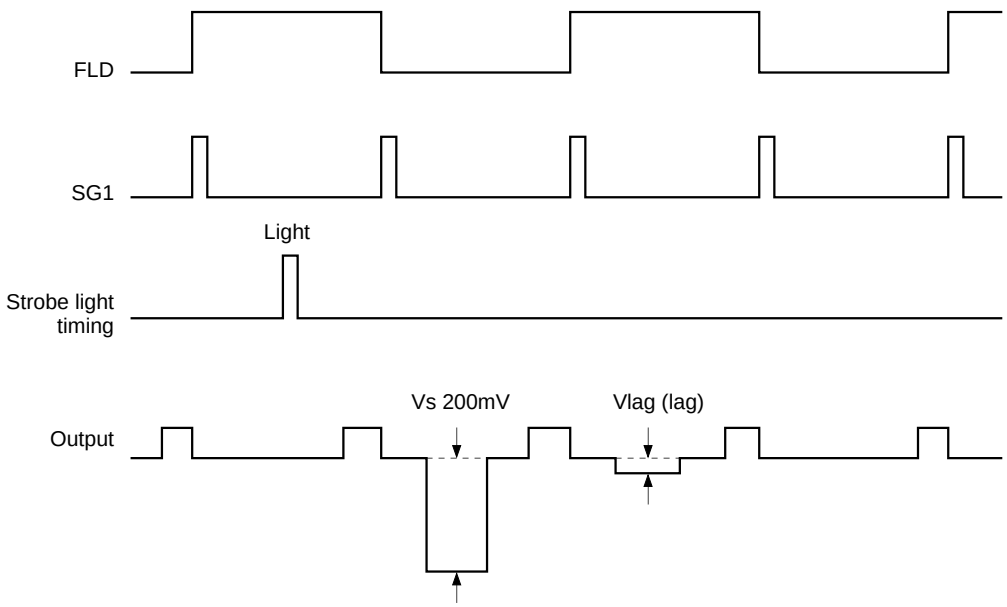
   Set to standard imaging condition II. Adjust light intensity to signal output average value V_A = 200mV. Then measure the signal output difference (ΔVf) between even field and odd field.

   $F = (\Delta Vf/200) \times 100$ [%]

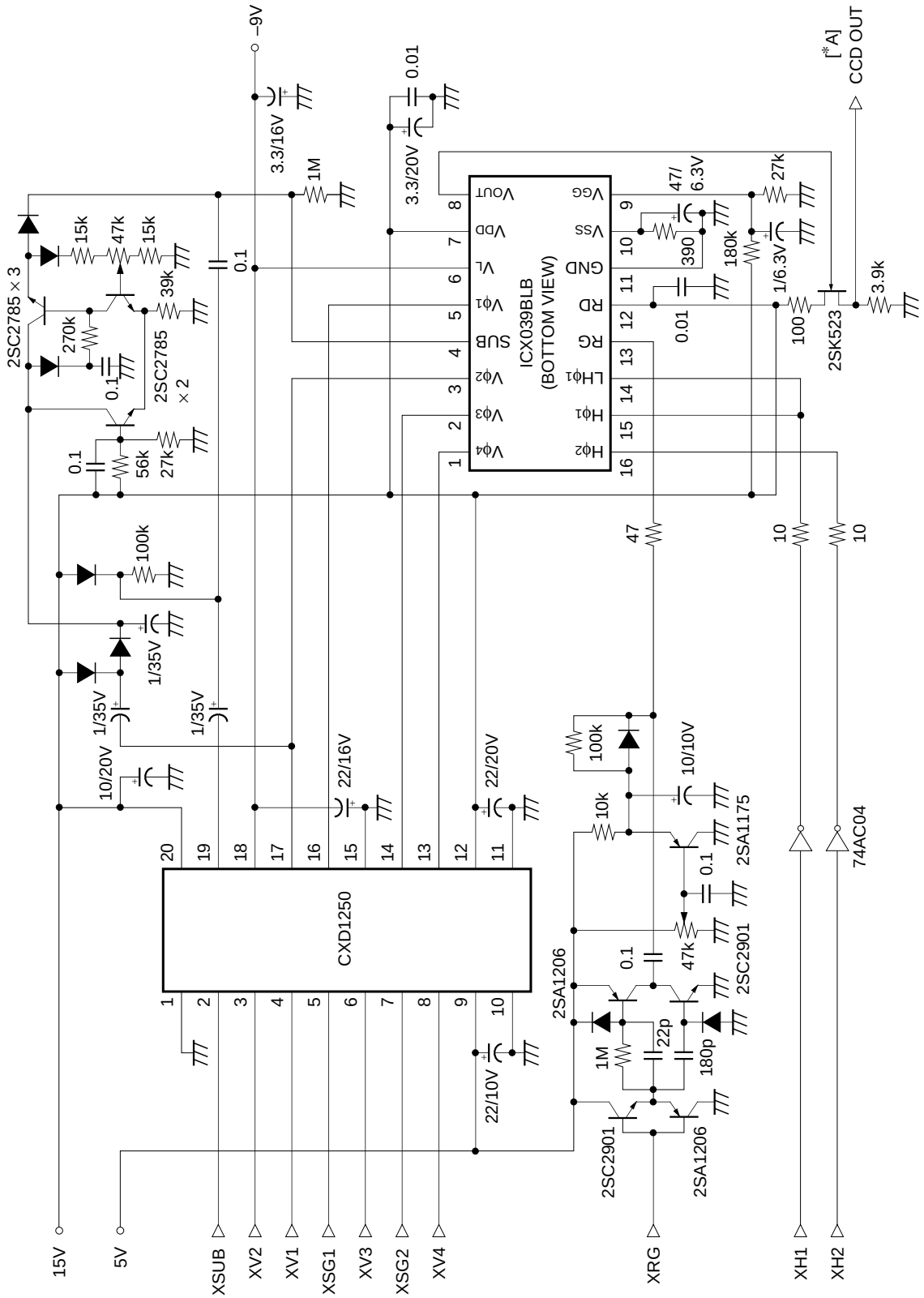
8. Lag

   Adjust signal output value (Vs) by strobe light to 200mV. Then light a stroboscopic tube with the following timing and measure the residual image (Vlag).

   $Lag = (Vlag/Vs) \times 100$ [%]

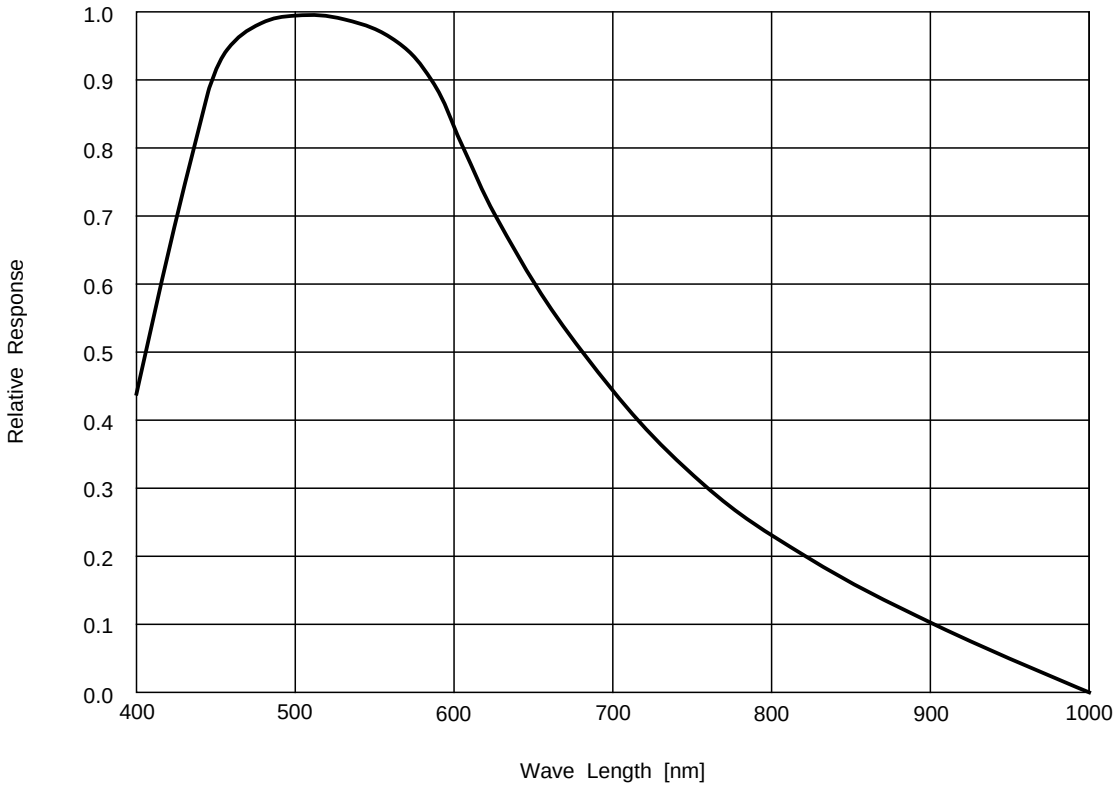


Drive Circuit

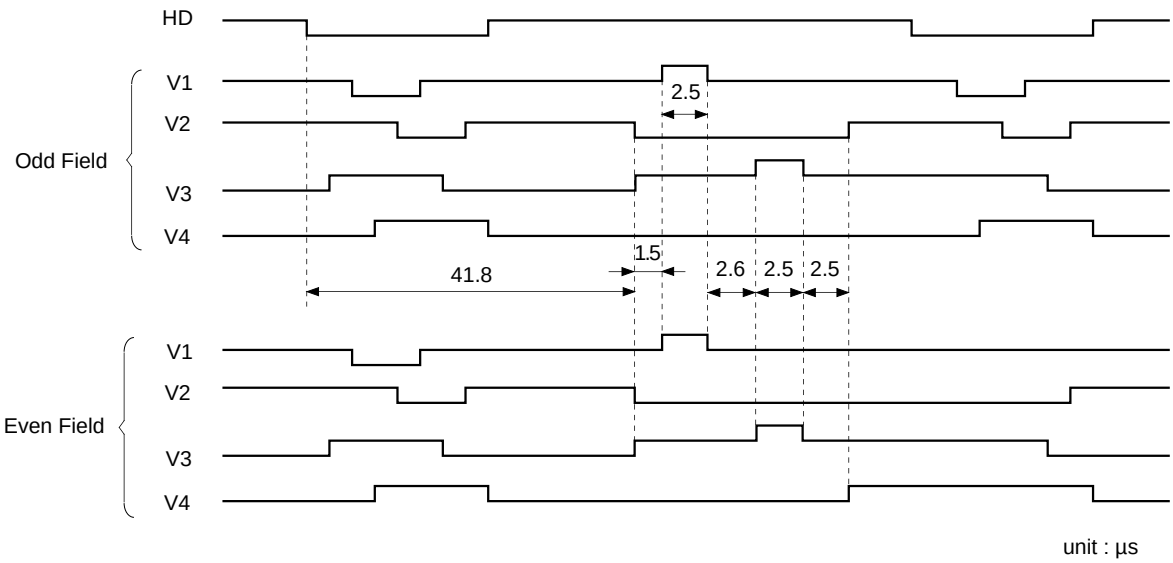


Spectral Sensitivity Characteristics

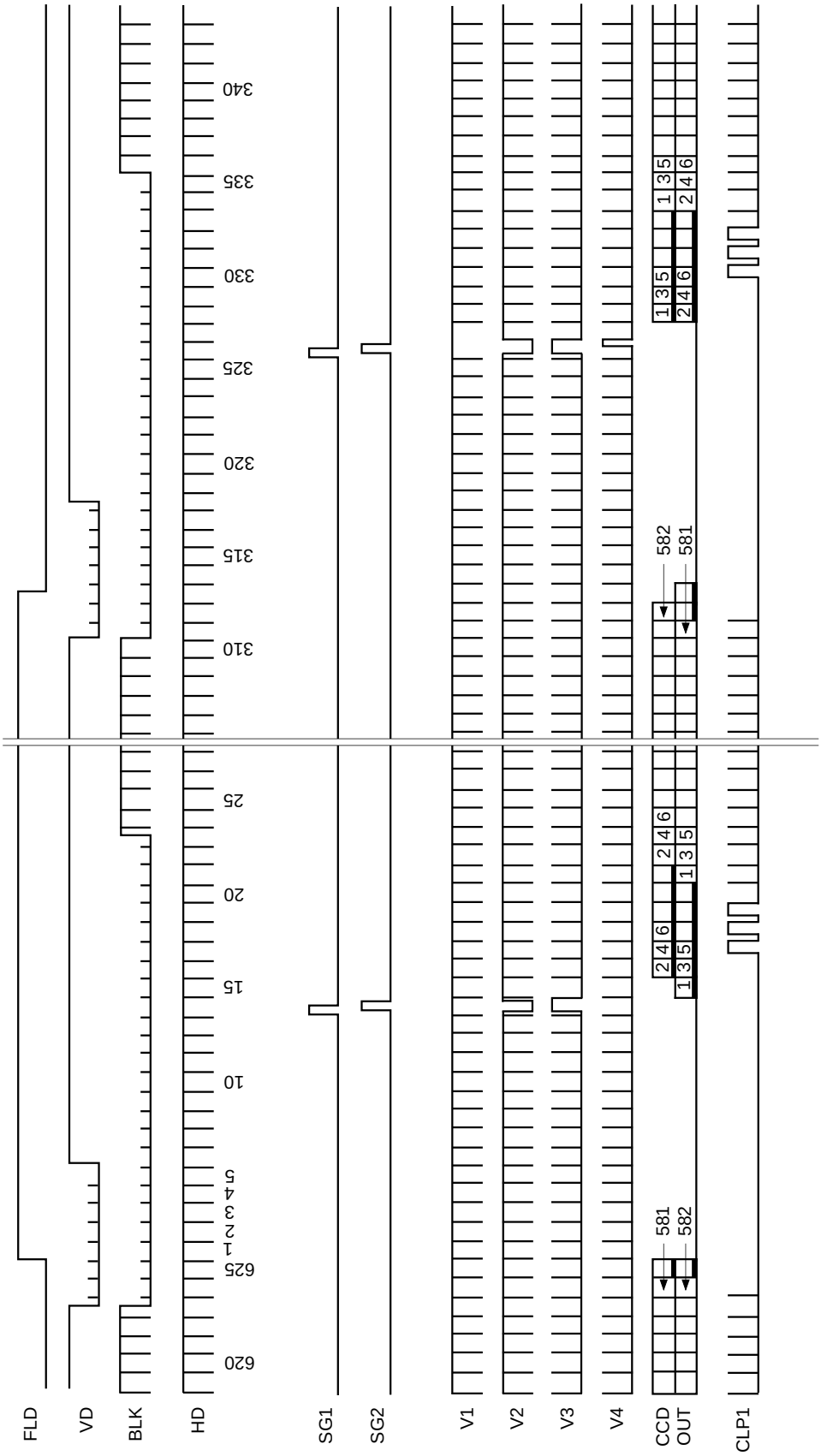
(Includes lens characteristics, excludes light source characteristics)



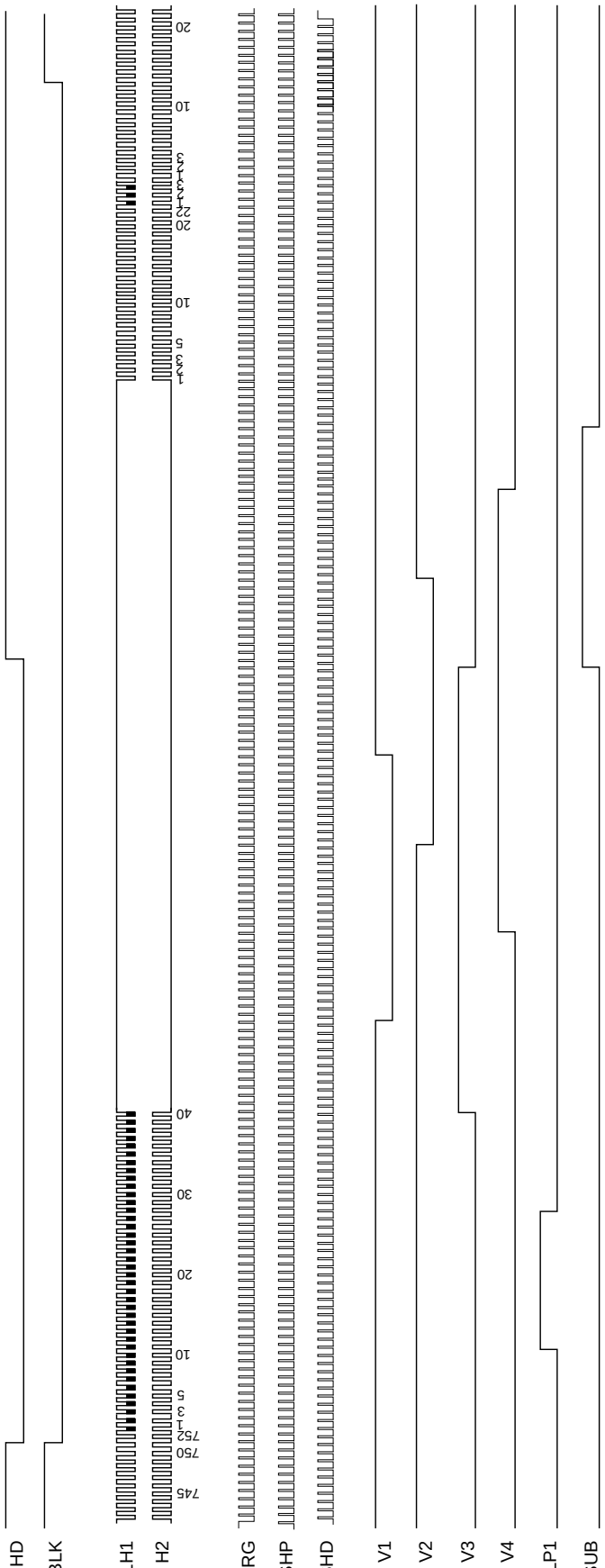
Sensor Readout Clock Timing Chart



Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

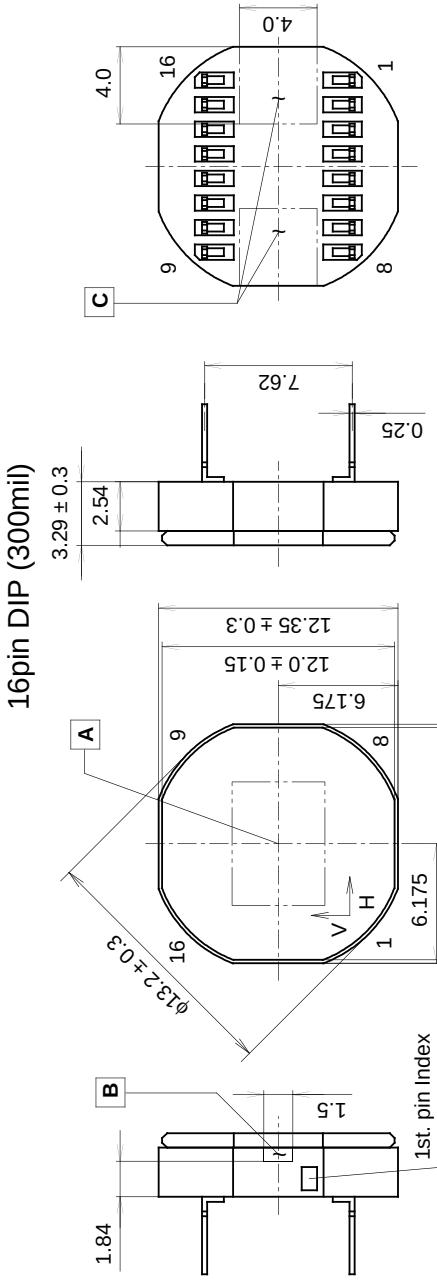
3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.
   a) Operate in clean environments (around class 1000 is appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods.
   For continuous using under cruel condition exceeding the normal using condition, consult our company.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm



1. **"A"** is the center of the effective image area.
2. The point **"B"** of the package is the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package is the height reference.
4. The center of the effective image area relative to the center of the package (*) is (H, V) = (0, 0) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 60µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.

* Center of the package : The center is halfway between two pairs of opposite sides, as measured from **"B"**, **"B'"**.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.9g