HARRIS Semiconductor

IH401A

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
Call Central Applications 1-800-442-7747
or email: centapp@harris.com

April 1999

QUAD Varafet Analog Switch

Features

- $r_{DS(ON)}$ (Typ) 35Ω
- $I_{D(OFF)}$ (Typ) 10pA
- Switching Times (R_L = 1kΩ)
  - t_{ON} 25ns
  - t_{OFF} 75ns
- Built-In Overvoltage Protection . . . . . ±25V
- Charge Injection Error (Typ) into 0.01μF Capacitor . . 3mV
- C_{ISS} (Typ) . . . . . <1pF
- Can Be Used for Hybrid Construction

Part Number Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
IH401A	-55 to 125	16 Ld CERDIP

Description

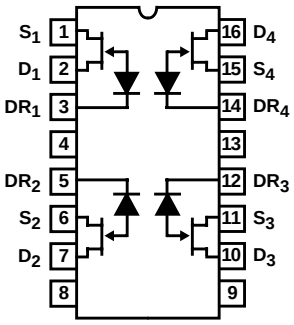
The IH401A is made up of 4 monolithically constructed combinations of varacitor type diode and a N-Channel JFET. The JFET itself is very similar to the popular 2N4391, and the driver diode is specially designed, such that its capacitance is a strong function of the voltage across it. The driver diode is electrically in series with the gate of the N-Channel FET and simulates a back-to-back diode structure. This structure is needed to prevent forward biasing the source-to-gate or drain-to-gate junctions of the JFET when used in switching applications.

Previous applications of JFETs required the addition of diodes, in series with the gate, and then perhaps a gate-to-source referral resistor or a capacitor in parallel with the diode; therefore, at least 3 components were required to perform the switch function. The IH401A does this same job in one component (with a great deal better performance characteristics).

Like a standard JFET, the practically perform a solid state switch function translator should be added to drive the diode. This translator takes the TTL levels and converts them to voltages required to drive the diode/FET system (typically a 0V to -15V translation and a 3V to +15V shift). With ±15V power supplies, the IH401A will typically switch $22V_{P-P}$ at any frequency from DC to 20MHz, with less than 50Ω $r_{DS(ON)}$.

Pinout

IH401A
(CERDIP)
TOP VIEW



File Number **3128.2**

Absolute Maximum Ratings

Supply Voltage
- V_S to V_D 35V
- V_G to V_S, V_D 35V

Thermal Information

Maximum Junction Temperature (Ceramic Package) . . . . . 175^oC
Storage Temperature Range . . . . . -65^oC to 150^oC
Lead Temperature (Soldering, 10s) . . . . . 300^oC

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At $25^oC/125^oC$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Switch "ON" Resistance	$r_{DS(ON)}$	V_{DRIVE} = 15V, V_{DRAIN} = -10V, I_D = 10mA	-	35	50	Ω
Pinch-Off Voltage	V_P	I_D = 1nA, V_{DS} = 10V	2	4	5	V
Switch "OFF" Current or "OFF" Leakage	$I_{D(OFF)}$	V_{DRIVE} = -15V, V_{SOURCE} = -10V, V_{DRAIN} = +10V	-	10	±500	pA
Switch "OFF" Leakage at 125^oC	$I_{D(OFF)}$	V_{DRIVE} = -15V, V_{SOURCE} = -10V, V_{DRAIN} = +10V	-	0.25	50	nA
Switch "OFF" Current	$I_{S(OFF)}$	V_{DRIVE} = -15V, V_{DRAIN} = -10V, V_{SOURCE} = +10V	-	10	±500	pA
Switch "OFF" Leakage at 125^oC	$I_{S(OFF)}$	V_{DRIVE} = -15V, V_{SOURCE} = -10V, V_{DRAIN} = +10V	-	0.3	50	nA
Switch Leakage When Turned "ON"	$I_{D(ON)}$ = $I_{S(ON)}$	V_D = V_S = -10V, V_{DRIVE}= +15V	-	0.02	±2	nA
AC Input Voltage Range without Distortion	V_{ANALOG}	See Figure 2	20	22	-	V_{P-P}
Charge Injection Amplitude	V_{INJECT}	See Figure 3	-	3	-	mV_{P-P}
Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	BV_{DIODE}	V_D = V_S = -V, I_{DRIVE} = 1µA, DRIVE = 0V	-30	-45	-	V
Gate to Source or Gate to Drain Reverse Breakdown Voltage	BV_{GSS}	V_{DRIVE} = -V, V_D = V_S = 0V, DRIVE = 1µA	30	41	-	V
Maximum Current Switch can Deliver (Pulsed)	I_{DSS}	V_{DRIVE} = 15V, V_S = 0V, D = +10V	35	55	-	mA
Switch "ON" Time (Note 1)	t_{ON}	See Figure 1	-	50	-	ns
Switch "OFF" Time (Note 1)	t_{OFF}	See Figure 1	-	150	-	ns

NOTE:

1. Driving waveform must be >100ns rise and fall time.

Test Circuits

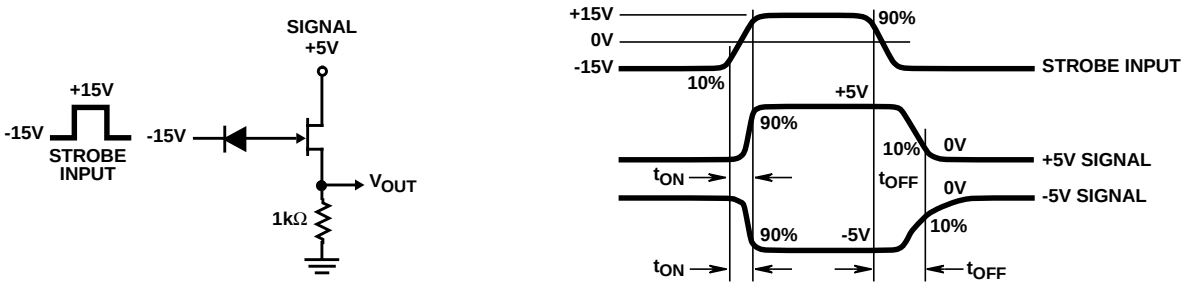


FIGURE 1. SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

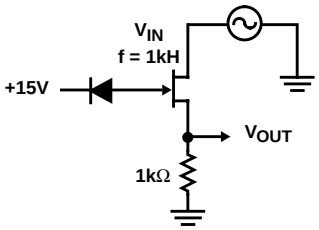


FIGURE 2. ANALOG INPUT VOLTAGE RANGE TEST CIRCUIT

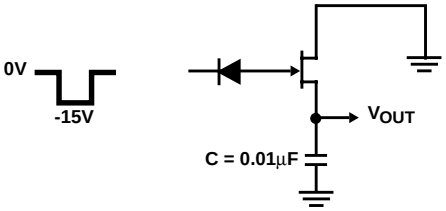


FIGURE 3. CHARGE INJECTION TEST CIRCUIT

Applications

IH401A Family

In general, the IH401A family can be used in any application formally using a JFET/isolation diode combination (2N4391 or similar). Like standard FET circuits, the IH401A requires a translator for normal analog switch function. The translator is used to boost the TTL input signals to the ±15V analog supply levels which allow the IH401A to handle ±10V analog signals. A typical simple PNP translator is shown in Figure 4.

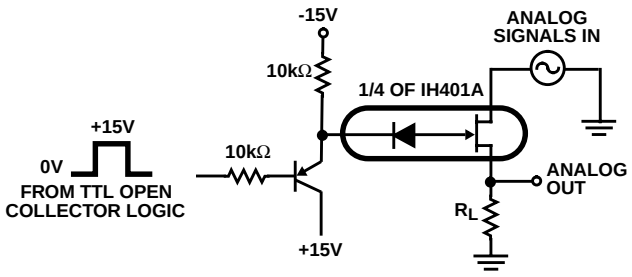


FIGURE 4. TYPICAL SIMPLE PNP TRANSLATOR

Although this simple PNP circuit represents a minimum of components, it requires open collector TTL input and $t_{(OFF)}$ is limited by the collector load resistor (approximately 1.5μs for 10kΩ). Improved switching speed can be obtained by increasing the complexity of the translator stage.

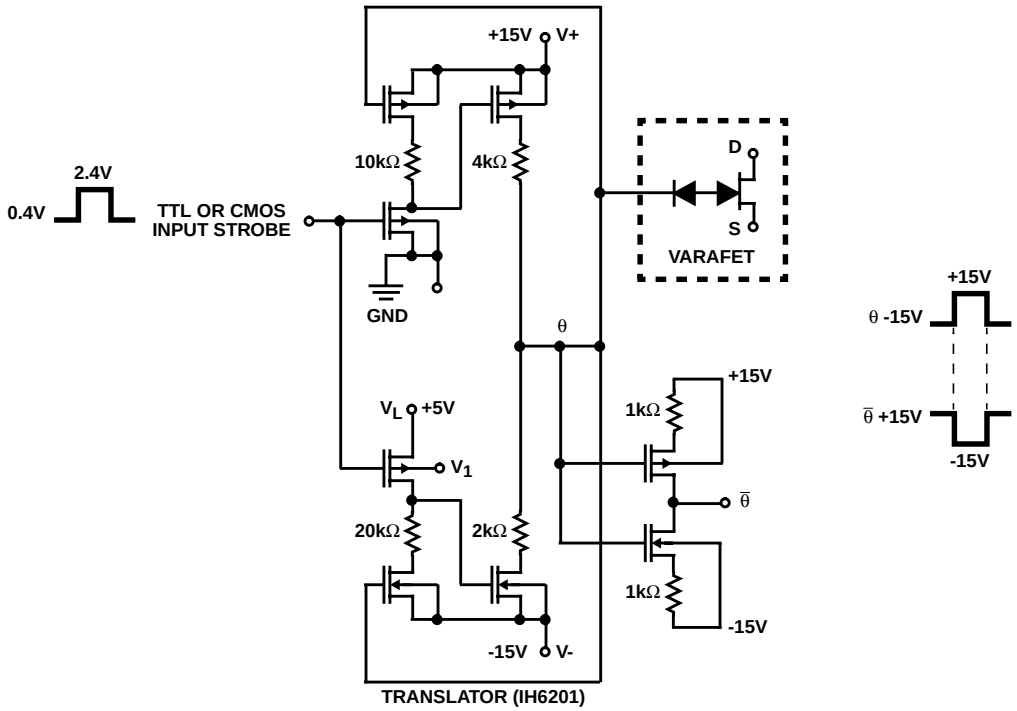
A translator which overcomes the problems of the simple PNP stage is the Harris IH6201 (See Note). This translator driving an IH401A varafet produces the following typical features:

- t_{ON} time of approx. 200ns } break before
- t_{OFF} time of approx. 80ns } make switch
- TTL compatible strobing levels of 2.4V / 0.4V
- $I_{D(ON)} + I_{S(ON)}$ typically 20pA up to ±10V analog signals
- $I_{D(OFF)}$ or $I_{S(OFF)}$ typically 20pA
- Quiescent current drain of approx. 100nA in either "ON" or "OFF" case

NOTE: The IH6201 is a dual translator (two independent translators per package) constructed from monolithic CMOS technology. The schematic of one-half IH6201, driving one-fourth of an IH401A, is shown in Figure 5.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401A can combine to make a SPDT switch, or an IH6201 plus an IH401A can make a dual SPDT analog switch. (See Figure 8)

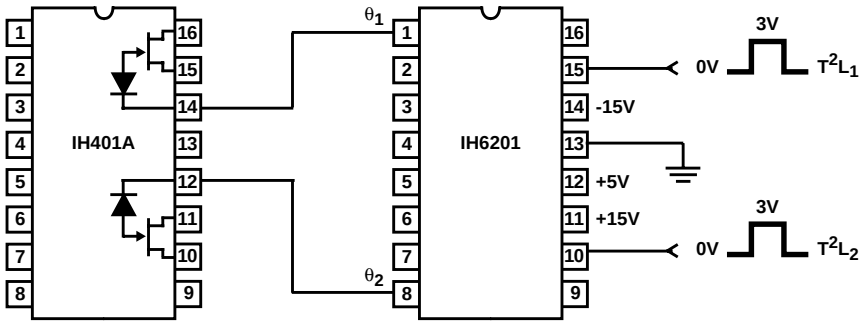
Typical Application Schematic ($^1/_2$ of IH401A, Driving $^1/_4$ of an IH401A)



NOTE: Each transistor output has a θ and output. $\overline{\theta}$ is just the inverse of θ, i.e., ($\overline{\theta}$ output is 180 degrees out of phase with respect to θ output).

FIGURE 5. IH6201 DRIVING AN IH401A

Switching Information



NOTE: Either switch is turned on when strobe input goes high.

FIGURE 6. DUAL SPST ANALOG SWITCH

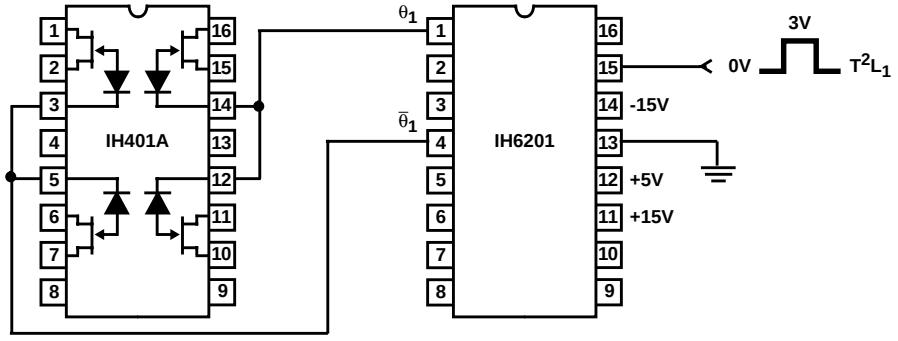


FIGURE 7. DPDT ANALOG SWITCH

Switching Information (Continued)

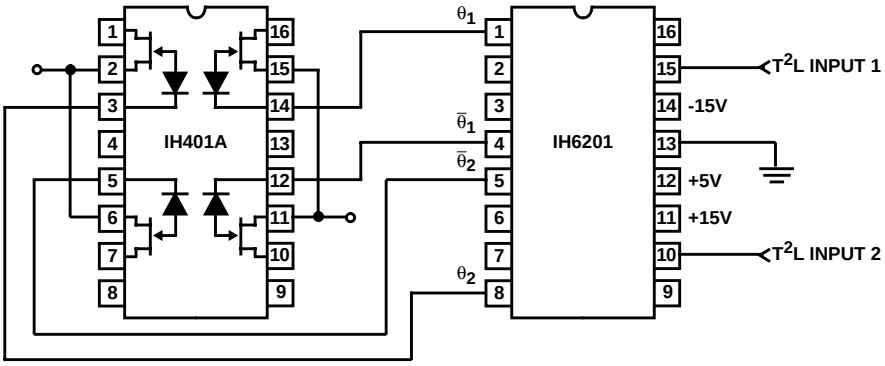


FIGURE 8. DUAL SPDT ANALOG SWITCH

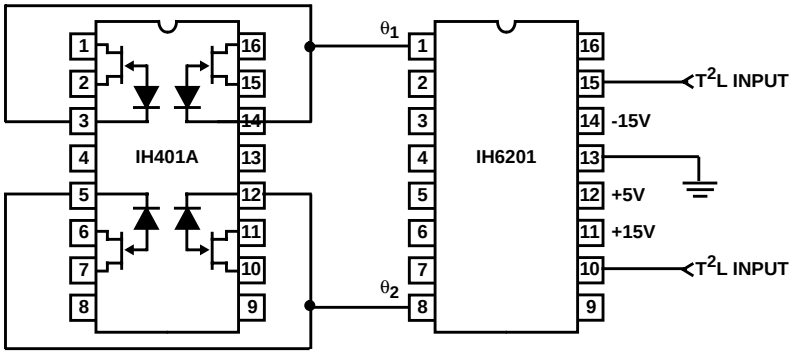


FIGURE 9. DUAL DPST ANALOG SWITCH