IMD10AMT1G

Dual Bias Resistor Transistor

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

- High Current: I_C = 500 mA max
- This is a Pb−Free Device

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector−Base Voltage	$V_{(BR)CBO}$	50	Vdc
Collector−Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter−Base Voltage	$V_{(BR)EBO}$	5.0	Vdc
Collector Current − Continuous	I_C	500	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Power Dissipation*	P_D	285	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
*Total for both Transistors.

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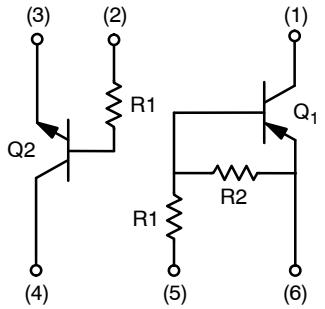
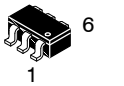
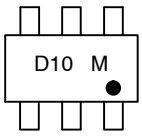


SC−74



SC−74R
318AA
Style 21

MARKING DIAGRAM



D10 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
IMD10AMT1G	SC−74R	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

April, 2012 − Rev. 0

Publication Order Number:
IMD10AMT1G/D

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1(PNP) omitted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Base Breakdown Voltage (I_C = 50 μAdc, I_E = 0 A)	$V_{(BR)CBO}$	50	–	Vdc
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0 A)	$V_{(BR)CEO}$	50	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 50 μAdc, I_C = 0 A)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector–Base Cutoff Current (V_{CB} = 50 Vdc, I_E = 0 A)	I_{CBO}	–	100	nA
Emitter–Base Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0 A)	I_{EBO}	–	0.5	mA
Collector–Emitter Cutoff Current (V_{CE} = 15 Vdc, I_B = 0 A)	I_{CEO}	–	500	nA
Collector–Emitter Cutoff Current (V_{CE} = 25 Vdc, I_B = 0 A)	I_{CES}	–	100	nA
ON CHARACTERISTICS (Note 1)				
DC Current Gain (V_{CE} = 5.0 V, I_C = 100 mA) Q1(PNP) (V_{CE} = 5.0 V, I_C = 1.0 mA) Q2(NPN)	h_{FE}	 68 100	 – 600	
Collector–Emitter Saturation Voltage (I_C = 10 mA, I_B = 1.0 mA)	$V_{CE(sat)}$	–	0.3	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	–	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	V_{OL}	4.9	–	Vdc
Input Resistor Q1(PNP) Q2(NPN)	R1	 70 7.0	 130 13	 Ω kΩ
Resistor Ratio Q1(PNP) Q2(NPN)	R1/R2	 0.008 –	 0.012 –	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle < 2.0%.

TYPICAL CHARACTERISTICS (NPN)

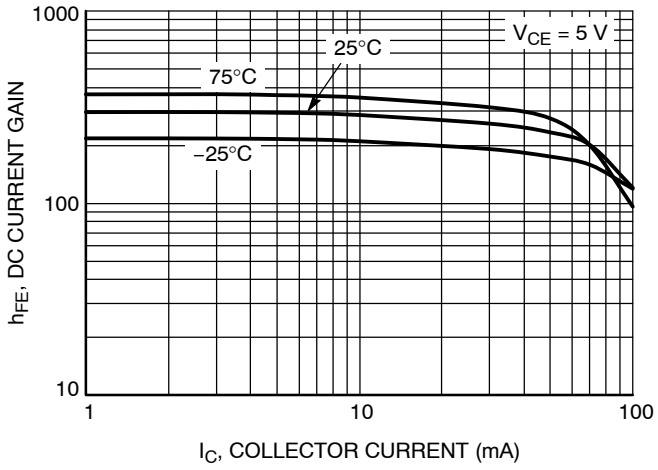


Figure 1. DC Current Gain

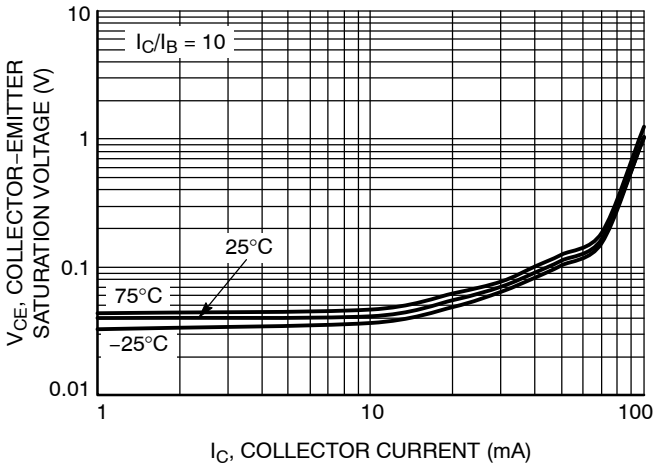


Figure 2. Collector−Emitter Saturation Voltage

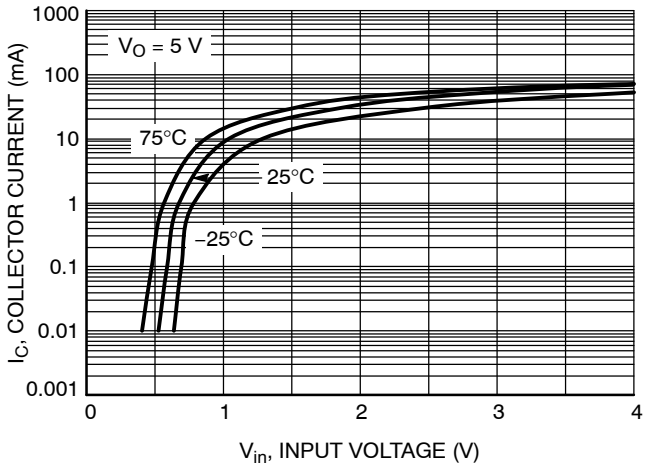


Figure 3. Output Current vs. Input Voltage

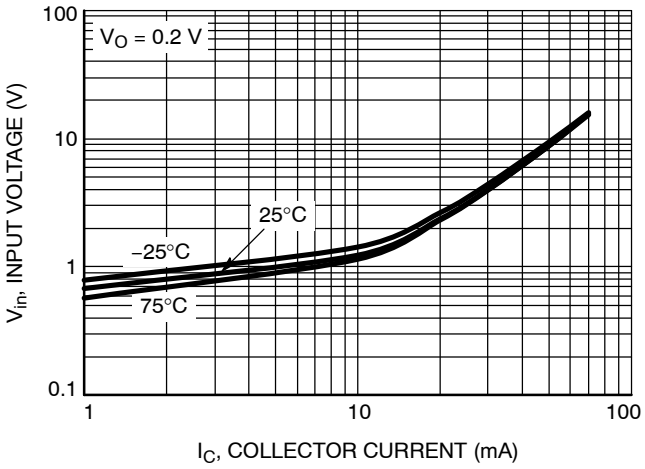


Figure 4. Input Voltage vs. Output Current

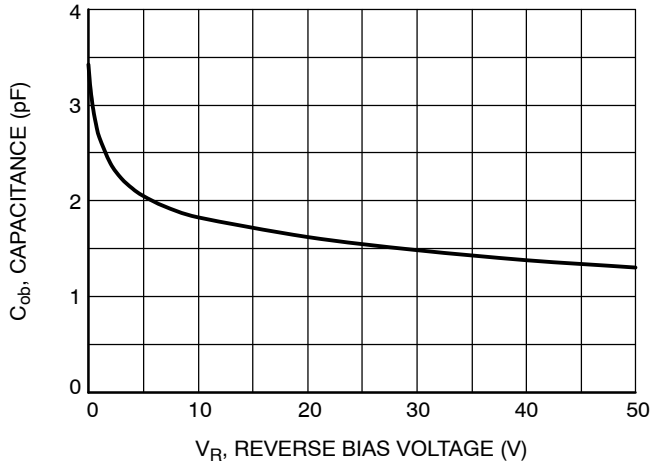


Figure 5. Output Capacitance

TYPICAL CHARACTERISTICS (PNP)

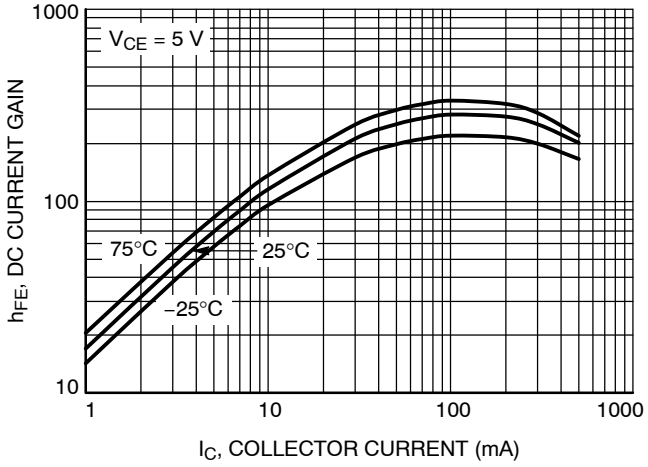


Figure 6. DC Current Gain

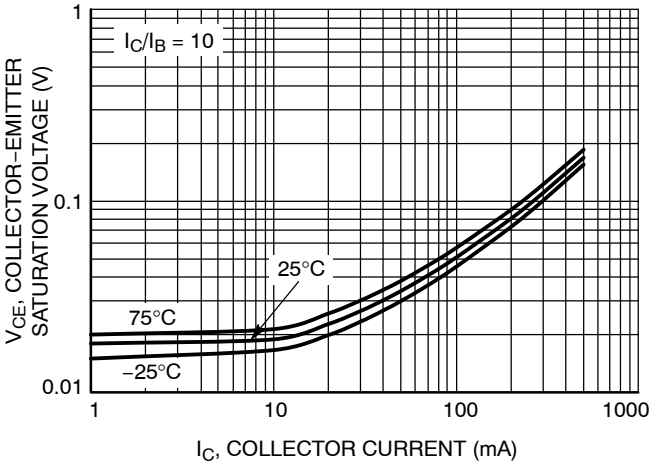


Figure 7. Collector−Emitter Saturation Voltage

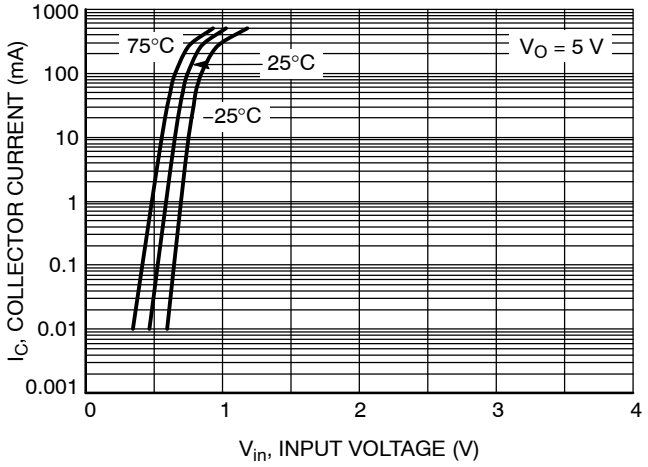


Figure 8. Output Current vs. Input Voltage

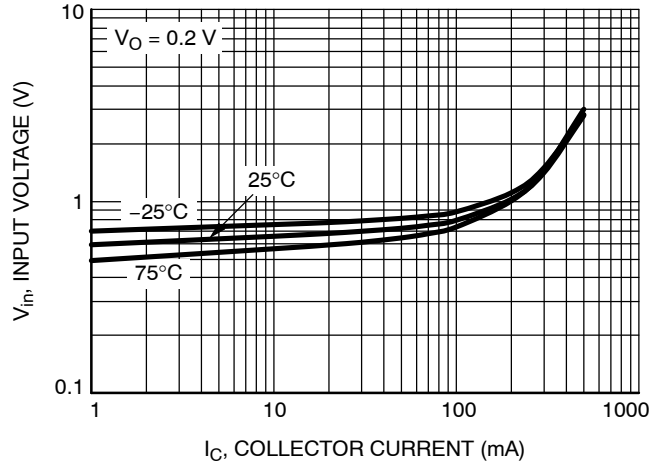


Figure 9. Input Voltage vs. Output Current

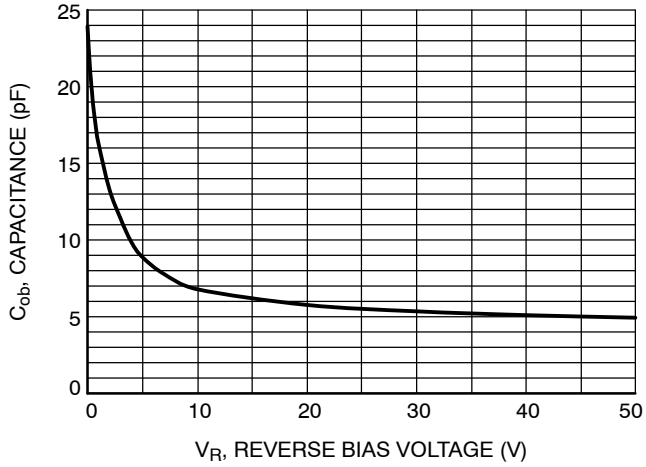
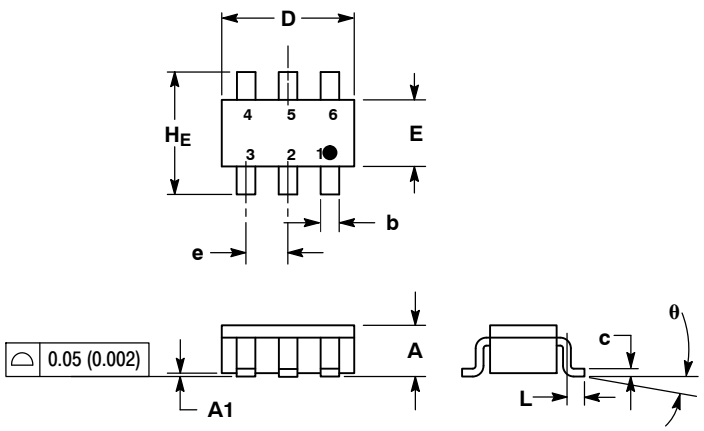


Figure 10. Output Capacitance

PACKAGE DIMENSIONS

SC−74R
CASE 318AA−01
ISSUE B

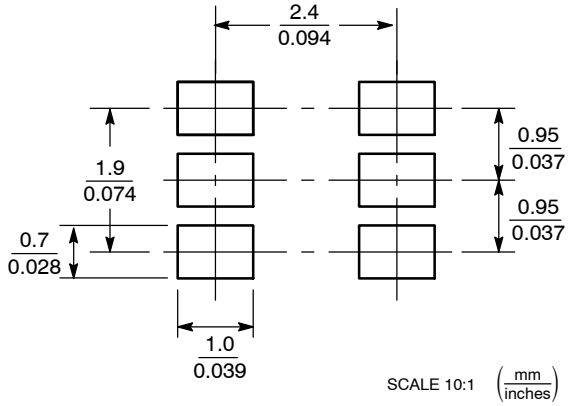


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

STYLE 21:
PIN 1. COLLECTOR 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. EMITTER 1
6. BASE 1

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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