Wireless LAN Integrated Medium Access Controller with Baseband Processor

The Intersil ISL3890 Wireless LAN Integrated Media Access Controller with Baseband Processor is part of the PRISM® Duette, Dual Band radio chipset. The ISL3890 directly interfaces with Intersil's ISL3690 Dual Band Direct Conversion transceiver. Adding Intersil's ISL3090 10GHz VCO and Intersil's ISL3990 Dual Band Power Amp completes an end-to-end WLAN Chipset solution providing both 5GHz 802.11a and 2.4GHz 802.11b/g standards. The 802.11 protocol is implemented in firmware supporting custom WLAN solutions.

Firmware implements the full IEEE 802.11 Wireless LAN MAC protocol. It supports BSS and IBSS operation under DCF, and operation under the optional Point Coordination Function (PCF). Low level protocol functions such as RTS/CTS generation and acknowledgment, fragmentation and de-fragmentation, and automatic beacon monitoring are handled without host intervention. Active scanning is performed autonomously once initiated by host command. Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers.

Orthogonal Frequency Division Multiplexing (OFDM) of 52 sub-carriers modulated with BPSK, QPSK, 16QAM or 64QAM and a variety of convolutional coding rates provides 8 selectable data rates at 2.4GHz and 5GHz. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability along with Complementary Code Keying provide an additional 4 selectable data rates at 2.4GHz.

Built-in flexibility allows the ISL3890 to be configured for a range of applications. The MAC is based on the ARM 946E processor core that offers a wide variety of code development support tools.

The ISL3890 is housed in a thin plastic BGA package suitable for CardBus or Mini-PCI circuit card applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ISL3890IK	-40 to 85	256 Lead BGA	V256.17x17A
ISL3890IK-TK	-40 to 85	Tape and Reel	

Features

- Firmware implements the full IEEE 802.11a/b/g Wireless LAN MAC protocols
- Internal WEP Engine allows 64 or 128 bit Encryption
- AES Hardware Accelerator
- Start-up modes allow the PCI configuration registers or the Card Bus card information structure to be Initialized from a small external serial EEPROM. This allows firmware to be downloaded from the host.
- On-chip SRAM memory
- A low frequency crystal oscillator can maintain time, which allows the high frequency clock source to be powered off during sleep mode.
- Firmware controlled antenna diversity
- Data Rates: 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, & 54Mbps
- Modulation . . OFDM with BPSK, QPSK, 16QAM, 64QAM DBPSK, DQPSK, CCK
- Convolutional coding and interleaving on all OFDM rates
- Targeted for OFDM Multipath Delay Spreads > 800ns for 6Mbps, and > 100ns for 54Mbps
- Targeted for CCK Multipath Delay Spreads > 90ns at 11Mbps, >200ns at 5.5Mbps and >360ns at 1 and 2Mbps
- Direct interface with the ISL3690 Direct Conversion transceiver
- High Data Rate Wireless LAN Systems targeting the IEEE 802.11a and b/g standards.
- Cardbus32 Wireless LAN Adapters
- Mini-PCI Wireless LAN Cards
- 3V PCI Wireless LAN Adapters

Simplified Block Diagram