PRELIMINARY | Data Sheet | November 2002 | FN9096.0

Optimized Multi-Phase PWM Controller with adjustable voltage offset

The ISL6556A controls microprocessor core voltage regulation by driving up to 4 synchronous-rectified buck channels in parallel. Multi-phase buck converter architecture uses interleaved timing to multiply channel ripple frequency and reduce input and output ripple currents. Lower ripple results in fewer components, lower component cost, reduced power dissipation, and smaller implementation area.

The ISL6556A utilizes the $r_{DS(on)}$ current-sensing method to measure current in each phase and also generate droop current. To ensure the accuracy of Droop, An external NTC compensation circuit can be used tro completely nullify the effect of $r_{DS(on)}$ temperature sensitivity.

A unity gain, differential amplifier is provided for remote voltage sensing. Any potential difference between remote and local grounds can be completely eliminated using the remote-sense amplifier. The threshold-sensitive enable input is available to accurately coordinate the start up of the ISL6556A with any other voltage rail. Dynamic-VID™ technology allows seamless on-the-fly VID changes. The offset pin allows accurate voltage offset settings that are independent of VID setting. The ISL6556A uses a 5V bias and has a built-in shunt regulator to allow 12V bias using only a small external limiting resistor

Ordering Information

PART NUMBER	TEMP. (^{O}C)	PACKAGE	PKG. NO.
ISL6556ACB	0 to 70	28-PIN SOIC	M28.3
ISL6556ACR	0 to 70	32-PIN QFN	L32.5X5B

Features

- Precision Multi-Phase Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Life, Load, Line and Temperature
  - Adjustable Reference-Voltage Offset
- Precision $R_{DS(on)}$ Current Sensing
  - Accurate Load-Line Programming
  - Accurate Channel-Current Balancing
  - Low-Cost, Lossless Current Sensing
- Internal Shunt Regulator for 5V or 12V Biasing
- Microprocessor Voltage Identification Input
  - Dynamic VID™ technology
  - 6-Bit VID Input
  - .8375V to 1.600V in 12.5mV Steps
- Threshold-Sensitive Enable Function for synchronizing with driver POR
- Over Current Protection
- Over-Voltage Protection
  - No Additional External Components Needed
  - OVP Pin to drive Crowbar Device

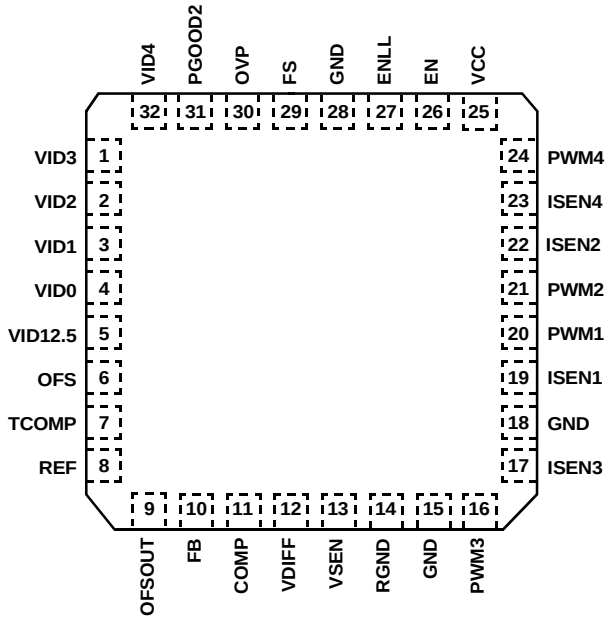
2, 3, or 4 Phase Operation

Applications

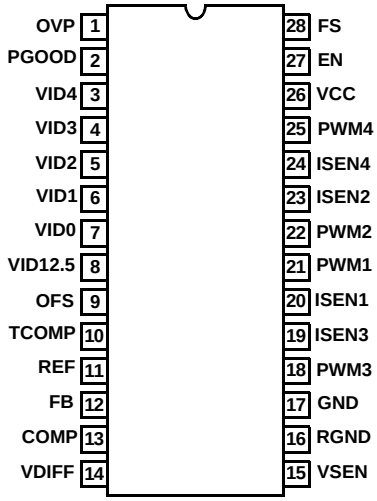
- Computer DC/DC converter VRM/VRD10.0
- Computer DC/DC Converter VRM/VRD9.X
- Telecom DC/DC

Pinouts

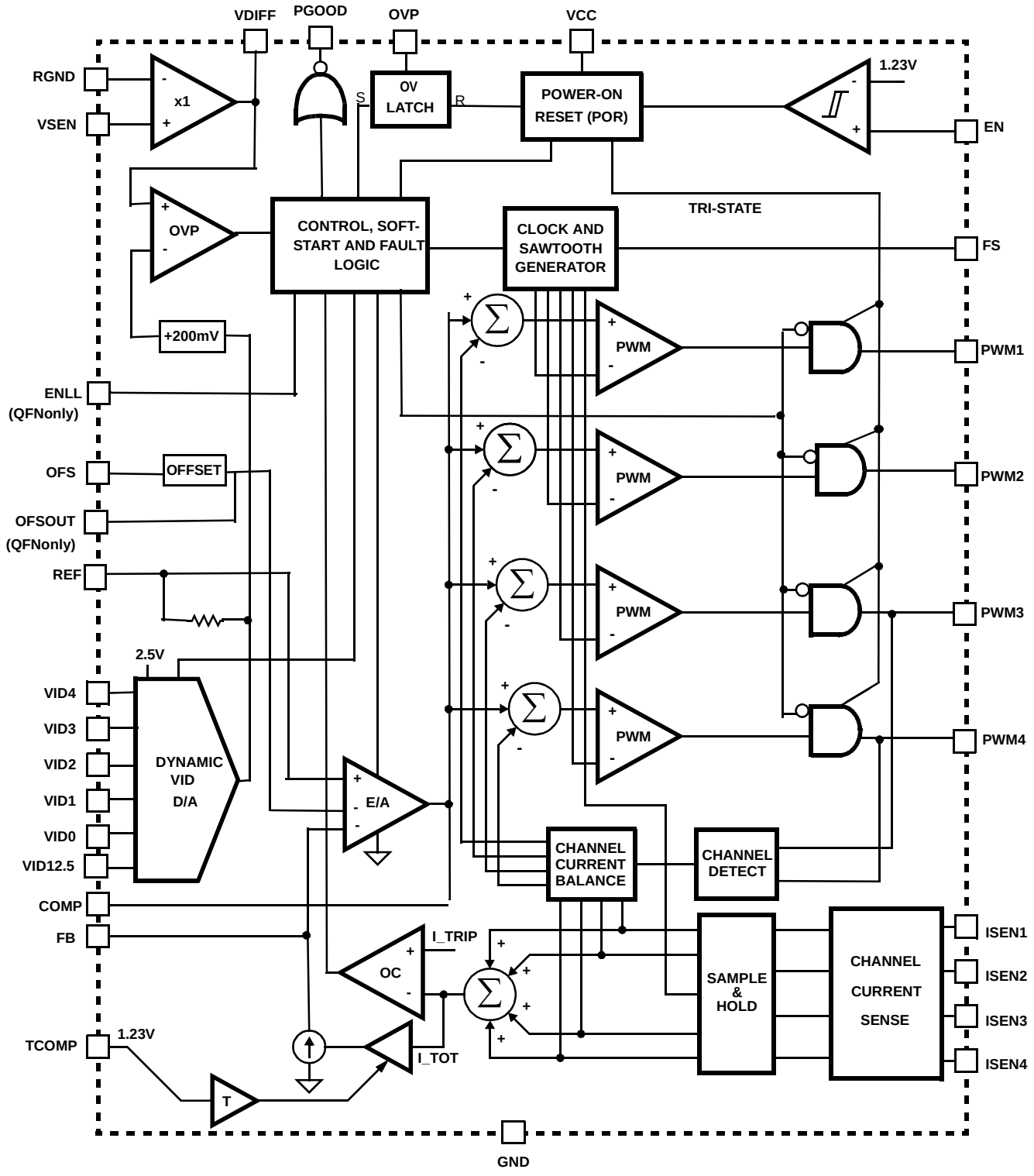
ISL6556ACR (32 LEAD QFN)
TOP VIEW



ISL6556ACB (28 LEAD SOIC)
TOP VIEW



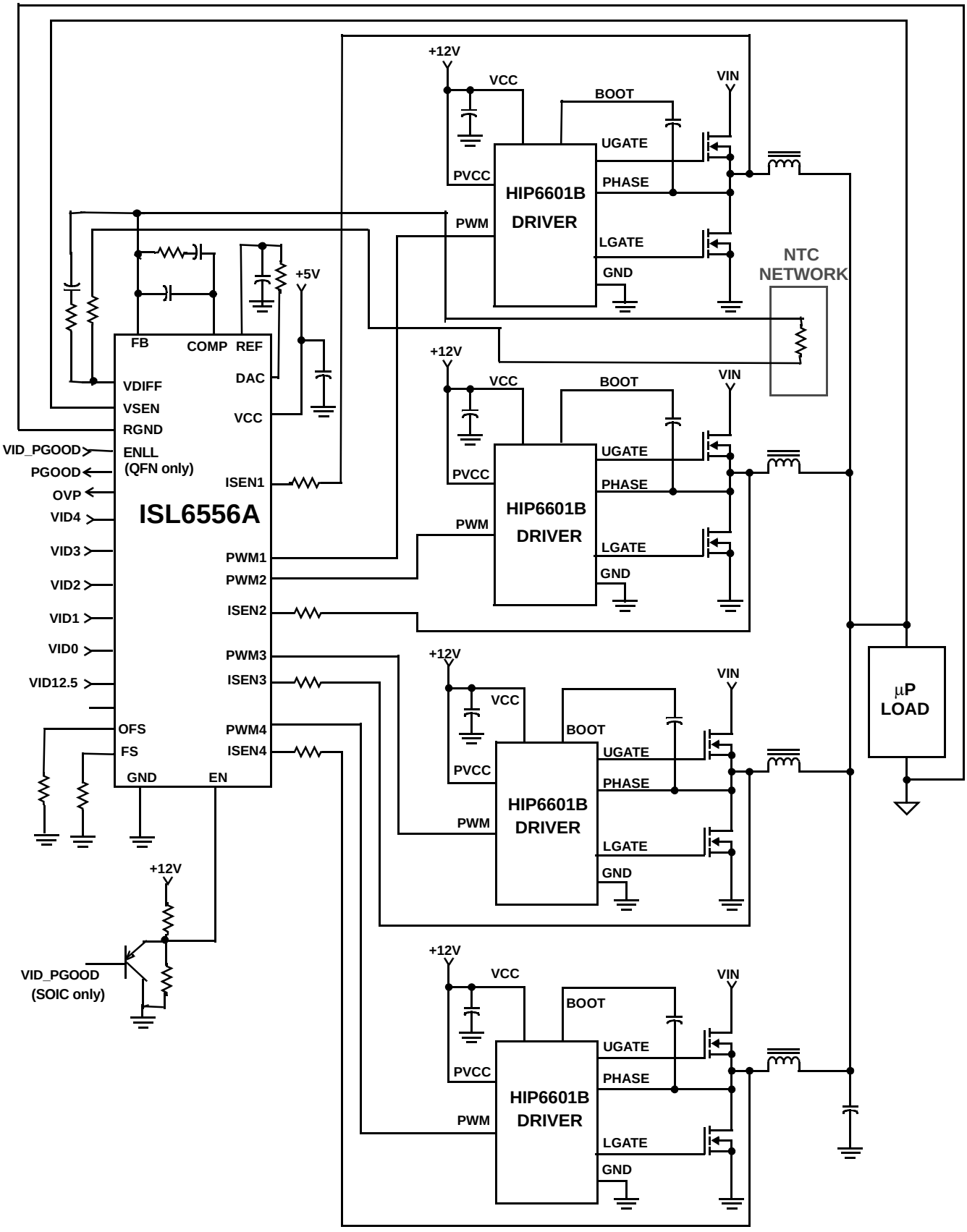
Block Diagram



NOTES:

1. These parts are designed and adjusted for accuracy within the system tolerance given in the Electrical Specifications. The system tolerance accounts for offsets in the differential and error amplifiers; reference-voltage inaccuracies; temperature drift; and the full DAC adjustment range.
2. VID input levels above 2.9V may produce an reference-voltage offset inaccuracy.

Typical Application



Functional Pin Description

VCC

Bias supply voltage for the controller. Connect this pin directly to a 5V power supply or to a 12V power supply through a 300ohm resistor.

GND

Return for VCC and signal ground for the IC.

EN

This pin is a threshold-sensitive enable input for the controller. Connecting the 12V supply to EN through an appropriate resistor divider provides a means to synchronize power-up of the controller and the FET driver ICs. When EN is driven above 1.23V, the ISL6556A is active depending on status of ENLL, the internal POR, and pending fault states. Driving EN below 1.23 volts will clear all fault states and prime the ISL6556 to softstart when re-enabled.

ENLL

This pin is implemented in QFN ISL6556A only. It's a logic-level enable input for the controller. When asserted to a logic high, the ISL6556A is active depending on status of EN, the internal POR, VID inputs and pending fault states. Deasserting ENLL will clear all fault states and prime the ISL6556A to softstart when re-enabled.

FS

This pin has two functions. A resistor replaced from FS to ground will set the switching frequency. There is an inverse relationship between the value of the resistor and the switching frequency. This pin can also be used to disable the controller. To disable the controller, pull this pin below 1V.

VID4, VID3, VID2, VID1, VID0, and VID12.5

These are the inputs to the internal DAC that provides the reference voltage for output regulation. Connect these pins to either open-drain with external pullup resistors or active-pull-up type outputs. VID4-VID12.5 have low current (20uA) internal pullups.

VDIFF, VSEN, and RGND

VSEN and RGND form the differential inputs to an amplifier configured as a bridge circuit with precision internal resistors. The amplifier bridge converts the remotely sensed differential voltage of the regulated output to a single-ended voltage, referenced to the local ground of the controller. VDIFF is the amplifier's output and the input to the regulation and protection circuitry. Connect VSEN and RGND to the sense pins of the remote load.

FB and COMP

Inverting input and output of the internal error amplifier repectiively. FB is connected to VDIFF through an RC network with a DC resistiive connection. A negative current, proportional to output current is present on the REF pin. By placing a properly sized load line set resistor between VDIFF and FB a precision output impedance (i.e. - "load line") can be implemented. The droop scale factor is set by the ratio of the ISEN resistors and the lower MOSFET $r_{DS(on)}$.

COMP is tied back to FB through an external R-C network with no DC connection for compensating the regulator.

DAC and REF

The DAC output pin is the output of the precision internal DAC reference. The REF input pin is the positive input of the Error Amp. In typical application, a 1% 1k ohm resistor is used between DAC and REF to generate a offset voltage. This voltage is proportional to the offet current determined by the offset resistor from OFS pin to the ground. A capacitor is used to between REF pin to the Ground.

PWM3, PWM2, PWM1, PWM4

Pulse-width modulating outputs. These logic outputs command the driver IC(s) when to turn on and off the synchronous buck MOSFETs of each channel.

ISEN4, ISEN3, ISEN2, ISEN1

Current sense inputs. The ISEN4, ISEN3, ISEN2, and ISEN1 pins are held to a virtual ground such that a resistor connected between them and the drain terminal of the associated lower MOSFET will carry a current proportional to the current flowing through the related channel. The current is determined by the negative voltage developed across the lower MOSFET's $r_{DS(on)}$ which is the channel current scaled by the inverse of the $r_{DS(on)}$. The current is used as a reference for channel balancing, protection, and regulation (via the FB pin).

PGOOD

PGOOD is an open-drain logic output that is low impedance until the VSEN voltage falls within regulation tolerances.

OFS and OFSOUT

The OFS pin provides a programmable means to introduce a DC offset current which can be used to generate DC offset voltage to the DAC reference. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unterminated.

The OFSOUT pin is implemented in 32-lead QFN ISL6556A only. It's the output of offset current. Is this pin is connected to REF pin, the offset current flows through the resistor between DAC and REF pin.FB Depending on where this pin will be connected to FB will generate a DC offset Voltage to the DAC reference.

In 28-lead SOIC ISL6556A, the OFS is internally tied to REF pin.

OVP

A latched over-voltage indicator. Once tripped OVP remains set until power is cycled.generated via an external resistor

and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unterminated.

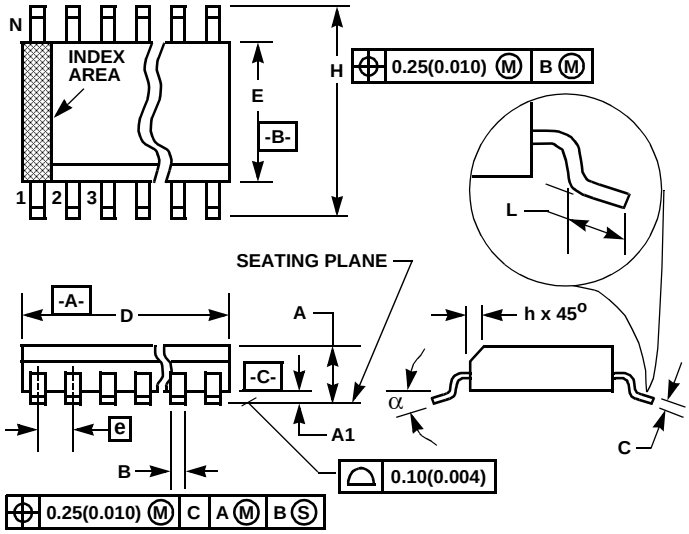
VID Code

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.8500V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.8750V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.9000V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.9250V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.9500V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V0
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.0000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.0250v
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.0500V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.0750V
0	0	0	0	0	0	1.0875V
1	1	1	1	1	1	OFF
1	1	1	1	1	0	OFF
1	1	1	1	0	1	1.1000V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.1250V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.1500V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.1750V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.2000V
1	1	0	1	0	0	1.2125V
1	1	0	0	1	1	1.2250V
1	1	0	0	1	0	1.2375V
1	1	0	0	0	1	1.2500V

VID Code

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.2750V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.3000V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.3250V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.3500V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.3750V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.4000V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.4250V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.4500V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.4750V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.5000V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.5250V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.5750V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.600V

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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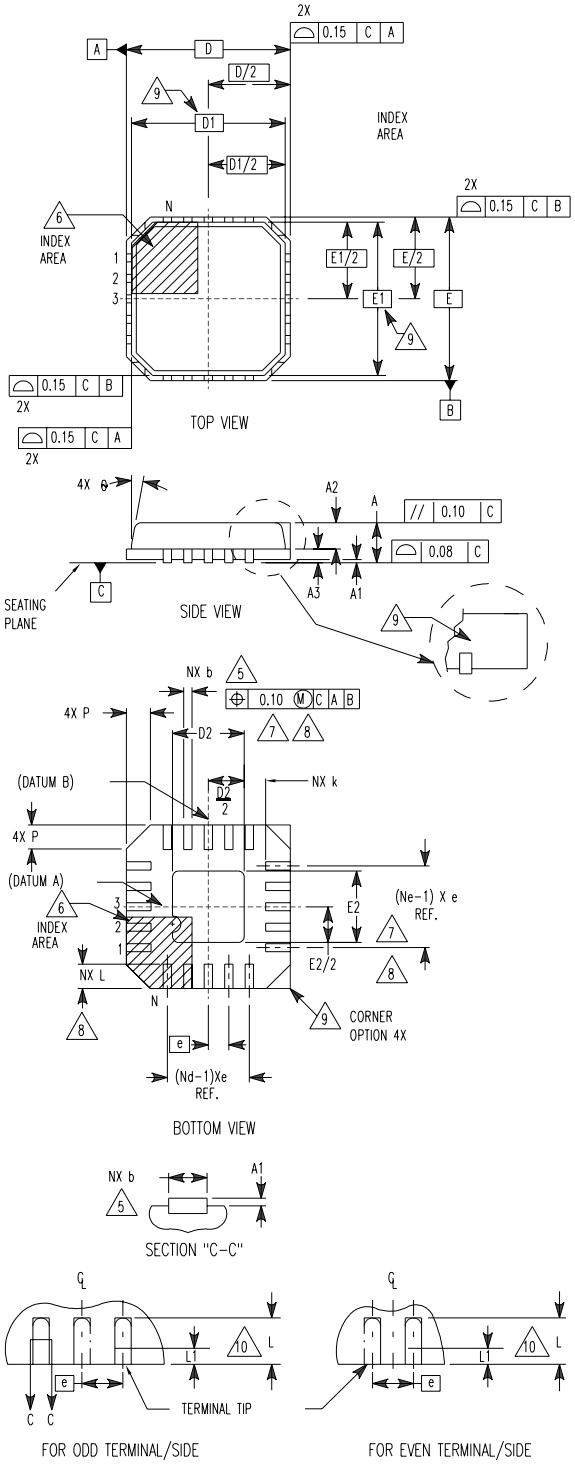
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.5x5B

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	3.15	3.30	3.45	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	3.15	3.30	3.45	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne		8		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.