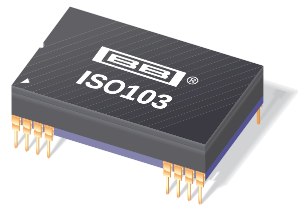
BURR - BROWN®



ISO103

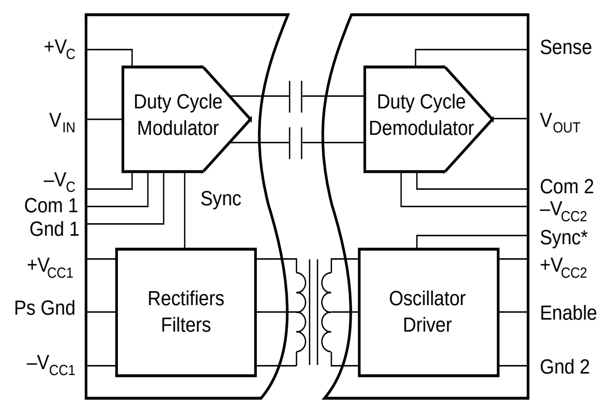
Low-Cost, Internally Powered ISOLATION AMPLIFIER

FEATURES

- SIGNAL AND POWER IN ONE DOUBLE-WIDE (0.6") SIDE-BRAZED PACKAGE
- 5600Vpk TEST VOLTAGE
- 1500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: –10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: ±10V to ±18V Input, ±50mA Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)
- BOARD AREA ONLY 0.72in.^{2} (4.6cm^2)

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- ISOLATED 4-20mA LOOP RECEIVER AND POWER
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION



*Ground if not used

DESCRIPTION

The ISO103 isolation amplifier provides both signal and power across an isolation barrier. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO103 easy to use, as well as providing for compact PC board layouts.

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SBOS001

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

		ISO103			ISO103B			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ISOLATION								
Rated Continuous Voltage(1)								
AC, 60Hz	T_{MIN} to T_{MAX}	1500			*			Vrms
DC	T_{MIN} to T_{MAX}	2121			*			VDC
Test Breakdown, 100% AC, 60Hz	10s	5657			*			Vpk
Isolation-Mode Rejection	1500Vrms, 60Hz		130			*		dB
	2121VDC		160			*		dB
Barrier Impedance			$10^{12} \parallel 9$			*		$\Omega \parallel pF$
Leakage Current	240Vrms, 60Hz		1	2		*	*	µA
GAIN								
Nominal			1			*		V/V
Initial Error			±0.12	±0.3		±0.08	±0.15	% FSR
Gain vs Temperature			±60	±100		±20	±50	ppm/°C
Nonlinearity	V_O = –10V to 10V		±0.026	±0.075		±0.018	±0.050	% FSR
	V_O = –5V to 5V		±0.009			*	±0.025	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			±20	±60		*	*	mV
vs Temperature			±300	±500		*	*	µV/°C
vs Power Supplies	V_{CC2} = ±10V to ±18V		0.9			*		mV/V
vs Output Supply Load	I_O = 0 to ±50mA		±0.3			*		mV/mA
SIGNAL INPUT								
Voltage Range	Output Voltage in Range	±10	±15		*	*		V
Resistance			200			*		kΩ
SIGNAL OUTPUT								
Voltage Range		±10	±12.5		*	*		V
Current Drive		±5	±15		*	*		mA
Ripple Voltage, 800kHz Carrier			25			*		mVp-p
	400Ω/4.7nF (See Figure 4)		5			*		mVp-p
Capacitive Load Drive			1000			*		pF
Voltage Noise			4			*		µV/√Hz
FREQUENCY RESPONSE								
Small Signal Bandwidth			20			*		kHz
Slew Rate			1.5			*		V/µs
Settling Time	0.1%, –10/10V		75			*		µs
POWER SUPPLIES								
Rated Voltage, V_{CC2}			±15			*		V
Voltage Range		±10		±18	*		*	V
Input Current	I_O = ±15mA		+90/–4.5			*		mA
	I_O = 0mA		+60/–4.5			*		mA
Ripple Current	No Filter		60			*		mAp-p
	C_{IN} = 1µF		3			*		mAp-p
Rated Output Voltage	Load = 15mA	±14.25	±15	±15.75	*	*	*	V
Output	50mA Balanced Load	10				*	*	V
	100mA Single-Ended Loads	10				*	*	V
Load Regulation	Balanced Load		0.3			*		%/mA
Line Regulation			1.12			*		V/V
Output Voltage vs Temperature			2.5			*		mV/°C
Voltage Balance Error, ±V_{CC1}			0.05			*		%
Voltage Ripple (800kHz)	No External Capacitors		50			*		mVp-p
	C_{EXT} = 1µF		5			*		mVp-p
Output Capacitive Load				1			*	µF
Sync Frequency	Sync-Pin Grounded (2)		1.6			*		MHz
TEMPERATURE RANGE								
Specification		–25		+85	*		*	°C
Operating		–25		+85	*		*	°C
Storage		–25		+125	*		*	°C

* Specifications same as ISO103.

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute. (2) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

ABSOLUTE MAXIMUM RATINGS

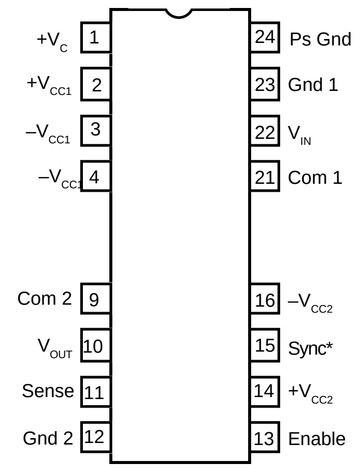
Supply Without Damage	±18V
V_{IN}, Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	1500Vrms
V_{ISO}, dv/dt	20kV/µs
Junction Temperature	150°C
Storage Temperature	–25°C to +125°C
Lead Temperature,10s	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



*Operation requires this pin be grounded or driven with TTL levels.

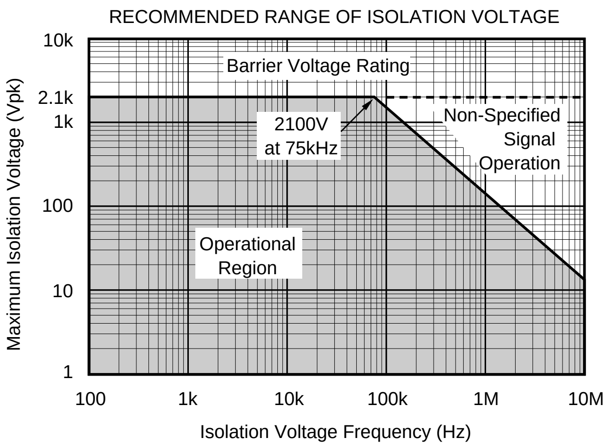
PACKAGE/ORDERING INFORMATION

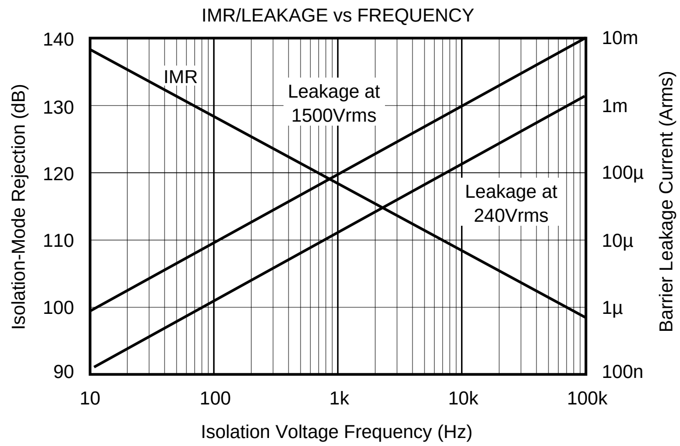
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
ISO103	24-Pin DIP	231	–25°C to +85°C			

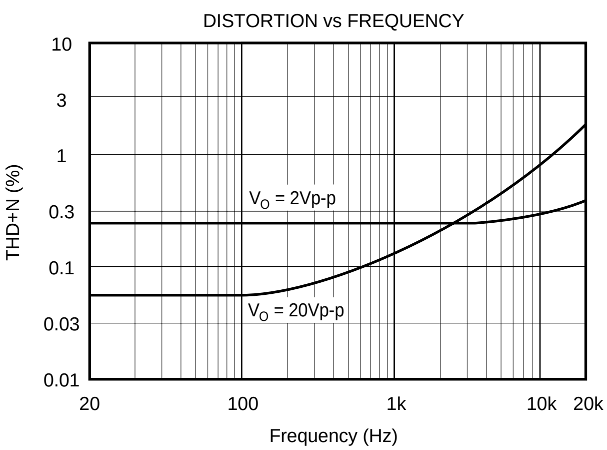
NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ISO103/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

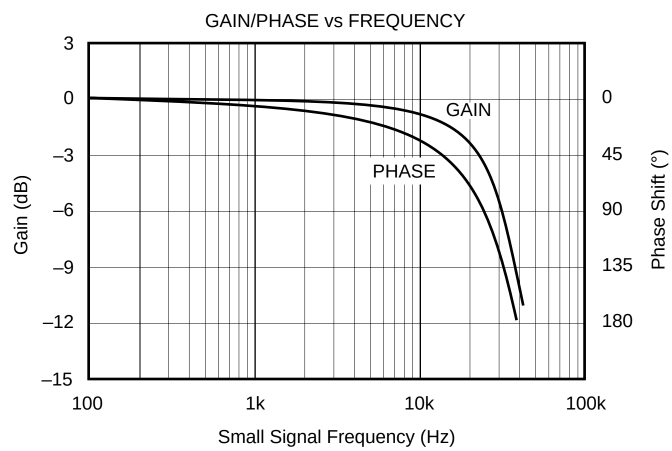
TYPICAL PERFORMANCE CURVES

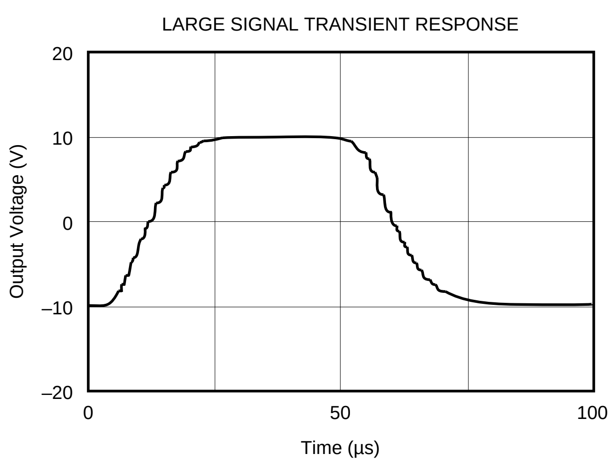
At T_A = +25°C, V_{CC2} = ±15VDC, ±15mA output current, unless otherwise noted.

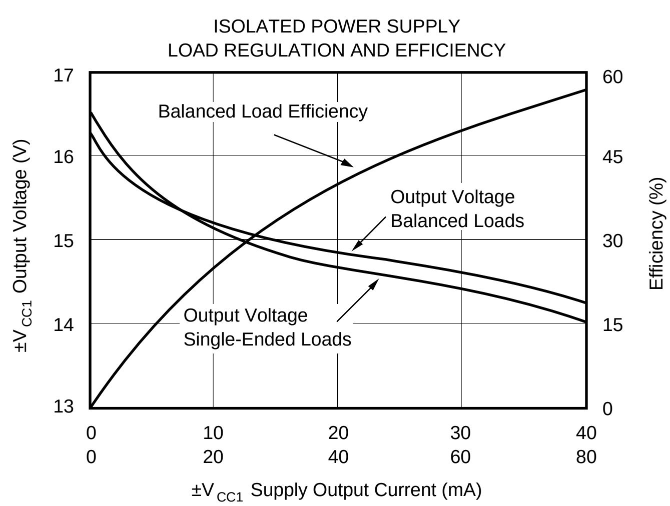






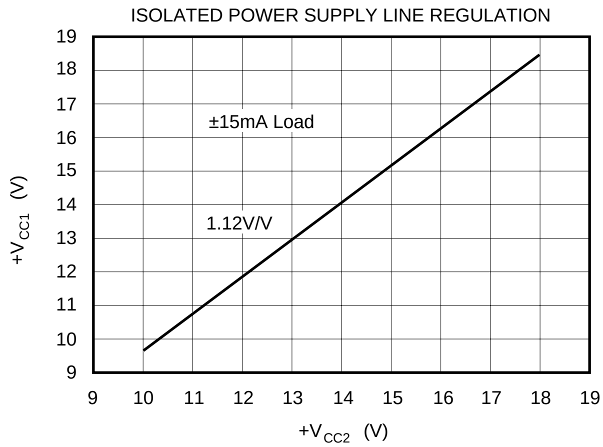


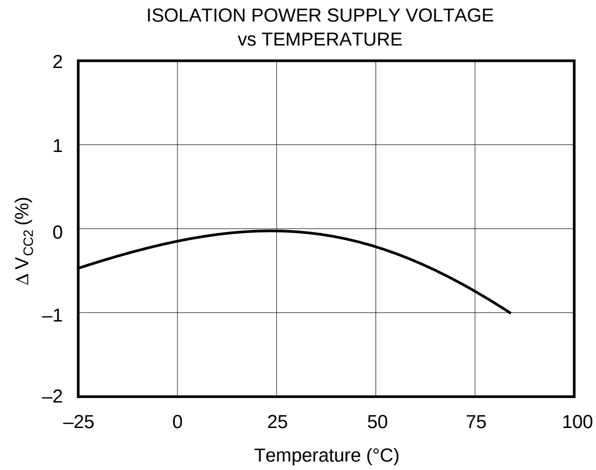


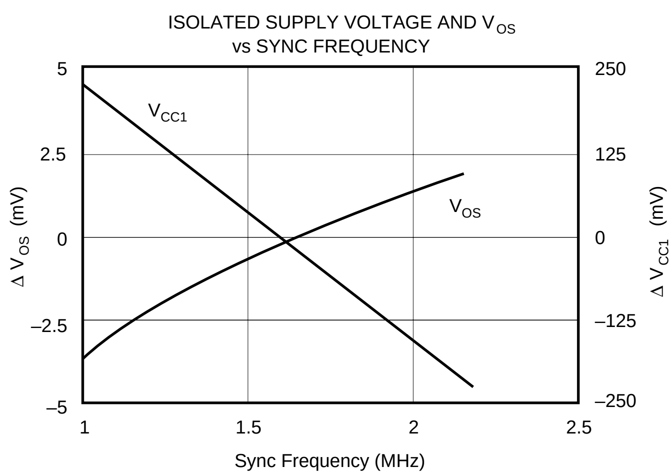


TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_{CC2} = ±15VDC$, ±15mA output current, unless otherwise noted.







THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminate beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, result in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC2}$, an option recommended if more than ±15mA are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC1}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input and output common pins and output sense are low current inputs tied to the signal source ground, output ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, Com 2 to Gnd 2, and Sense to V_{OUT} at the ISO103 socket. The enable pin may be left open if the ISO103 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.2MHz to 2MHz TTL clock signal provides synchronization of multiple units.

The ISO103 isolation amplifier contains a transformer-coupled DC/DC converter that is powered from the output side of the isolation amplifier. All power supply pins (1, 2, 3, 4, 14, and 16) of the ISO103 have an internal 0.1µF capacitor to ground. L_1 is used to slow down fast changes in the input current to the DC/DC converter. C_1 is used to help regulate the voltage ripple caused by the current demands of the converter. L_1, C_1, and C_2 are optional, however, recommended for low noise applications.

The DC/DC converter creates an unregulated ±15V output to $\pm V_{CC1}$. If the ISO103 is the only device using the DC/DC converter for power, pins 1 and 2 and pins 3 and 4 can be connected directly without C_O or L_O in the circuit. If an external capacitor is used in this configuration, it should not exceed 1µF. This configuration is possible because the isolation amplifier and the DC/DC converter are synchronized internally.

If additional devices are powered by the DC/DC converter of the ISO103, the application may require that the ripple voltage of the ISO103 converter be attenuated. In which case, L_O and C_O should be added to the circuit. The inductor is used to attenuate the ripple current and a higher value capacitor can be used to reduce the ripple voltage even further.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of ±0.5% for the values shown; greater range may be provided by increasing the size of R_1 and R_2. Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

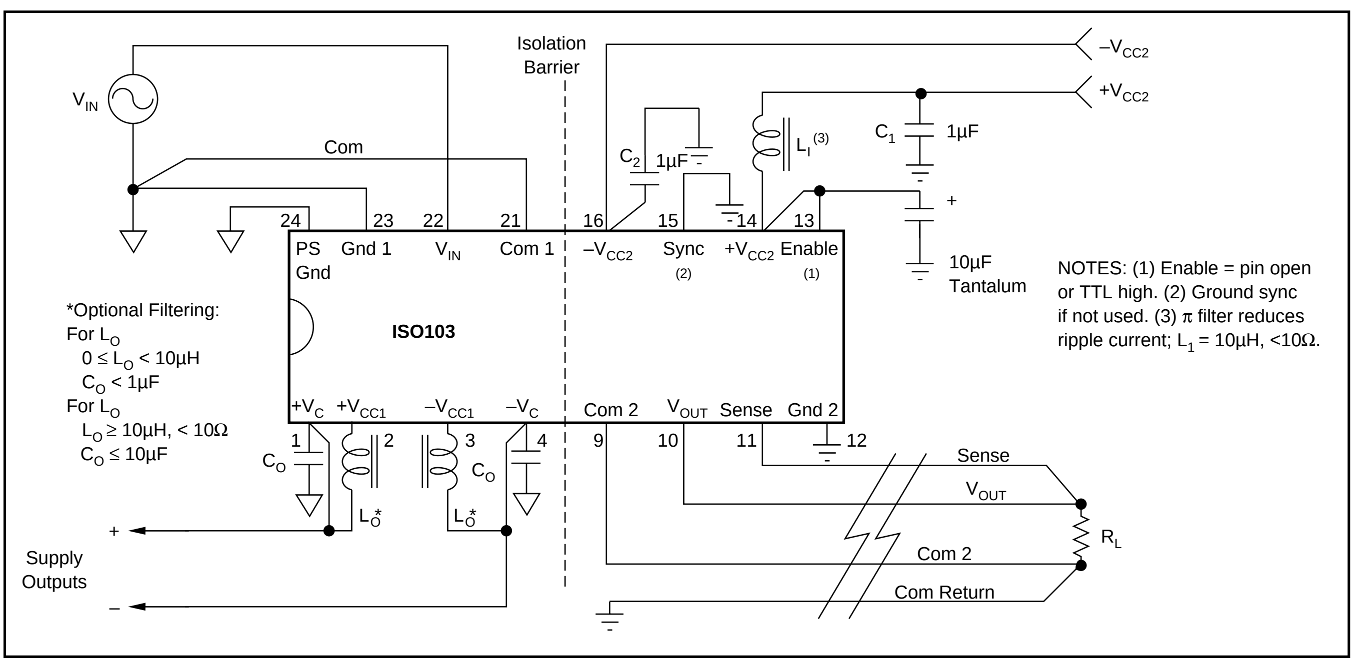


FIGURE 1. Signal and Power Connections.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input referred errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

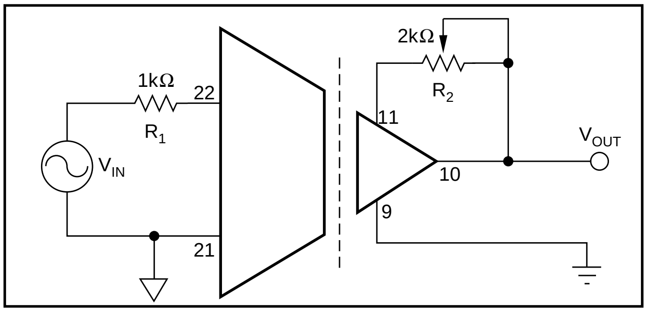


FIGURE 2a. Gain Adjust.

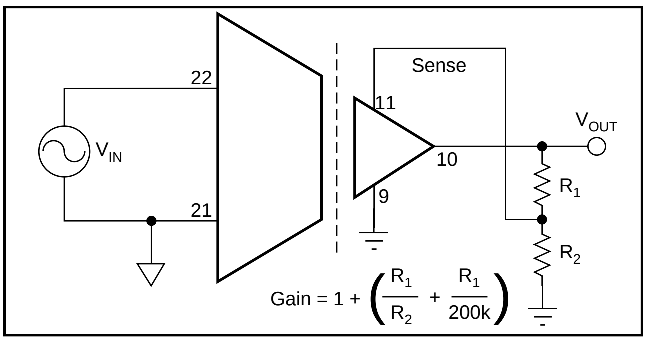


FIGURE 2b. Gain Setting.

Figure 3 shows a method for trimming V_{OS} of the ISO103. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a ±100mV trim, power supply sensitivity is 8mV/V at the output.

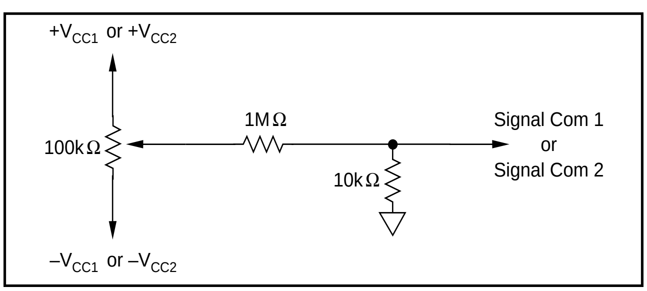


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to <5mVp-p without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

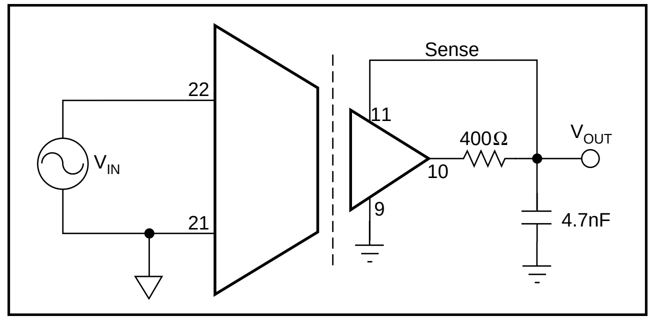


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO103s can be accomplished by connecting pin 15 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO103 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic provided the frequency is between 1.2MHz and 2MHz, and the duty cycle is greater than 25%.

Multichannel synchronization with reduced power dissipation for applications requiring less than ±15mA from V_{CC1} is accomplished by driving both the Sync input pin (15) and Enable pin (13) with the TTL oscillator as shown in Figure 5.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO103 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed 20kV/µs. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO103 was designed to reliably operate with 1500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, a 5600V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

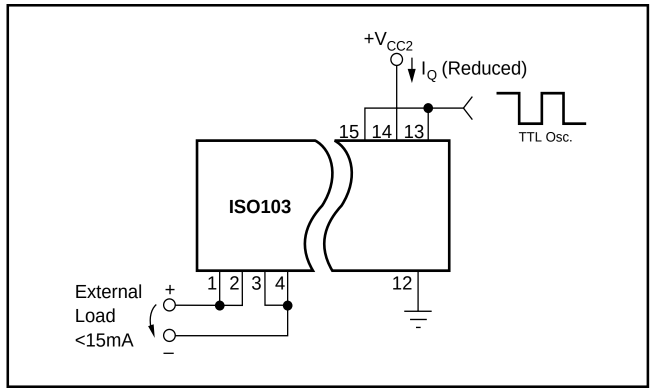


FIGURE 5. Reduced Power Dissipation.

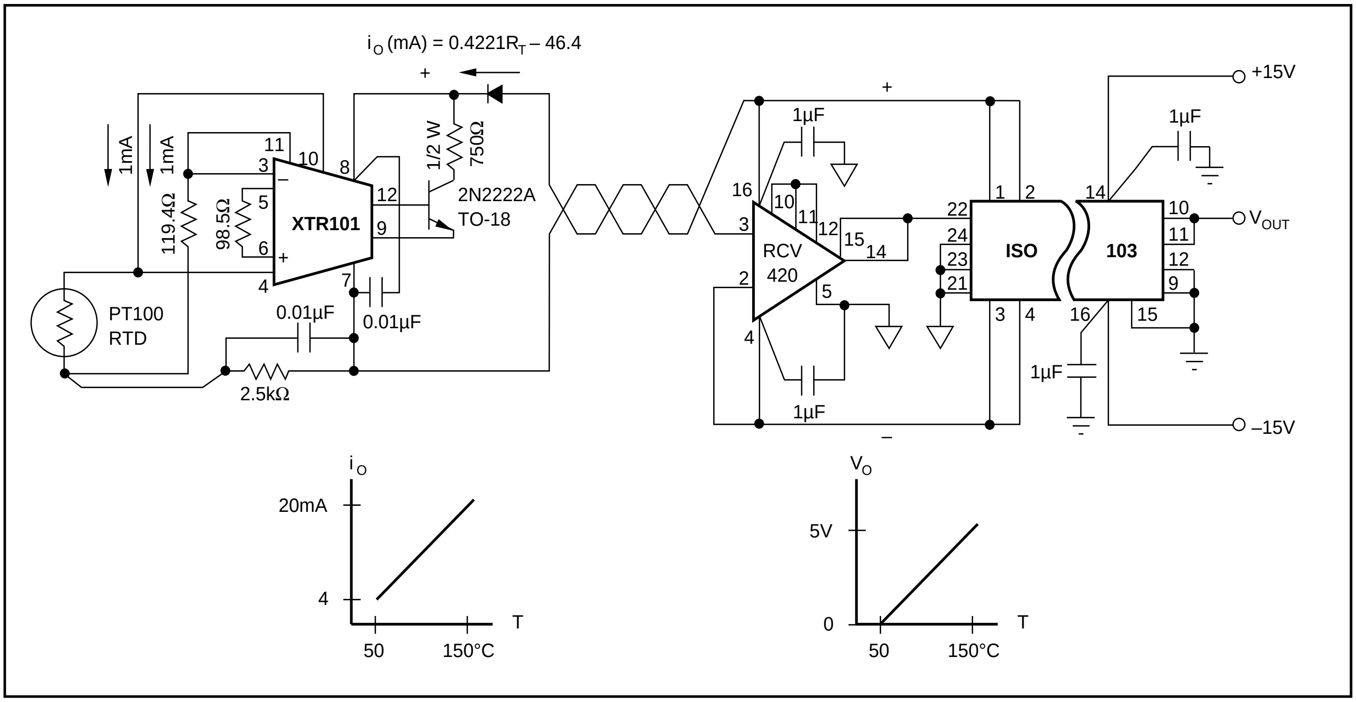


FIGURE 6. Isolated 4-20mA Instrument Loop.

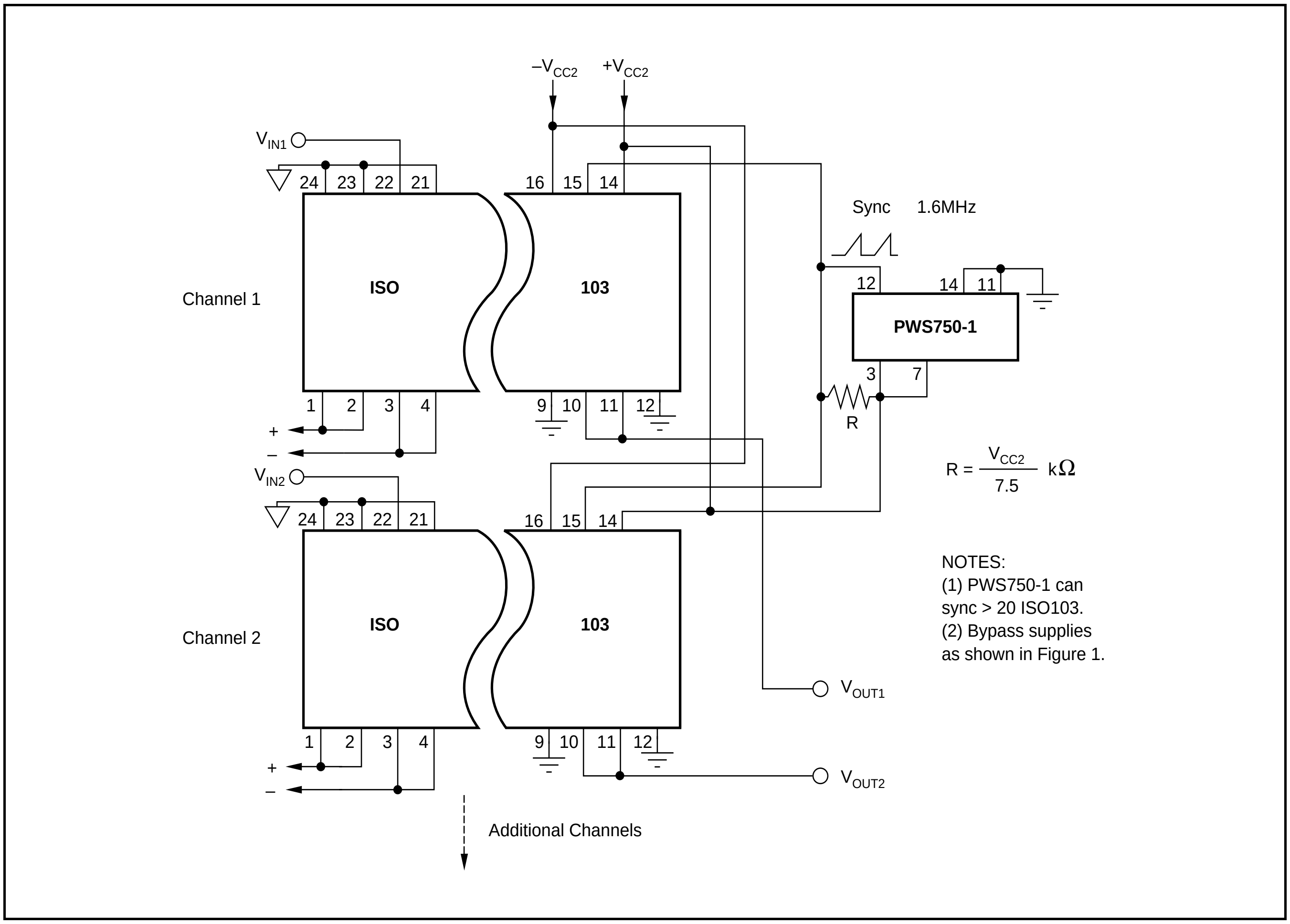


FIGURE 7. Synchronized-Multichannel Isolation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ISO103	NRND	CDIP SB	JVB	16		TBD	Call TI	Call TI
ISO103B	NRND	CDIP SB	JVB	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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