OVERVIEW

The **KS0165** wavetable synthesizer with effect processor chip represents the state-of-the-art in multimedia audio technology. The KS0165 combines a high-quality 32-voice wavetable synthesizer, a powerful 16-bit CPU, MPU-401 compatibility, effect processor & 16k delay RAM into a single chip. The audio performance of a typical KS0165 system compares favorably to the best multimedia audio solutions available today, but at a fraction of the cost. A typical KS0165 system provides 32 voices of 16-bit, 44.1 kHz sample rate wavetable synthesis and effects such as chorus and reverb, MPU-401 compatibility, General MIDI, GS and MT-32 compatibility. With KS0165, a complete wavetable synthesizer may be implemented with as few as three ICs. Both serial and parallel MIDI interfaces are provided

.

FEATURES

- **High-quality 32-voice wavetable synthesizer**
- **General MIDI compliant**
- **Internal audio effects processor & 16K Delay RAM**
- **Supports all common CDP D/A formats**
- **Supports up to 8Mbytes of sample memory**
- **Supports 8-bit, 16-bit and compressed samples**
- **Directly supports ROM, SRAM and DRAM**
- **Hardware-based Roland MPU-401 emulation**
- **16-bit embedded CPU minimizes host PC overhead**
- **Integrated SRAM for embedded CPU**
- **Integrated MIDI UART**
- **Software-controlled SLEEP mode**
- **Sequoia Pegasus synthesizer firmware**
- **100 pin QFP package**
- **Fully software configurable**
- **Comprehensive Software Developers Kit**

ORDERING INFORMATION

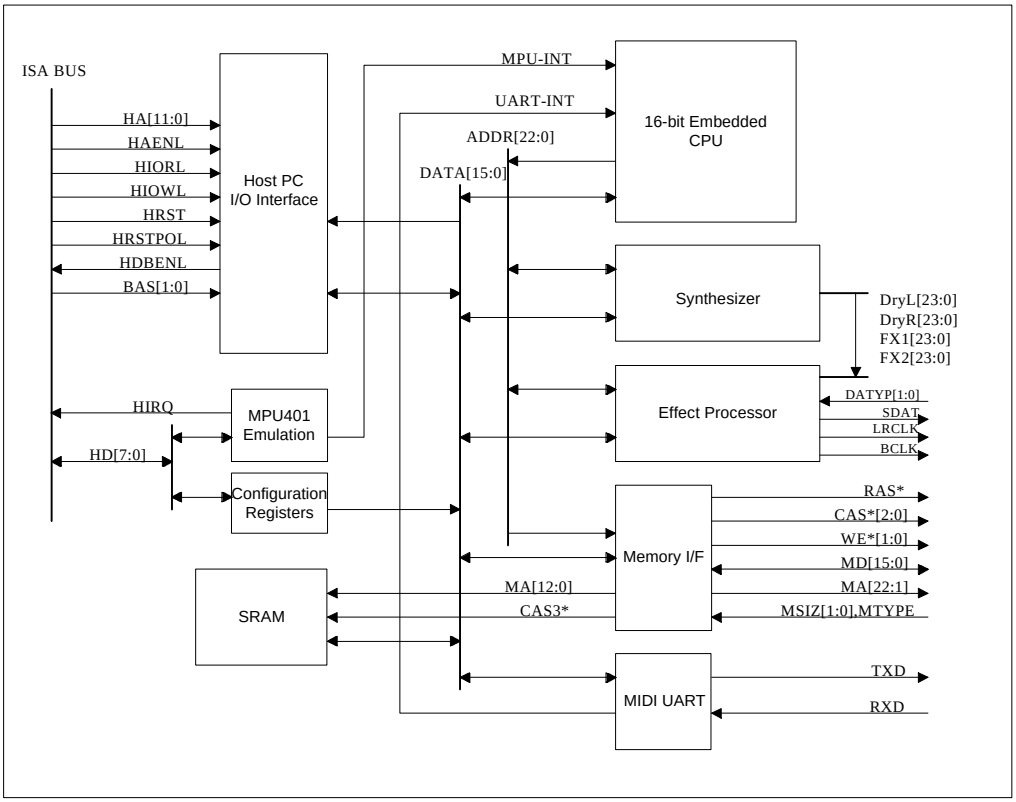
Device	Package	Temperature Range
KS0165	100-QFP	0°~+70°C

APPLICATIONS

- **MULTIMEDIA AUDIO PRODUCTS**
- **MUSICAL SYNTHESIZERS**

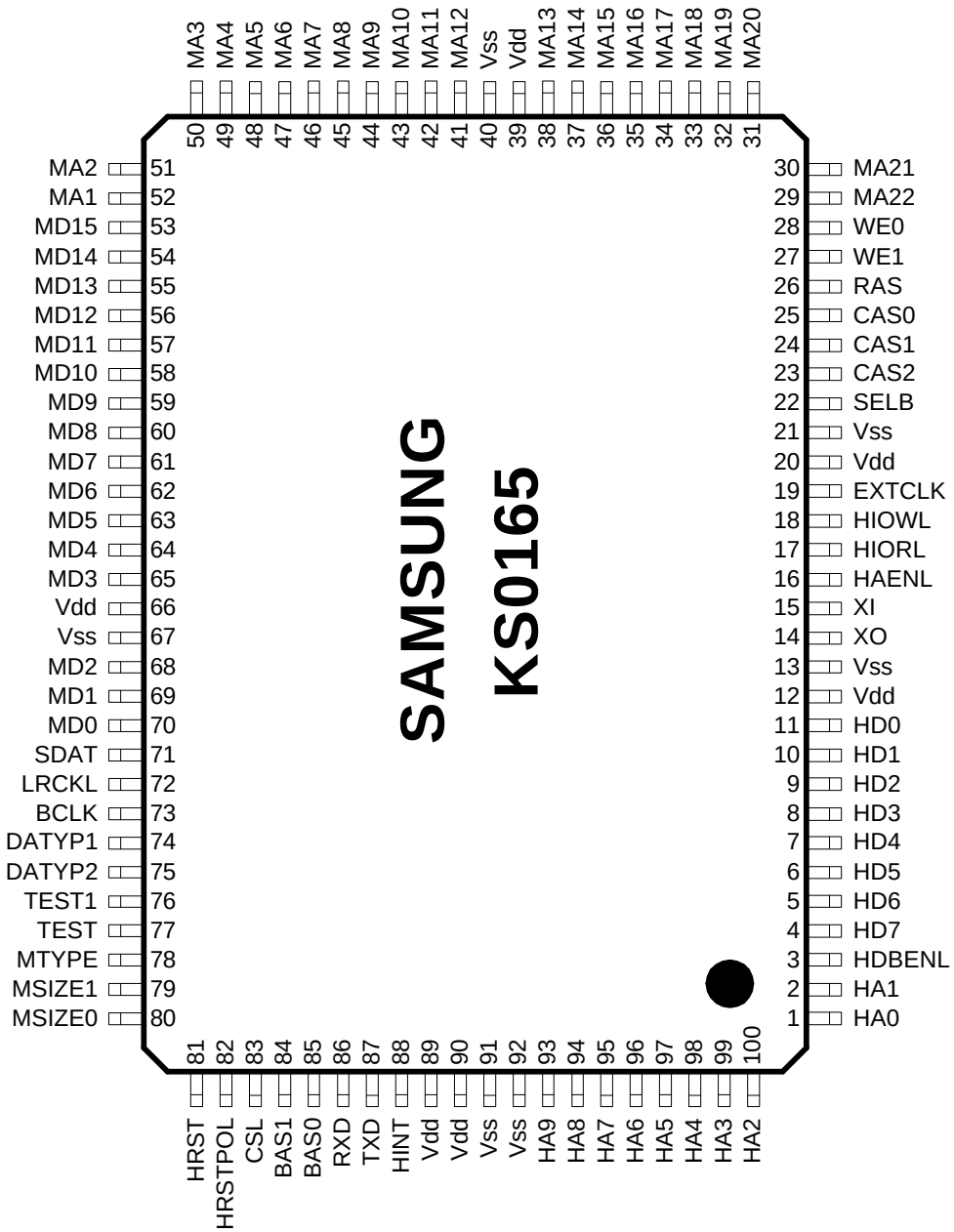
RELATED PRODUCTS

- **KS0175-1M 1MB Sample ROM**
- **KS0175-2M 2MB Sample ROM**
- **KS0175-4M 4MB Sample ROM**
- **KF353/D/S Dual Operational Amplifier**



BLOCK DIAGRAM

TYPICAL APPLICATION



PIN ASSIGNMENT- 100-QFP

PIN ASSIGNMENT(Continued)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	HA1	26	RAS	51	MA2	76	TEST1
2	HA0	27	WE1	52	MA1	77	TEST
3	HDBENL	28	WE0	53	MD15	78	MTYPE
4	HD7	29	MA22	54	MD14	79	MSIZE1
5	HD6	30	MA21	55	MD13	80	MSIZE0
6	HD5	31	MA20	56	MD12	81	HRST
7	HD4	32	MA19	57	MD11	82	HRSTPOL
8	HD3	33	MA18	58	MD10	83	CSL
9	HD2	34	MA17	59	MD9	84	BAS1
10	HD1	35	MA16	60	MD8	85	BAS0
11	HD0	36	MA15	61	MD7	86	RXD
12	VDD	37	MA14	62	MD6	87	TXD
13	VSS	38	MA13	63	MD5	88	HINT
14	XO	39	VDD	64	MD4	89	VDD
15	XI	40	VSS	65	MD3	90	VDD
16	HAENL	41	MA12	66	VDD	91	VSS
17	HIORL	42	MA11	67	VSS	92	VSS
18	HIOWL	43	MA10	68	MD2	93	HA9
19	EXTCLK	44	MA9	69	MD1	94	HA8
20	VDD	45	MA8	70	MD0	95	HA7
21	VSS	46	MA7	71	SDAT	96	HA6
22	SELB	47	MA6	72	LRCKL	97	HA5
23	CAS2	48	MA5	73	BCKL	98	HA4
24	CAS1	49	MA4	74	DATYP1	99	HA3

25	CAS0	50	MA3	75	DATYP0	100	HA2

PIN DESCRIPTION

Pin Name	*Pin #*	*Type*	*Description*
HOST PC INTERFACE			
HA[9:0]	1 - 2, 93 - 100	I	Host Address Bits 9-0. These are the low 10 bits of the Host PC address bus, which are decoded to control access the MPU-401. For IBM PC application, these pins should be connected directly to A[9-0]. Alternatively, these pins may be tied to GND, and a fully qualified chip select signal may be connected to the CSL* pin instead.
HAENL	16	I	Host Address Enable. This is the Host PC I/O enable. All I/O operations are ignored any time this signal is high. For PC applications, these pins should be connected directly to AEN*.
CSL	83	I	Chip Select. In most applications where the MPU-401 emulation is being used, the KS0164 address decoder will be used. However, if a non-standard address decode is required, or of a plug-n-play address decode is available, a fully qualified, active-low chip select signal may be connected to this pin instead. If this pin is not used, it must be pulled up to V_{DD}.
HD[7:0]	4 - 11	I/O	Buffered Host PC Data Bus Bits [0:7]. These pins have 18mA drivers, so they may be directly connected to the host PC data bus in most applications. If additional buffering is desired a 74LS245 may be used with its Enable pin connected to HDBEN*, and its DIR pin connected to HIOR*.
HIORL	17	I	Host I/O Read. This is the Host PC I/O read enable.
HIOWL	18	I	Host I/O Write. This is the Host PC I/O write strobe. Data is written to internal registers on the rising edge of this signal.
HRST	81	I	Host PC Reset. The active polarity of this pin is programmable via the HRSTPOL pin. For PC application, this pin should be connected directly to the PC-bus RSTDRV signal. For daughter card applications, connect this pin to the reset signal from the host board.
HRSTPOL	82	I	Determines the signal polarity of the HRST pin. Set this pin low to make HRST active low (typical for daughter card applications), set this pin high to make HRST active high (use for ISA bus applications).
HDBENL	3	O	Host PC Data Bus Buffer Enable. This output controls the enable to the 74LS245 which buffers the Host PC data bus. This pin is driven low any time the MPU-401 is addressed for an I/O access.
HINT	88	O	Host MPU-401 Interrupt. This is an active high interrupt output to the Host PC. It should be connected to one of the Host IRQ lines, normally IRQ2.

Pin Name	*Pin #*	*Type*	*Description*

MEMORY INTERFACE

MA[22:1]	29 - 38 41 - 52	O	Memory Address Bus Bits [22:1]. This is the external memory address bus. When accessing static memory devices (ROM/SRAM), these pins will contain a stable address throughout the entire memory cycle. When accessing dynamic memory, pins MA[11:0] will contain the multiplexed DRAM address.
MD[15:0]	53 - 70	I/O	Memory Data Bus Bit [15:0]. This is the external memory data bus.
WE1	27	O	Memory Upper Byte Write Enable. When this signal is low during an external memory access, it indicates that data bits MD[15:8] should be written to the addressed memory device.
WE0	28	O	Memory Lower Byte Write Enable. When this signal is low during an external memory access, it indicates that data bits MD[7:0] should be written to the addressed memory device.
RAS	26	O	Dynamic Memory Row Address Strobe. This signal is the Row Address Strobe for all external DRAM. When a DRAM device is addressed, this signal will be driven low shortly after the row address has been placed on MA0-11. It will also be driven low during ROM/SRAM cycles to provide CAS-before-RAS refresh for any DRAM devices in the system.
CAS2-0	23 - 25	O	Dynamic Memory Column Address Strobes/Static Memory Chip Selects [2:0]. When a DRAM device is addressed, one of these signals will be driven low shortly after the column address has been placed on MA[11:0]. It will also be driven low during ROM/SRAM cycles to provide CAS-before-RAS refresh for any DRAM devices in the system. When a ROM or SRAM device is addressed, one of these signals will be driven low shortly after the address has been placed on MA[22:0].
MTYPE	78	I	Memory Type Select. When this pin is tied to GND, the optional memory device(s) connected to CAS1 and/or CAS2 are configured as static(ROM or SRAM) devices. When this pin is pulled up to V_{DD}, the optional memory device(s) connected to CAS1 and/or CAS2 are configured as dynamic (DRAM) devices.
MSIZE[1:0]	79,80	I	Dynamic Memory Size Select. When optional dynamic memory is connected to CAS1 and/or CAS2, these pins configure the size of the DRAM devices so that proper address multiplexing can be performed by the KS0164. The size is configured as follows: MSIZE1 MSIZE0 DRAM Size 0 0 64K 0 1 256K 1 0 1M 1 1 4M

Pin Name	*Pin #*	*Type*	*Description*

D/A & EFFECTS PROCESSOR INTERFACE

SDAT	71	O	D/A Converter Serial Data . These are the serial data outputs from the effect processor. SDAT would be connected to the data input of an external 16-bit stereo serial D/A converter.
BCLK	73	O	D/A Converter Bit Clock. This is the bit clock for the external serial D/A converter for the synthesizer.
LRCLK	72	O	D/A Converter L/R Clock. This is the L/R clock for the external serial D/A converter for the synthesizer.
DATYPE[1:0]	74, 75	I	D/A Converter Serial Data Format Select. These signals selects the data format of the D/A devices as follows: DATYPE1 DATYPE0 D/A Data Format 0 0 20bit I2S 0 1 16bit Right-Justified 1 0 20bit Left-Justified 1 1 20bit Right-Justified

CLOCK INPUT

XI	15	I	16.9344 MHz Oscillator Buffer Input. This input will normally be connected to one side of a 16.9344MHz crystal, with a 20pF capacitor to ground. If desired, an externally generated 16.9344MHz clock may be connected to this pin instead. Note that due to internal analog circuitry, the chip may not behave reliably if this clock input is not close to the design frequency.
XO	14	O	16.9344 MHz Oscillator Buffer Out. This input will normally be connected to one side of a 16.9344MHz crystal, with a 20pF capacitor to ground. If the OSCI pin is being driven by an externally generated clock, this pin should be left unconnected.

POWER AND GROUND

VDD	12, 20, 39,66, 89,90	+5V	Digital power supply.
VSS	13, 21, 40, 67, 91,92	GND	Digital ground.

Pin Name	*Pin #*	*Type*	*Description*

MISCELLANEOUS

RXD	86	I	MIDI Receive Data. This is the TTL-level serial input to the 31.25 kBAUD MIDI UART. For normal MIDI communication, this pin must be driven by an external opto-isolator from the current-loop MIDI line.
TXD	87	O	TTL MIDI Transmit Data. This is the TTL-level serial output from the 31.25 kBAUD MIDI UART. For normal MIDI communication, this pin must drive an external voltage-to-current converter to drive the current-loop MIDI line.
BAS[1:0]	84, 85	I	MPU-401 Base Address Select [1:0]. These pins select whether the MPU-401 emulation will be decoded at address 320H, 330H, 340H, or 350H. BAS1 BAS0 ADDRESS 0 0 320H 0 1 330H 1 0 340H 1 1 350H
EXTCLK	19	I	TEST Pin - Manufacturing Test Pin. For normal operation, this pin must be tied to GND. Applying power to the device with this pin floating or tied to a logic high level may cause permanent damage to the device.
TEST	77	I	TEST Pin - Manufacturing Test Pin. For normal operation, this pin must be tied to GND. Applying power to the device with this pin floating or tied to a logic high level may cause permanent damage to the device.
TEST1	76	I	TEST Pin - Manufacturing Test Pin. For normal operation, this pin must be tied to GND. Applying power to the device with this pin floating or tied to a logic high level may cause permanent damage to the device.
SELB	22	I	TEST Pin - Manufacturing Test Pin. For normal operation, this pin must be tied to GND. Applying power to the device with this pin floating or tied to a logic high level may cause permanent damage to the device.

GENERAL DESCRIPTION

The **KS0165** is a highly integrated wavetable synthesizer chip, designed to be part of high-performance, low-cost multimedia audio systems. The chip contains a complete 32-voice, 16-bit, 44.1kHz wavetable synthesizer with effect processor, a high-performance 16-bit CPU, compatibility with established standard audio interfaces, and all necessary system glue logic. With its on-chip CPU, an KS0165-based synthesizer imposes absolutely minimal host CPU overhead. Its hardware-based MPU-401 emulation completely eliminates the memory overhead, software compatibility, and stability problems of TSR-based emulations. The following sections give a brief description of the major functional blocks of the KS0165.

HOST PC INTERFACE

All necessary ISA bus interface logic is completely contained on-chip. This includes address decoding for the MPU-401 emulation, control signal interpretation, and optional data bus buffer control. All PC interface control logic operates completely asynchronously to the synthesizer/CPU logic. Standard interfacing techniques are used to provide a highly compatible and reliable interface.

The MPU-401 emulation can be decoded for any one of four standard address ranges, as selected by the BAS[1:0] pins. In addition, a serial MIDI interface may be used, leaving the MPU-401 emulation inactive. This mode is particularly useful for stand-alone synthesizer modules and WaveBlaster-type daughter board applications.

To better support non-PC-based applications, including stand-alone applications where no host CPU is available, the reset signal polarity is programmable via the HRSTPOL pin, to accommodate existing active high or active low reset signals.

MPU-401 INTERFACE

The primary interface for communicating MIDI data to/from the KS0165 is the on-chip MPU-401 emulation. This emulation provides the full hardware functionality and partial software functionality of a real MPU-401. MPU-401 UART mode is fully supported, while a subset of the "intelligent" mode commands are also supported. The intelligent mode support currently provided is adequate to support virtually all existing MPU-401 applications. All hardware necessary to support full intelligent mode is present, allowing more complete intelligent mode software support to be added in the future if it become necessary. The MPU-401 interface is used for communicating MIDI and command data between the PC and the on-board synthesizer, the PC and external devices connected to the on-board MIDI interface available through the joy stick connector on the card bracket. Normally, the MIDI UART under the control of the embedded CPU, so that it can provide FIFO buffering of MIDI data. However, the UART transmitter can also be directly connected to the MPU-401 emulation. This allows UART mode data transfers from the PC to external MIDI devices to take place with no intervention on the part of the CPU, although the CPU will still intercept and process MPU-401 command data and UART receive data. It is also possible for the on-board synthesizer to directly process MIDI data from external sources, if desired. Unlike a real MPU-401, the emulation provides the optional capability of generating transmit interrupts to the PC for enhanced performance.

MIDI UART NTERFACE

The second of available interfaces for communicating MIDI data to/from the KS0165 is the on-chip of MIDI UART. This interface is always active, and works independently from the MPU-401 emulation, allowing the KS0165 to easily be used in stand-alone MIDI modules and WaveBlaster-type daughter board applications.

EMBEDDED CPU

In sharp contrast to many other low-cost multimedia audio solutions currently available, the KS0164 does not rely on the host PC processor or a slow external micro controller to drive the wavetable synthesizer. Rather, the KS0164 contains a high-performance custom-built 16-bit CPU incorporating such advanced features as six different addressing modes, a hardware multiplier, a barrel shifter, and a peak execution rate of nearly 3 million instructions per second. In addition to providing optimal synthesizer audio quality, this reduces host PC CPU overhead and the resulting degradation of application/game performance. The considerable

memory overhead, compatibility problems, and erratic audio quality associated with TSR-based solutions are also completely eliminated. In addition to handling the myriad chorus associated with operating the wave table synthesizer, the embedded CPU is also responsible for performing much of the work of MPU-401 emulation. Unlike a purely hardware-based solution, this makes possible future software updates to support additional functionality, such as full MPU-401 intelligent mode support.

SYNTHESIZER

The synthesizer extends and improves upon the functionality of the KS0164. The basic function remains unchanged. but the following areas are changed. The KS0164 digital filter worked quite well, but at very low cutoff frequencies cutoff coefficient is sensitive. At very low cutoff frequency, a single-bit change in the coefficient created audible artifacts. this made low-frequency filter sweeps all but impossible. In Filter calculation datapath was very easy to generate arithmetic overflow. This makes unpleasant audio effects. To correct this, the internal datapath have been expanded to 18 bits. Because the KS0165 has a internal effect processor, it provide a proper interface with Effect processor. The specification for the synthesizer are follows:

Architecture : Digital Wavetable Synthesizer
Voices : 32
Polyphony : 32 Note Maximum
Multi timbral Capability
: Up to 16 Parts
Sample Memory
: Up to 16 MWords of
ROM/SRAM/DRAM
Available Sample Sets
: 1M*16bits, 512*16bits
D/A converter
: 16bit Linear Serial Converter,
All Common Data Formats Supported
Sample Playback Rate
: Fixed @ 44.1kHz
Level & Panning Controls
: Separate 16bit L&R Volume Control for
Each voice
Filters : 2 Separate 2 pole Resonant Digital filter
for each voice
Data Formats
: 8/16-bit signed linear or 8/12-bit
compressed
Envelopes : Hardware Envelopes for amplitude
and filters
Effects : Reverb, Chorus(Down load Effect
algorithm)
Firmware : Sequoia Development Group Pegasus
Compatibility
: Roland MT-322 Sound set Compatible
Customized Sound Sets available

EFFECT PROCESSOR & DELAY RAM

KS0165 provides effects sound to D/A by embedded effects synthesizer. Effects algorithm is downloaded by host CPU from external MASK ROM. It generates reverb, chorus and other effects. KS0165 does not need any external SRAM & Delay RAM which are used by buffer and effect delay ram.

GENERAL DESCRIPTION(Continued)

The specifications for the synthesizer are as follows:

Architecture	Digital Wavetable Synthesizer
Voices	32
Polyphony	32 Notes Maximum
Multi-Timbral Capability	Up To 16 Parts
Sample Memory	Up To 24 Mbytes of ROM/SRAM/DRAM
Available Sample Sets	2Mx16-bits, 1Mx16-bits, 512Kx16-bits
D/A Converter	16-Bit Linear Serial Converter, All Common Data Formats Supported
Sample Playback Rate	Fixed @ 44.1 kHz
Level And Panning Controls	Separate 16-Bit L&R Volume Controls For Each Voice
Filters	2 Separate 2-Pole Resonant Digital Filters For Each Voice
Data Formats	8- Or 16-Bit Signed Linear Or 8- Or 12-Bit Compressed
Envelopes	Hardware Envelopes For Amplitude and Filters
Effects	Effects Loop Provided For DSP Multiple Effects Processor
Firmware	Sequoia Development Group Pegasus Synthesizer Firmware
Compatibility	Fully General-MIDI Compliant Roland MT-32 Sound Set Compatible

SYSTEM TIMING AND CONTROL

All timing is derived from a 16.9344 MHz crystal oscillator, or an externally generated oscillator of any frequency up to 33Mhz. However, note that the internal MIDI UART baud rate is directly proportional to the system clock rate. At any crystal frequency other than 16.9344 MHz, the UART BAUD rate will not be correct.

SAMPLE MEMORY INTERFACE

Each memory access cycle consists of 3 cycles of the 16.9344 MHz master clock, or 177.15 nsec. This is adequate to allow use of 150 nsec ROM, and 80 nsec DRAM. The memory interface supports a minimum of one and a maximum of three memory devices. The device connected to CAS0 must be a ROM. In general the CPU will execute entirely out of this ROM, and most, if not all, synthesizer voices will also be playing primarily from this ROM, although entirely RAM-based systems can be supported with some additional logic. ROM memory accesses are exploited to allow DRAM refresh to occur simultaneously with ROM accesses by executing CAS-before-RAS refresh cycles on all DRAM banks in parallel with all ROM/SRAM accesses. For systems with ROM-based samples, this scheme provides adequate refresh for all DRAM in the system. For a totally DRAM-based system, it is necessary to allocate one synthesizer voice to perform DRAM refresh. For a combined ROM/DRAM system, as long as at least two voices are playing samples from ROM at all times, adequate refresh will be provided automatically, otherwise one voice must be dedicated to providing DRAM refresh.

REGISTER DESCRIPTION

DIRECT-ADDRESSED REGISTERS

MPU-401 DATA REGISTER **READ/WRITE**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+0	HMAD	D7	D6	D5	D4	D3	D2	D1	D0

D[7:0]	MPU-401 data.

MPU-401 COMMAND REGISTER **WRITE ONLY**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+1	HMAC	C7	C6	C5	C4	C3	C2	C1	C0

C[7:0]	MPU-401 command.

MPU-401 STATUS REGISTER **READ ONLY**

ADDRESS	MNEMONIC	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BASE+1	HMAC	RXRDY	TXRDY	1	1	1	1	1	1

RXRDY	Received Data Ready Status 0 = Received data is available in HMAD 1 = Received data is not available
TXRDY	Transmit Data Buffer Ready Status 0 = MPU-401 is ready to receive next data/command in HMAD or HMAC 1 = MPU-401 is not ready to receive next data/command

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Supply Voltage (Measured To V_{ss})	V_{DD}	-0.5	+7.0	V
Input Voltage (Any Pin)	V_{IN}	V_{SS} -0.5	V_{DD}+0.5	V
Ambient Operating Temperature Range	T_{opr}	0	+70	°C
Storage Temperature Range	T_{stg}	-55	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage (Measured To GND)	V_{DD}	4.75	5.0	+5.25	V
Digital Input High Voltage	V_{IH}	2.2	-	V_{DD}+0.3	V
Digital Input Low Voltage	V_{IL}	V_{SS}-0.3	-	0.8	V
Digital Output High Voltage (I_{OH}=400μA)	V_{OH}	2.4	-	-	V
Digital Output Low Voltage (I_{OL}=3.2mA)	V_{OL}	-	-	0.45	V
Input Leakage High Current	I_{IH}	-10	0	10	μA
Input Leakage Low Current*	I_{IL}	-10	0	10	μA
Supply Current	I_{CC}	-	100	250	mA
Pull-up Resistance**	R_{UP}	40	-	250	kΩ

Test Condition : V_{DD}=5.0V, V_{SS}=0V, f_{osc}=16.9344MHz, T_a=25°C.

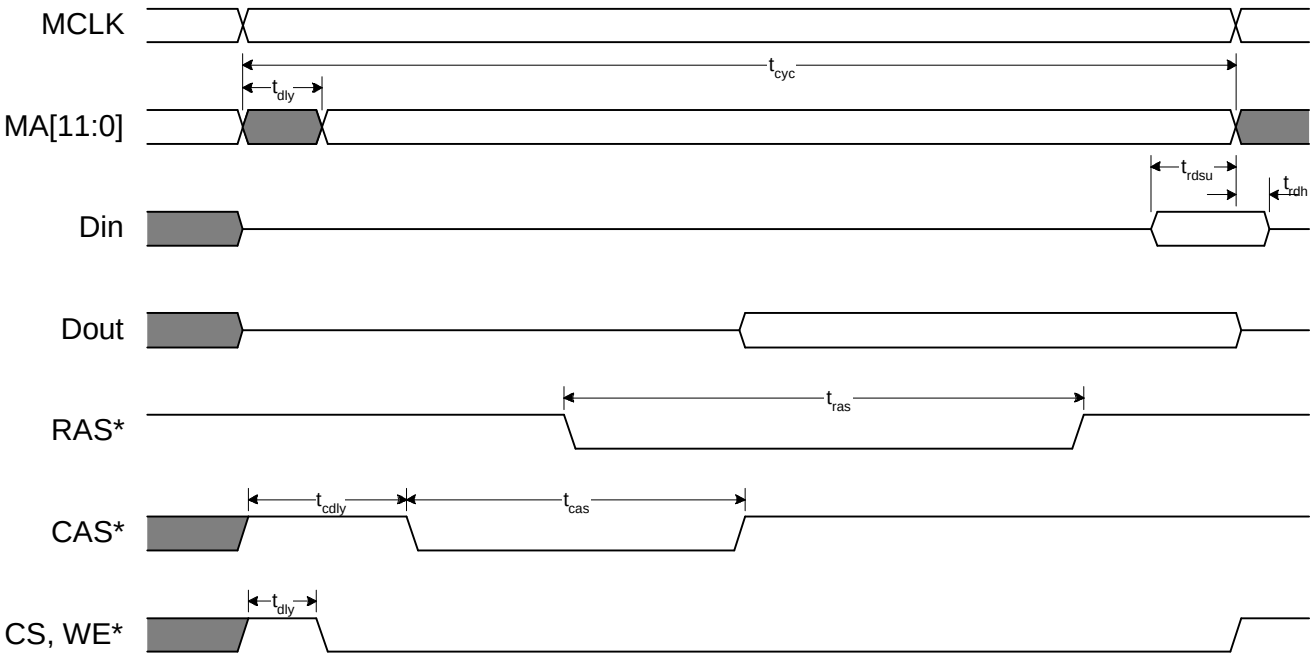
* For pins TEST, TEST1,MTYPE, MSIZ1-0, BAS1-0, HRSTPOL, HRST, DATYPE1-0 and CSL.

** All input pins except ones in *.

ELECTRICAL SPECIFICATION(Continued)

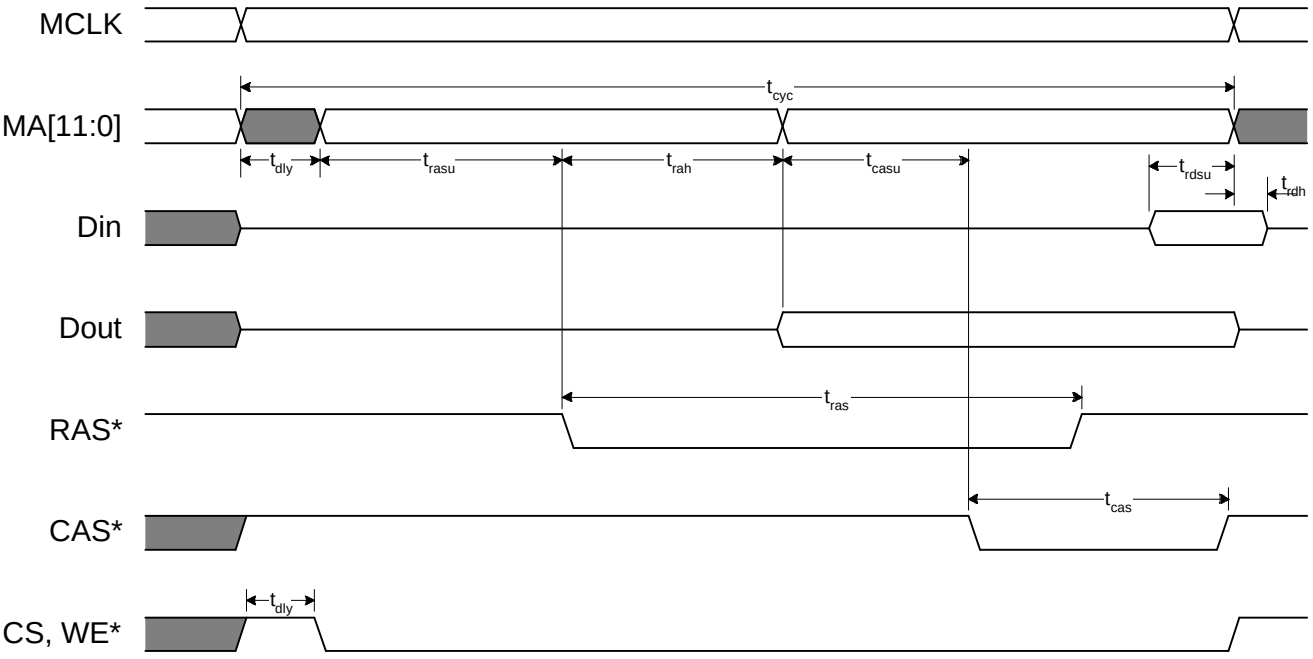
AC ELECTRICAL CHARACTERISTICS

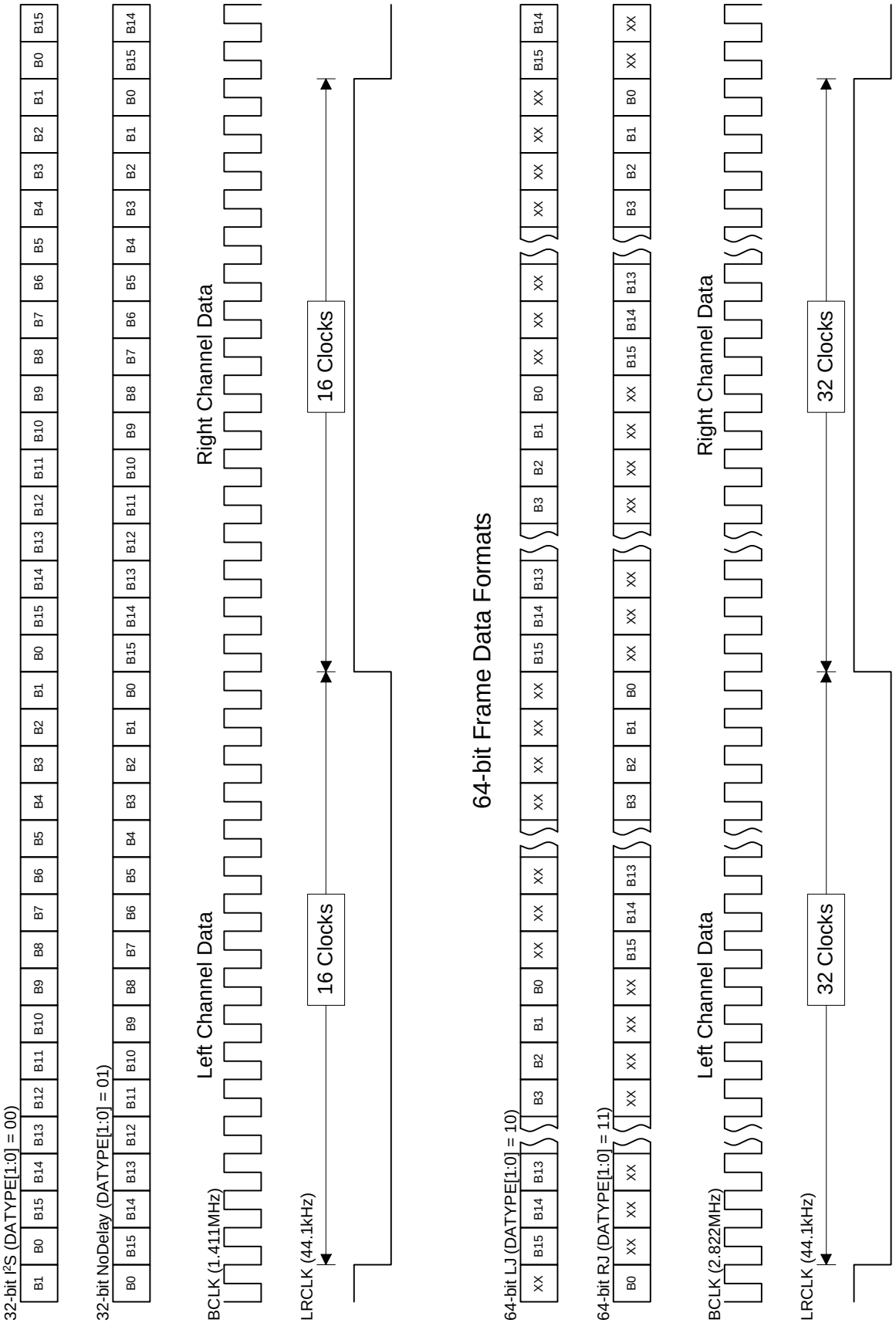
CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Memory Cycle Time	t_{cyc}	-	177	-	nsec
Memory Address/Control Delay	t_{dly}	-	15	-	nsec
Memory Read Data Setup Time	t_{rdsu}	15	-	-	nsec
Memory Read Data Hold Time	t_{rdh}	0	-	-	nsec
RAS* Active Time	t_{ras}	-	88	-	nsec
CAS* Active Delay Time	t_{cdly}	-	29	-	nsec
CAS* Active Time	t_{cas}	-	59	-	nsec
Row Address Setup Time	t_{rasu}	-	44	-	nsec
Row Address Hold Time	t_{rah}	-	29	-	nsec
Column Address Setup Time	t_{casu}	-	29	-	nsec
Oscillator Frequency	f_{osc}	-	-	16.9344	MHz



ROM/SRAM MEMORY INTERFACE TIMING

DRAM MEMORY INTERFACE TIMING




32-bit Frame Data Formats
32-bit I²S (DATYPE[1:0] = 00)
B1 B0 B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 B15
32-bit NoDelay (DATYPE[1:0] = 01)
B0 B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 B15 B14
Left Channel Data
Right Channel Data
BCLK (1.411MHz)
LRCLK (44.1kHz)
16 Clocks
16 Clocks
64-bit Frame Data Formats
64-bit LJ (DATYPE[1:0] = 10)
XX B15 B14 B13 B3 B2 B1 B0 XX XX XX XX XX XX B15 B14 B13 B3 B2 B1 B0 XX XX XX XX XX XX B15 B14
64-bit RJ (DATYPE[1:0] = 11)
B0 XX XX XX XX XX XX B15 B14 B13 B3 B2 B1 B0 XX XX XX XX XX XX B15 B14 B13 XX XX XX XX XX XX B15 B14 B13 B3 B2 B1 B0 XX XX
Left Channel Data
Right Channel Data
BCLK (2.822MHz)
LRCLK (44.1kHz)
32 Clocks
32 Clocks

Audio Board Design & PCB Layout Guidelines

Overview

Proper analog circuit design and PCB layout are essential to achieving optimum audio performance, as well as acceptable EMI (FCC/VDE) characteristics from PC audio boards. This document outlines the basic guidelines that should be followed to ensure acceptable performance in these critical areas. As a reference, please refer to the evaluation board schematics and PCB layout.

Design Overview

In order to achieve optimum audio performance, in terms of signal-to-noise ratio, noise, floor, and distortion, always provide separate analog and digital supplies and grounds. All digital components should be connected to VCC and GND, directly from the PC bus connectors. Single-ended analog circuitry, such as D/A converters, CODECs, etc., should be operated from a separate +5V supply which is locally regulated down from the +12V supply available on the PC bus. All operational amplifiers should be powered by filtered ±12V supplies derived from the ±12V supplies available on the PC bus. Operational amplifiers should ***never*** be operated from a single-ended supply. This will not only reduce the dynamic range and headroom, but also significantly degrade the signal-to-noise ratio.

Handling Grounds

For optimum audio performance, it would be most desirable to keep the analog and digital supplies and returns totally isolated from one another. However, for the sake of EMI (FCC) performance, it is generally necessary to keep all supplies closely coupled. Also, in a PC, there are a limited number of supplies to work from, and only a single GND. These conflicting requirements are best met by allowing the digital and analog returns (GND & AGND) to be directly connected at only a single location, preferably directly adjacent to the card bracket. This single connection should be a substantial one, at least 100-200 mils. This connection is indicated in the Evaluation Board Schematics as a GNDSTRAP component. AC coupling the returns by means of 1-10nF capacitors straddling the perimeter of the AGND /GND planes, at intervals of no more than 1-1.5″, should provide the coupling necessary to prevent EMI problems which can be caused by the separate ground planes. The DB-15 connector shell must be securely connected to the GND plane, and the connector must be securely screwed to the bottom of the bracket, while the top of the bracket should have a tab which is securely screwed of riveted to the AGND plane, thus referencing all outgoing signal lines to the (relatively) clean chassis ground at the bracket. In past designs, these techniques have consistently resulted in a > 10dB margin relative to the FCC Class-B limits.

In the analog section, it is desirable to have two AGND planes, rather than a single AGND plane, and a single power plane. All analog supplies can be easily routed as normal traces, since the currents are very low. If possible, place the AGND planes on the outer layer, and do all signal and power routing on the two inner layers, to minimize noise pickup from adjacent boards. In SMT designs, make layers 2 & 4 AGND planes, and place as much routing as possible on layer 3, minimizing exposed routing on layer 1.

The AGND plane should completely underlie **all** analog circuitry, including and D/A or A/D converters or CODECs. There should be **no** VCC or GND routing, or unnecessary digital signal routing through the area covered by the AGND plane.

Analog Signal Routing

Proper component is essential to getting optimum audio performance. All traces should be kept as short and straight as possible. Avoid running traces parallel to other traces for other than very short distances. Keep any digital or clock traces as far as possible from A/D and D/A converters.

To minimize noise pickup, all routing to op-amp inputs should be kept as short as possible. Op-amp output signals are far less critical, being driven by a relatively low impedance source. Avoid routing op-amp input and output signals near each other to prevent feedback problems. Also, be sure to follow the supply bypassing guidelines below. never route an analog signal through a digital area, or vice-versa.

Audio Board Design & PCB Layout Guidelines(Continued)

Digital Signal Routing

Use of vias should be minimized, particularly on high speed signals, such as clocks. For this reason, hand-routing is **strongly** recommended, rather than using an auto-router. Even the auto-routers available today will use far more vias than an experienced hand-router. Our evaluation boards are all completely hand-routed. Keep all unbuffered PC-bus signals as short as possible, preferably no more than 1-2″. Also rigorously avoid passing digital signals over any splits in the planes. Keep all crystals as close as possible to the other components to which they are connected, and, if possible, surround their traces with GND traces. **Never** allow an oscillator or clock signal to cross the GND/AGND plane split! Securely attach, by soldering, the crystal case to its associated ground plane, usually GND.

Supply Bypassing

In the digital section of the board, be sure no VCC pin is more than about 1″ from a bypass capacitor. In the analog section, this may be relaxed somewhat, but try to ensure that each supply pin is within at least 1.5-2″ of a bypass capacitor. In both the digital and analog sections, evenly distribute the bypass capacitors, and use an even mix of 0.1μF and 0.001μF capacitors. For the KS0165, one bypass capacitor for each VCC pin is recommended. All bypass capacitors should be routed such that the connection is from the VCC and GND planes to the capacitor, and then from the capacitor to the IC pins.

EMI Suppression

Adequate EMI suppression can most easily be achieved through careful PCB layout, and the use of small capacitors to GND/AGND, rather than ferrite beads. Since the analog input and output signal points are all (relatively) low impedance, small capacitors(1-10nF) can be connected between these points and AGND with no appreciable effect on audio performance. All such capacitors should be places as close as possible to the connectors, and the traces leaving them (going to the connectors) should not pass near any unfiltered traces which might couple-in unwanted high-frequency noise.

PACKAGE DIMENSIONS (100-QFP-1420C)