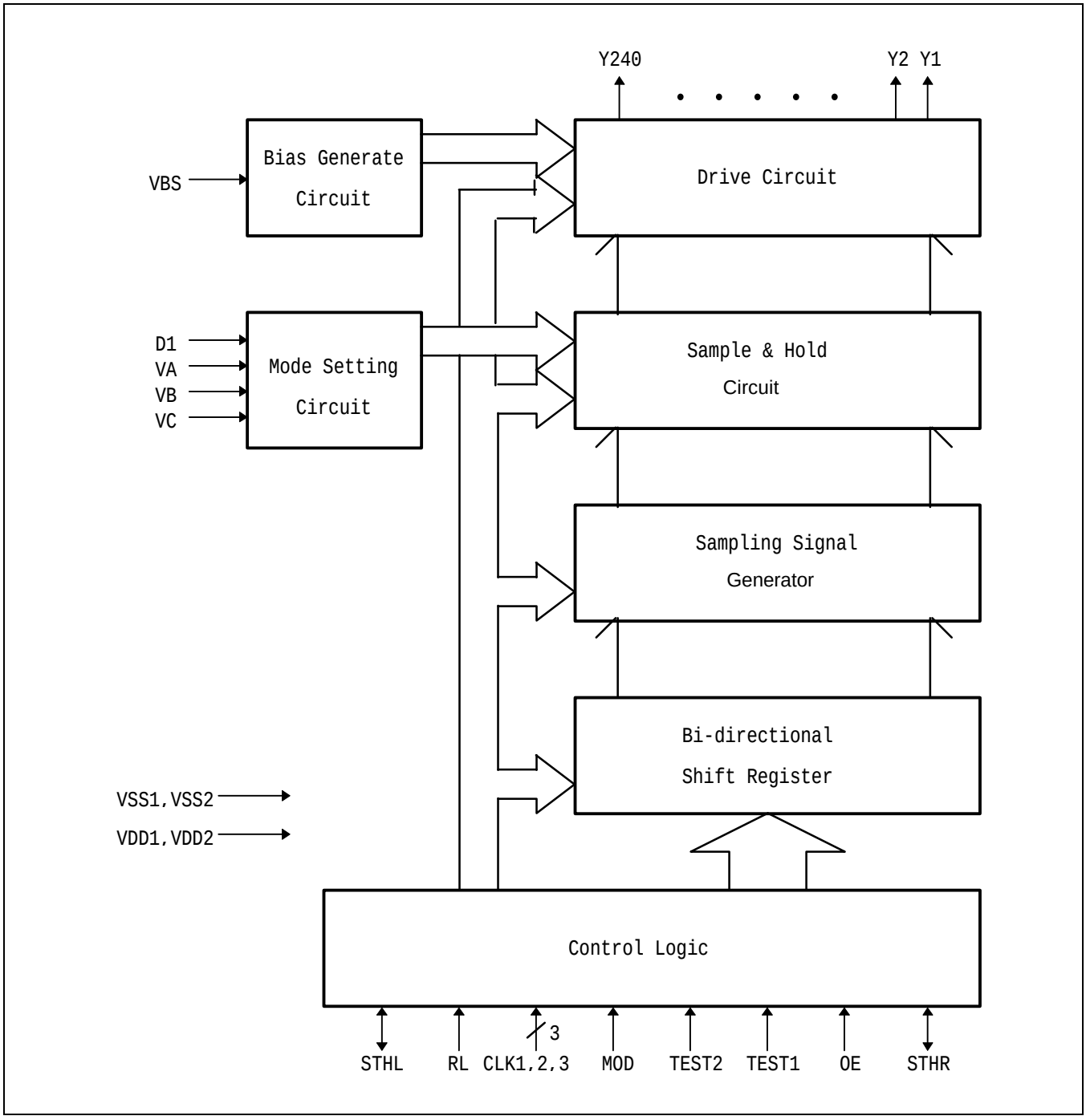
INTRODUCTION

The KS0608 is a source driver for the TFT liquid crystal panel used for LCD unit such as a pocket sized TV set, CNS, Viewcam etc. and has 240 LCD driver outputs.

FEATURES

- ❏ Active matrix LCD source driver
- ❏ No. of LCD drive outputs: 240 outputs
- ❏ Logic supply Voltage: 2.7V to 5.5V
- ❏ Driver supply Voltage: 3.0V to 5.5V
- ❏ Output dynamic range: 4.8Vp-p (at 5V Drive supply Voltage)
- ❏ Operating frequency: 10MHz (Max)
- ❏ Output deviation: ±15mV (Typ)
- ❏ Video signal setting: Compatible to stripe and delta pixel array panels by mode setting circuit.
- ❏ Video signal sampling: Possible to switch the output shift direction (Y1 → Y240 ⇔ Y240 → Y1)
- ❏ Possible to use 3-point sequential sampling by CLK1, CLK2, and CLK3
- ❏ Possible to connect Serial cascade
- ❏ After data loading. Clock stop automatically.
- ❏ COG (Chip On Glass)

BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Name	Description
V_{DD1}	Logic power	2.7V to 5.5V
V_{DD2}	Drive power	3.0V to 5.5V Set so that $V_{DD1} \leftarrow V_{DD2}$
V_{SS1}	Logic ground	Ground (0V)
V_{SS2}	Drive ground	Ground (0V)
Y1 to Y240	LCD drive output	Output pin output the voltage corresponding to the video signal held in the Sample and Hold circuit
VA, VB, VC	Video signal input	Video signal input pin
D1	Video signal changing input	Set the video signal that is sampled in the Sample and Hold circuit samples in VA, VB, VC order and VC. VA, VB order when it is L and H, respectively.
STHR	Left shift start pulse input/output	RL=H: Start pulse input pin RL=L: Start pulse output pin
STHL	Right shift start pulse input/output	RL=H: Start pulse output pin RL=L: Start pulse input pin
RL	Shift direction Select pin	Select pin for switching the video signal sampling order STHR/STHL input/output. Samples video signals in Y1 → Y240 order when it is H. Samples video signals in Y240 → Y1 order when it is L.
CLK1 to 3	Shift clock input	The video signal is sampled in order at CLKs rising edge. CLK1 RL= H : Y1,Y4,Y7 ..... Y238 RL= L : Y3,Y6,Y9 ..... Y240 : Y2,Y5,Y8 ..... Y239 CLK2: RL= H : Y3,Y6,Y9 ..... Y240 CLK3 RL= L : Y1,Y4,Y7 ..... Y238
OE	Output circuit operating change input	Setting pin for changing video signal sampling circuit and output OP-AMP operation.
MOD	Mode change input	Setting pin for simultaneous or 3-point sequential sampling. MOD = L: 3-point sequential sampling mode MOD = H: Simultaneous sampling mode, CLK2 = CLK3 = H
VBS	Bias controlling input	Controlling output bias by voltage input. Ability of output driving LCD is changed.
TEST1 to 2	Test pin	Test pin, TEST1 to 2 connect to V_{DD1}

OPERATION OF FUNCTION

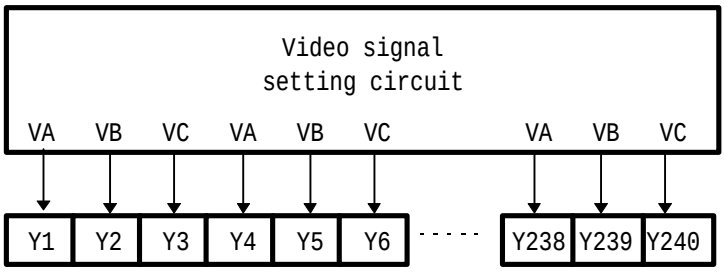
CASCADE SEQUENCE FOR OUTPUT PIN EXPANDING

- **When RL= H**
  Connect the previous STHL pin to the next STHR pin and connect input pin besides STHR and STHL to each device equally.
- **When RL= L**
  Connect the previous STHR pin to the next STHL pin and connect input pin besides STHR and STHL to each device equally.

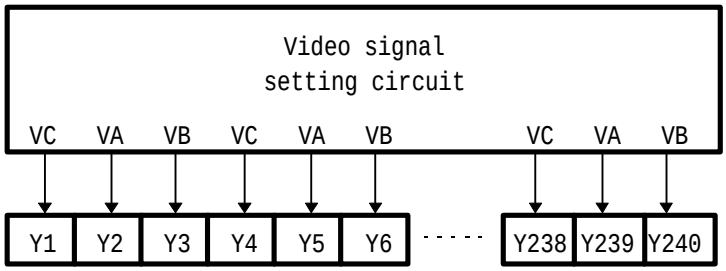
VIDEO SIGNAL MODE SETTING FUNCTION

The order of video signal corresponding to each output pin can be set as shown in the diagram below by changing the D1 signal.

· **When D1= L**



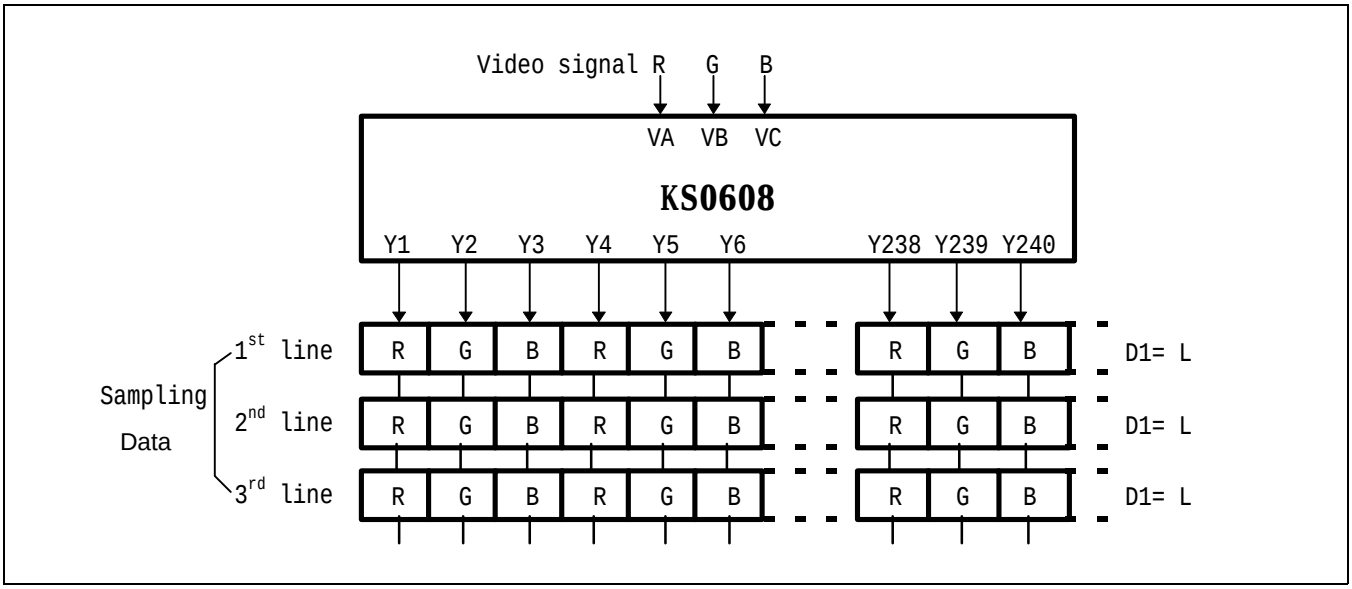
· **When D1= L**



EXAMPLES OF LCD PANEL CONNECTION

According to video signal mode setting function. Connections to Stripe and Delta array panels are possible. Stripe pixel array panel connection

(1) STRIPE Pixel Array Panel Connection



Video signal input pin connection.

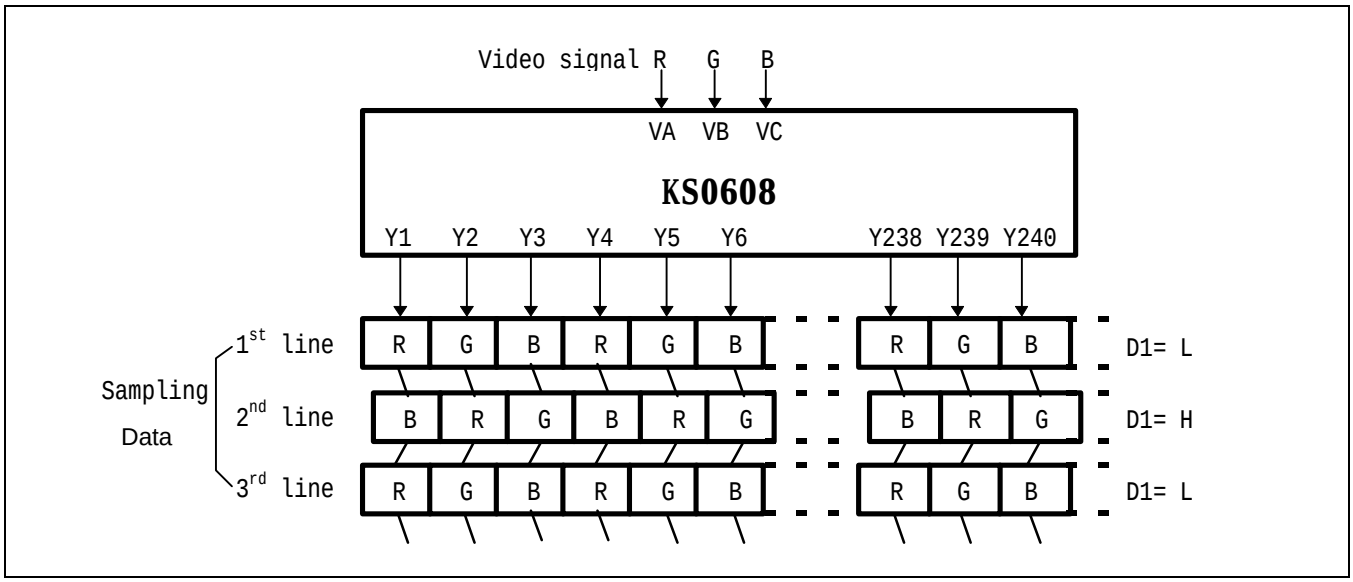
Video signal input pin	VA	VB	VC
Video signal	R	G	B

Setting of video signals sampled by output circuits and mode setting

	1st line	2nd line	3rd line	After 4th line
Y(3n+1)	R	R	R	R
Y(3n+2)	G	G	G	G
Y(3n+3)	B	B	B	B
D1 pin setting	H	H	H	H

(n=0,1,2,.....,79)

(2) DELTA Pixel Array Panel Connection



Video signal input pin connection.

Video signal input pin	VA	VB	VC
Video signal	R	G	B

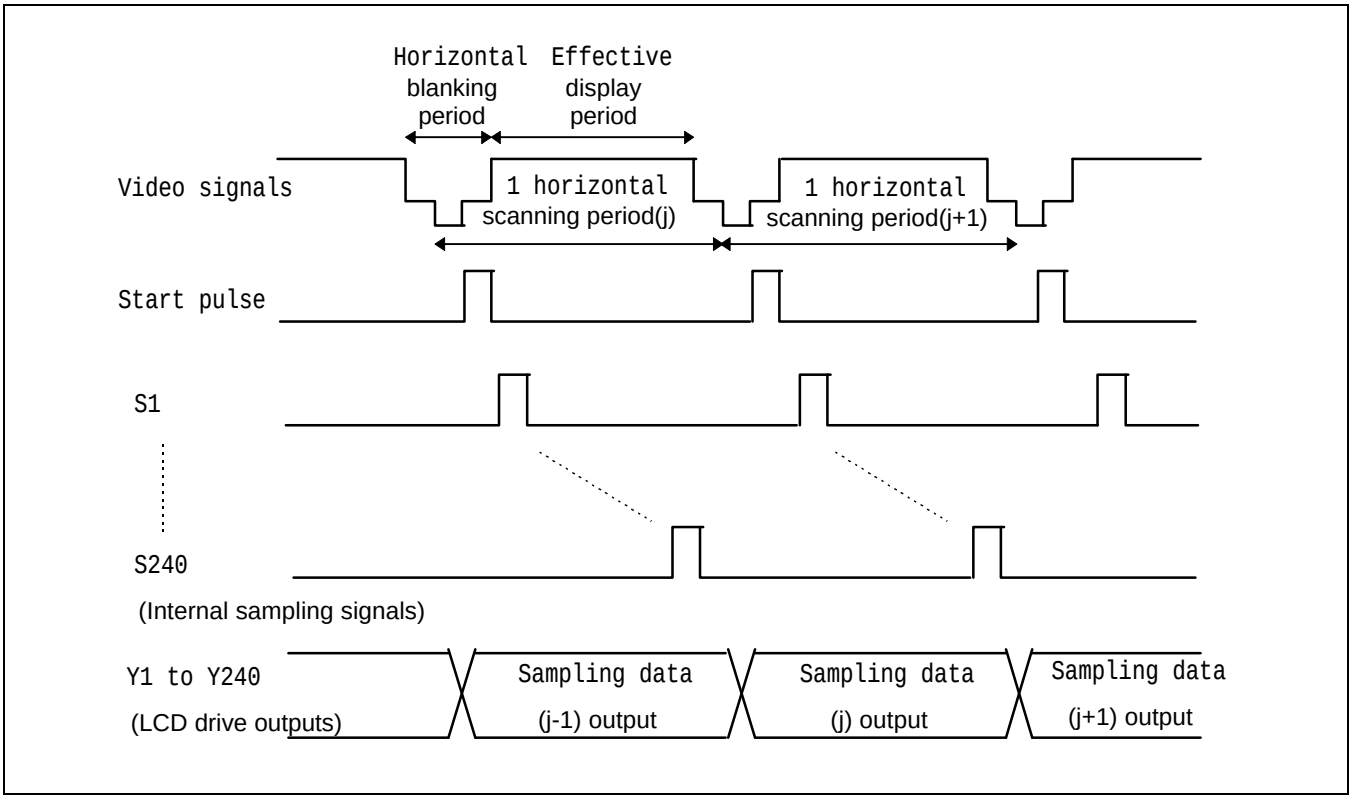
Setting of video signals sampled by output circuits and mode setting

	1st line	2nd line	3rd line	After 4th line
Y(3n+1)	R	B	R	B and R are alternately selected
Y(3n+2)	G	R	G	R and G are alternately selected
Y(3n+3)	B	G	B	G and B are alternately selected
D1 pin setting	H	L	H	L and H are alternately selected

(n=0,1,2,.....,79)

OPERATING TIMING OUTLINE

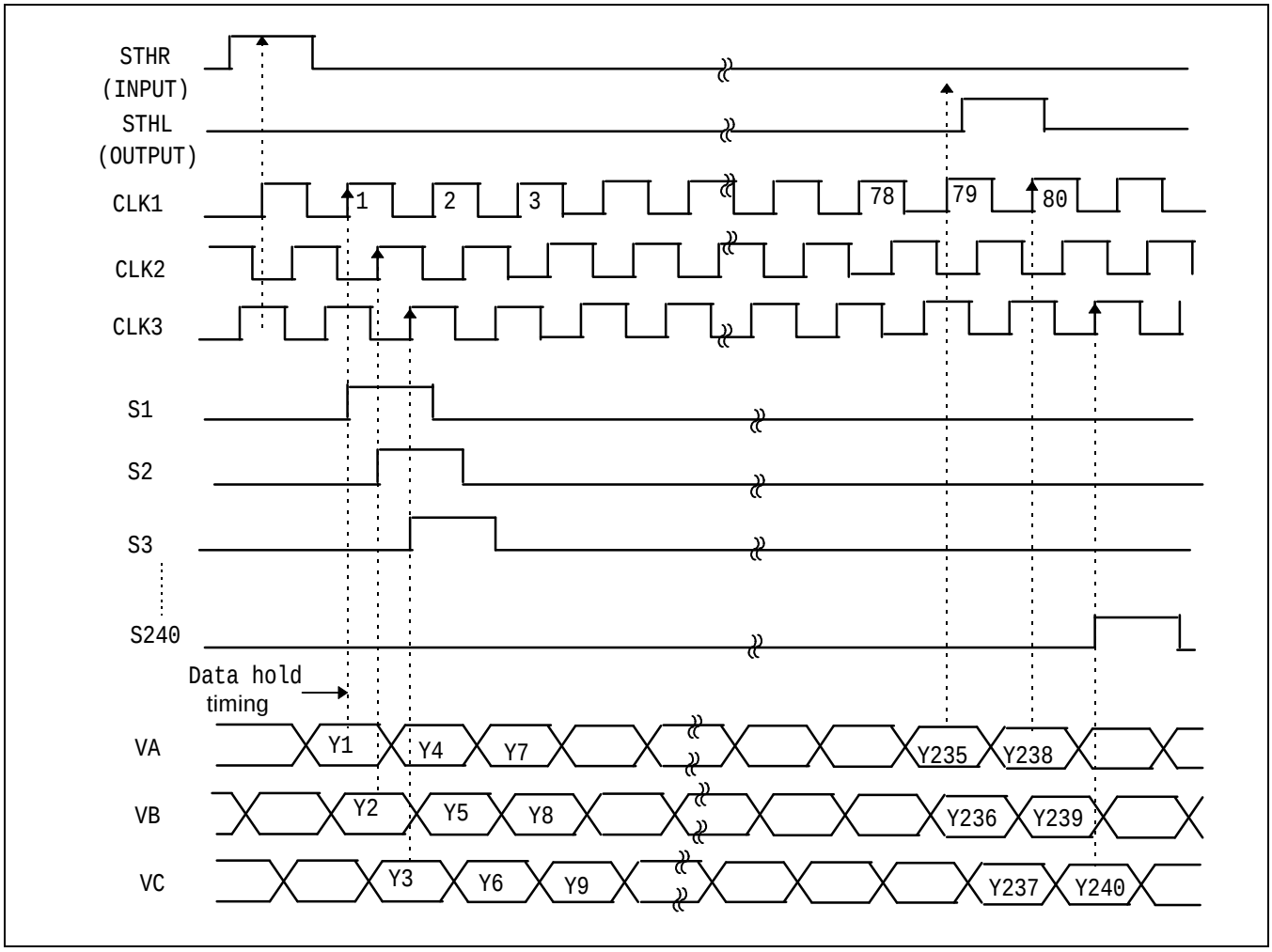
Full Operating timing



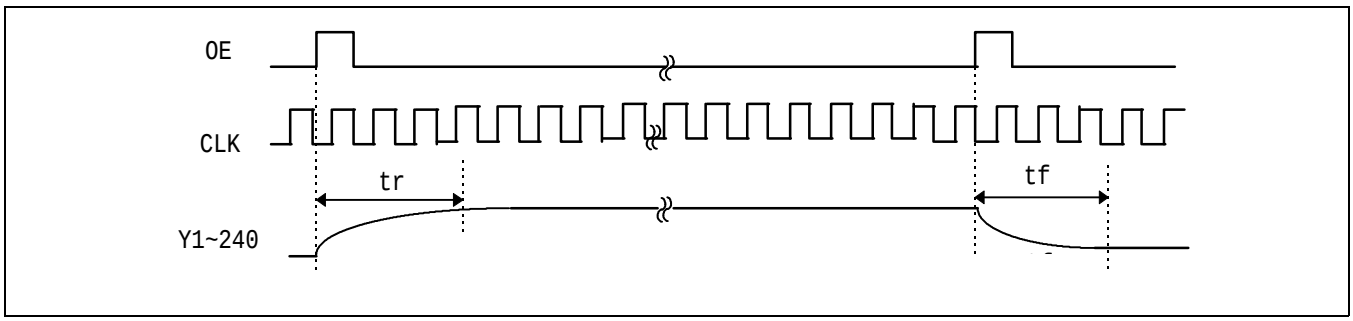
Samples a video signal based on the internal sampling pulse timing during 1 horizontal scanning period in each sample and hold circuit of the output circuit and outputs values corresponding to the sampling data.

OPERATING TIMING CHART

(1) Sequential Sampling Mode. In case RL = H, D1 = L, MOD = L

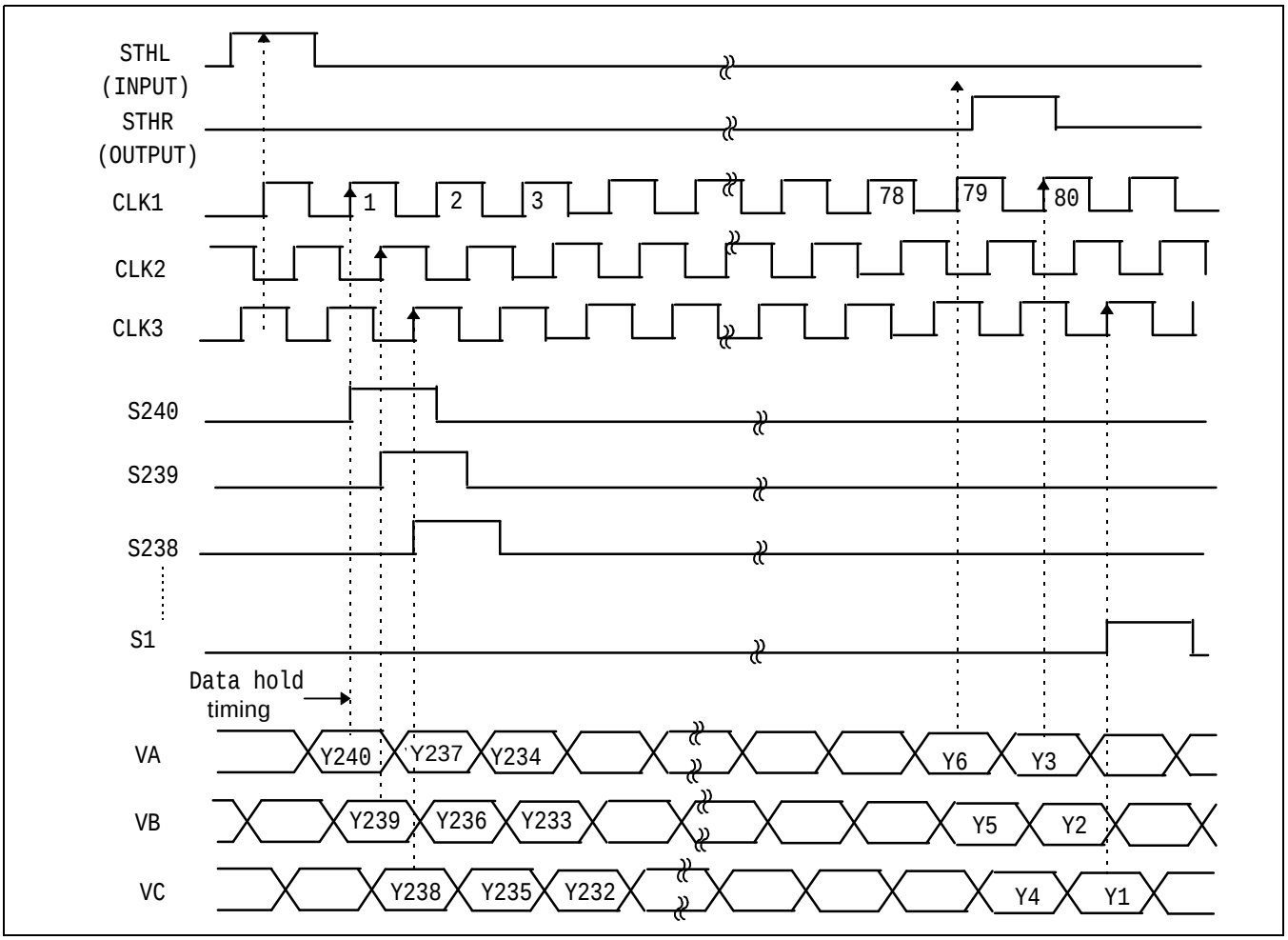


- S1 to S240 are internal sampling signals.
- Auto stand-by
  After 240th sampling Analog signal automatically become to stand-by status.
  Until the next input of STHR = H, stop sampling video signal.



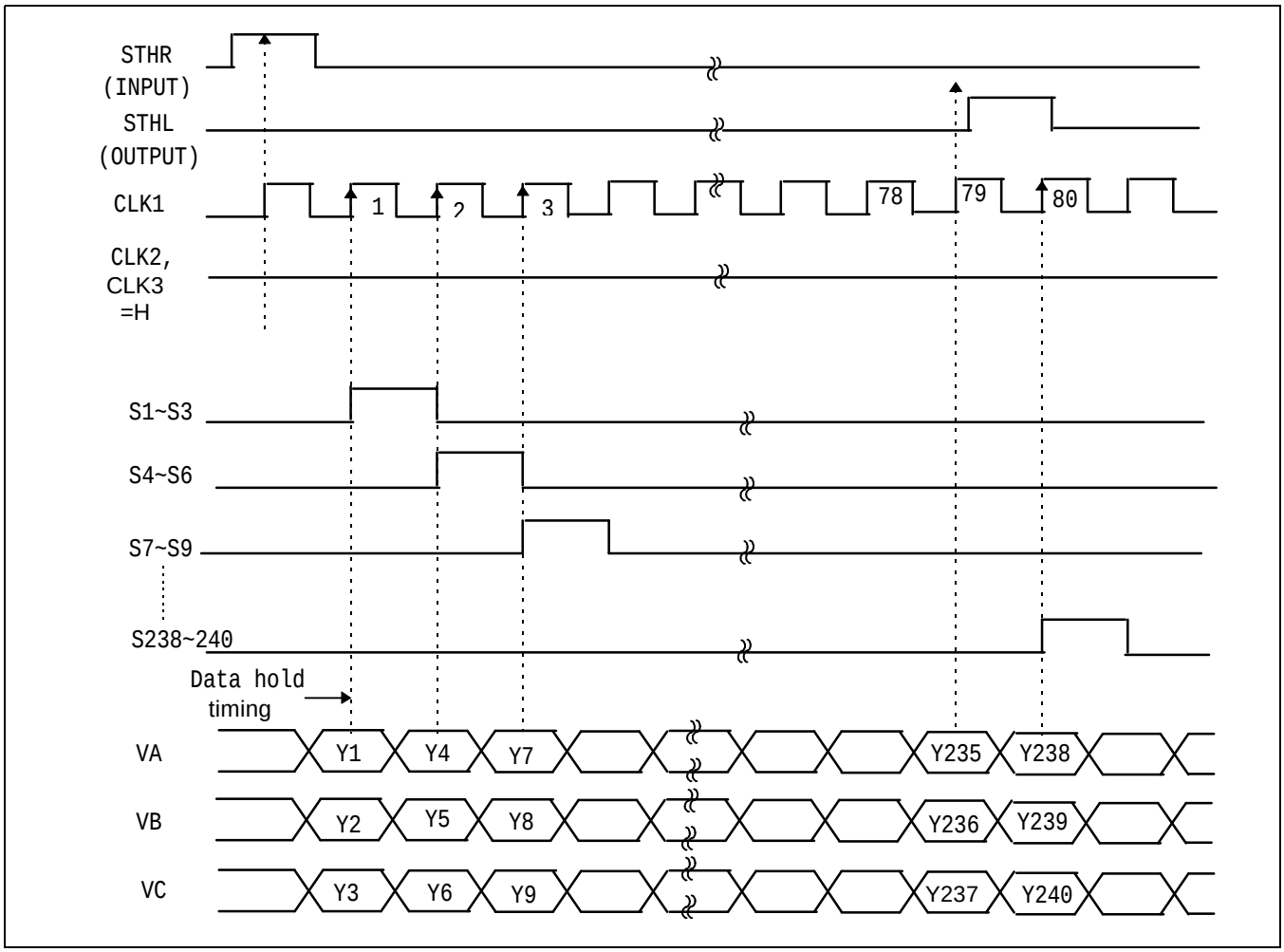
Start to output new data level at rising edge of OE Settling time tr, tf, be controlled by VBS

(2) Sequential sampling mode. In case RL = L, D1 = L, MOD = L



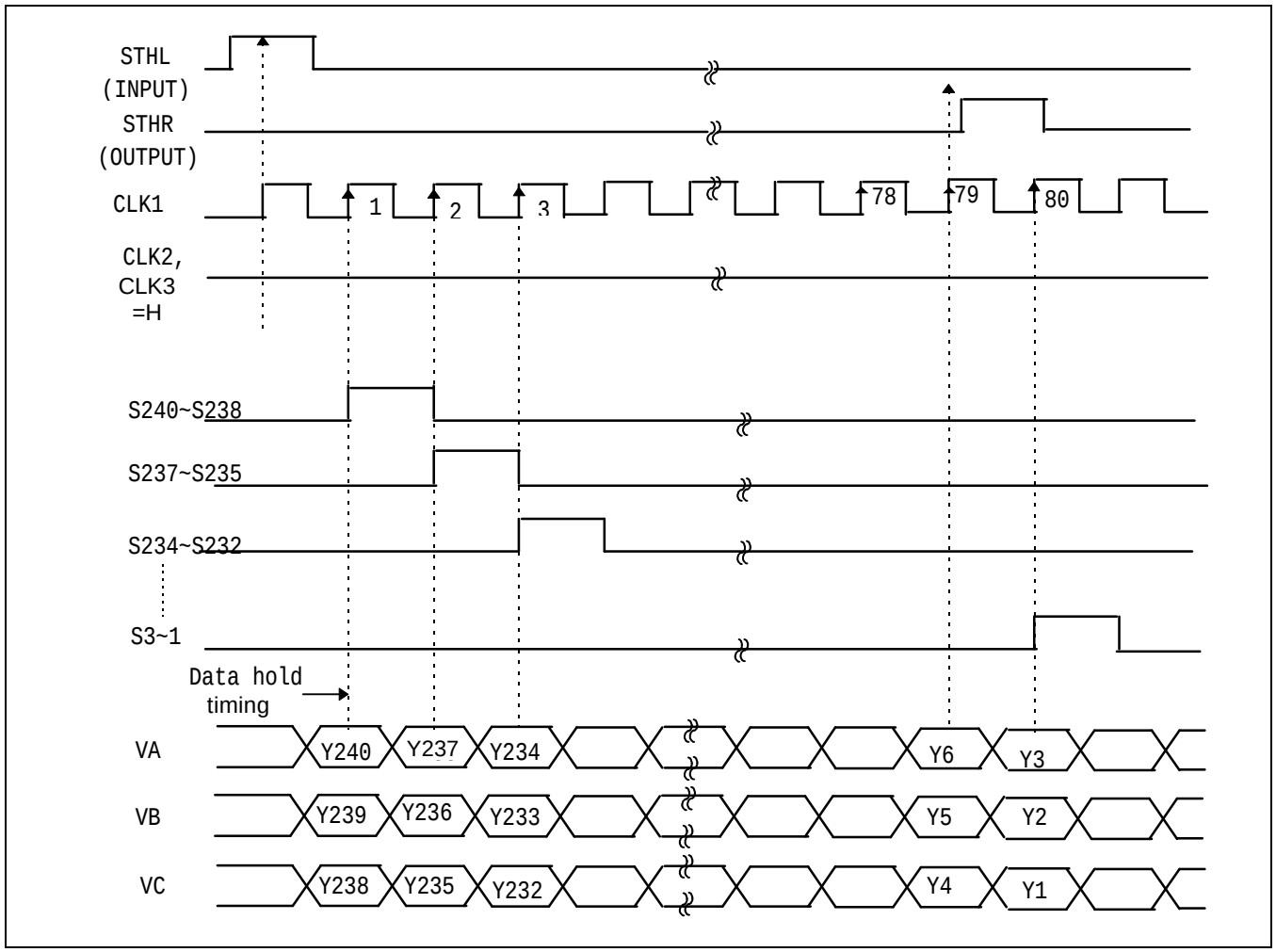
- S1 to S240 are internal sampling signals.

(3) Simultaneous sampling mode. In case RL = H, D1 = L, MOD = H



- S1 to S240 are internal sampling signals.

(4) Simultaneous sampling mode. In case RL = L, D1 = L, MOD = H



- S1 to S240 are internal sampling signals.

ABSOLUTE MAXIMUM RATING

(V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD1},V_{DD2}	–0.3 to + 7.0	V
Input voltage	VIN	–0.3 to V_{DD1} + 0.3	V
		–0.3 to V_{DD2} + 0.3	V
Output voltage	VOUT	–0.3 to V_{DD1} + 0.3	V
		–0.3 to V_{DD2} + 0.3	V
Storage temperature	Tstg	–45 to + 125	°C
Operating temperature	Topr	–30 to + 85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VDD1	–	2.7	3.0	5.5	V
	VDD2	–	3.0	5.0	5.5	V
Analog reference voltage	VBS	–	1.0	2.0	3.0	V
Operating frequency (When sequential sampling)	fCLK	–	0.5	–	10	MHz
Analog input voltage	VA,AB,VC	–	0.1	–	V_{DD2} – 0.1	V
Output load capacitance	CY	–	–	–	100	pF
Analog input capacitance	CinA	When 1MHz	–	9	20	pF
Logic input capacitance	CinD	When 1MHz	–	12.5	20	pF

Standard voltages V_{SS1} and Vss2 are GND (0V).
Relationship of power supply voltage $V_{DD1} \leq V_{DD2}$
In the case of turning on power supply set VA, VB, VC, Logic input pins after V_{DD1}, V_{DD2}.
And in the case of shutting off power set by reverse sequence of this.

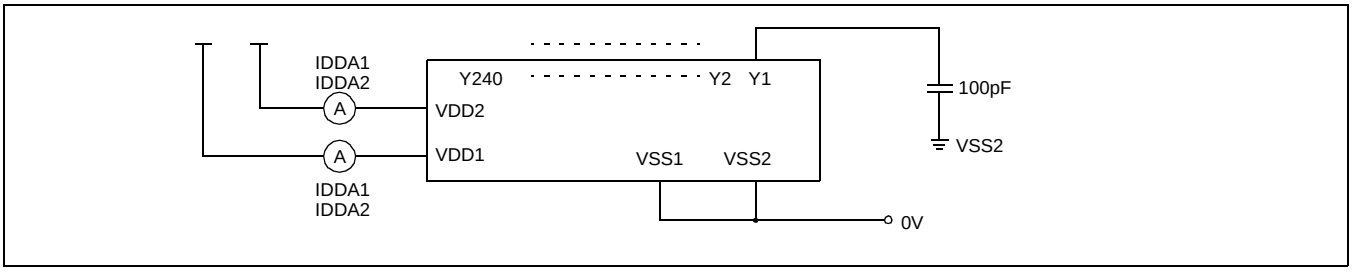
DC CHARACTERISTICS

(Ta = 25°C,V_{DD1}= 3.0V,V_{DD2} = 5.0V,V_{SS1} = V_{SS2} = 0V,VBS = 2.5V,Fclk=10MHz,When sequential sampling mode)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog current consumption	IDDA1	Note1, 2, 3	–	4.5	10	mA
	IDDA2	Note1, 2, 3 but have noload	–	3.5	–	mA
Digital current consumption	IDDD1	Note1	–	1.5	3.5	mA
	IDDD2	Non clocking status	–	–	100	μA
High level input voltage	VIH	CLK1 to 3, OE, D1, RL, MOD, STHR, STHL, TEST1 to 2	0.7 V_{DD1}	–	V	V
Low level input voltage	VIL		0	–	0.3 V_{DD1}	V
Input leakage current	VL1	CLK1, RL, OE, D1, VBS	–10	–	10	μA
Pull-up resistor	RPU1	V_{DD1} = 3.6V/CLK2,3 TEST1 to 2	1.5	5	15	kΩ
Pull-down resistor	RPU2	V_{DD1} = 3.6V/MOD	30	100	300	kΩ
High level output voltage	VOH	IO = –1mA/STHR, STHL	V_{DD1} – 0.3	–	–	V
Low level output voltage	VOL	IO = 1mA/STHR, STHL	–	–	0.3	V
Analog input current	IVA to IVC	VA, VB, VC frequency = 0.5MHz VA, VB, VC amplitude = (V_{DD2}–0.1) to 0.1V	–150	–	150	μA
High level output current	IOH	VA, VB, VC = 4.8V Set output voltage (Y1 to Y240) = 3.8V	0.03	0.15	–	mA
Low level output current	IOL	VA,VB,VC = 0.2V Set output voltage (Y1 to Y240) = 1.2V	0.15	2	–	mA
Output deviation	ΔVO	VA, VB, VC = 0.1 to 4.9V	–	± 15	–	mV

NOTES:

1. Load condition is the figure as follows.
   Analog input signal (VA, VB, VC = 5MHz, Amplitude 0.2 to 4.8V), OE = 100kHz, VBS = 2.5V



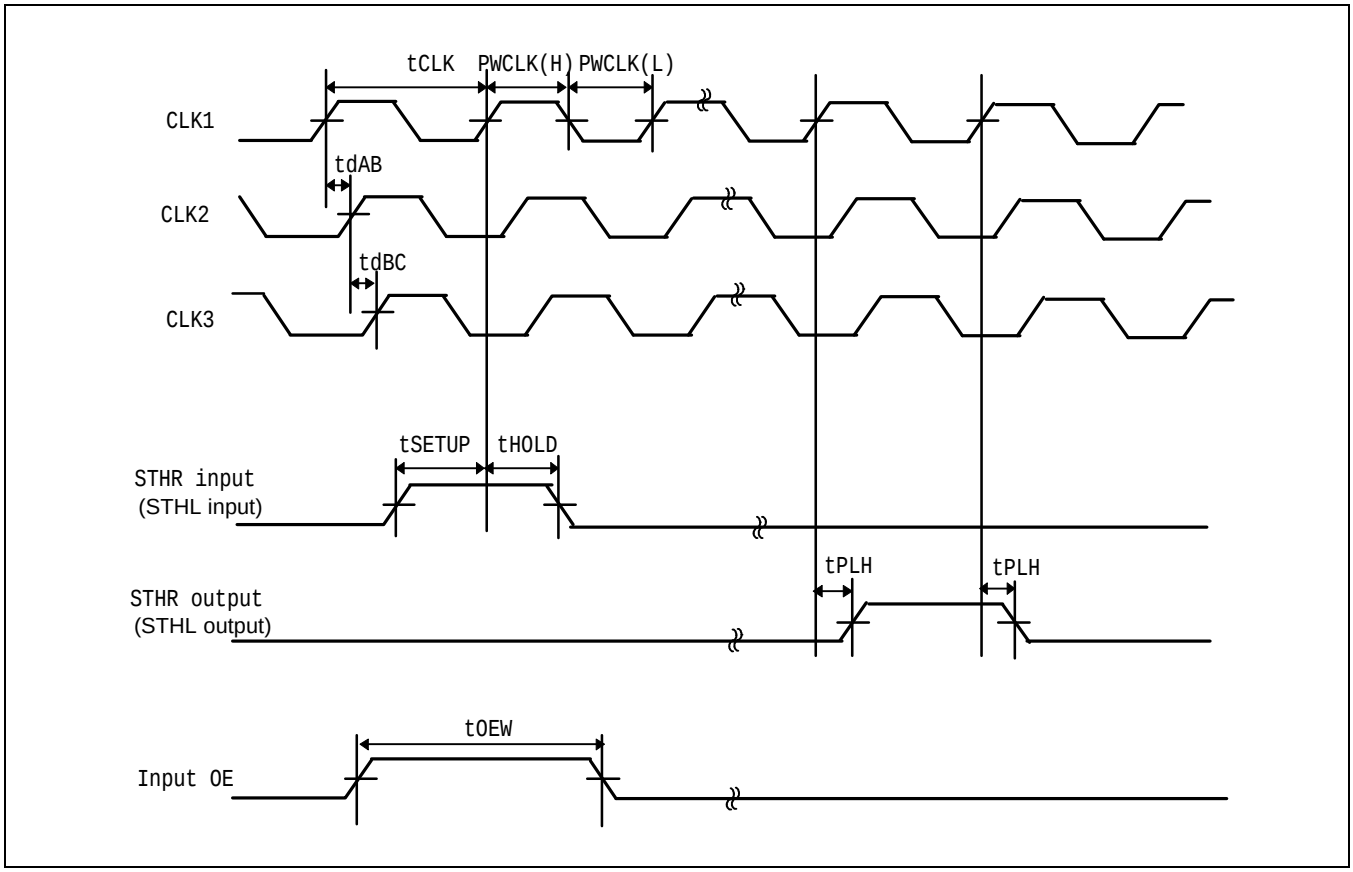
2. Load condition is variable.
3. Formula of power consumption in the case of adding load is as follows.
   IDDA1 × V_{DD2} + IDDD1 × V_{DD1}
   In the case of noload should change IDDA1 to IDDA2 from this formula.

AC CHARACTERISTICS

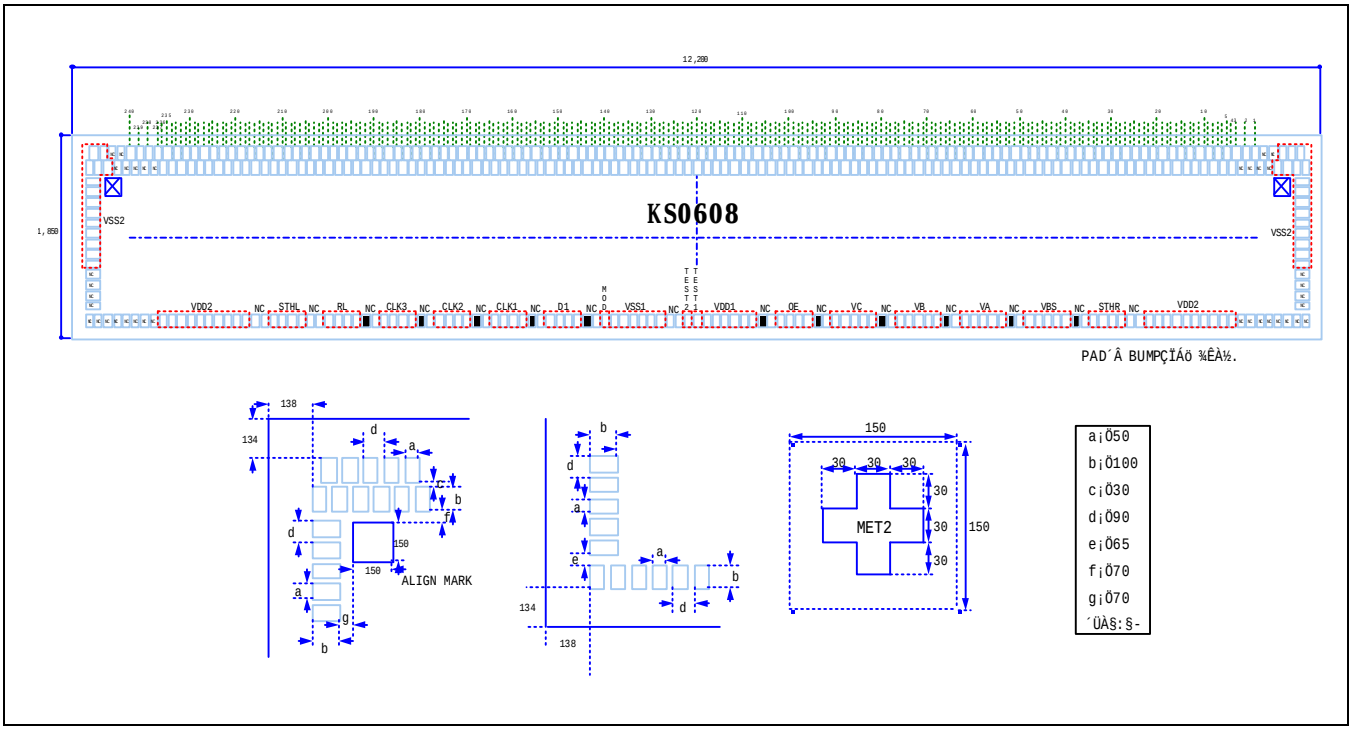
(Ta = –30°C to + 85, V_{DD1} = 2.7 to 5.5V, V_{DD2} = 3.0 to 5.0V, V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock cycle time	tCLK	–	100	–	2000	ns
High level clock width	PWCLK (H)	–	40	–	–	ns
Low level clock width	PWCLK (L)	–	40	–	–	ns
Between CLKs delay time	tdAB, tdBC	–	25	–	tCLK/2	ns
Start pulse setup time	tSETUP	–	10	–	–	ns
Start pulse hold time	tHOLD	–	10	–	–	ns
Start pulse output delay time	tPLH	load capacitance = 25pF	10	–	50	ns
High level OE width	tOEW	–	1.0	–	–	µs

AC TIMING DIAGRAM



PAD FORMAT


12,200
1,850
KS0608
VSS2
VSS2
VDD2 NC STHL NC RL NC CLK3 NC CLK2 NC CLK1 NC D1 NC MODE VSS1 NC TEST2 TEST1 VDD1 NC OE NC VC NC VB NC VA NC VBS NC STHR NC VDD2
PAD´Â BUMPÇïÁö ¾ÊÀ½.
138
134
ALIGN MARK
150
150
MET2
30
30
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