

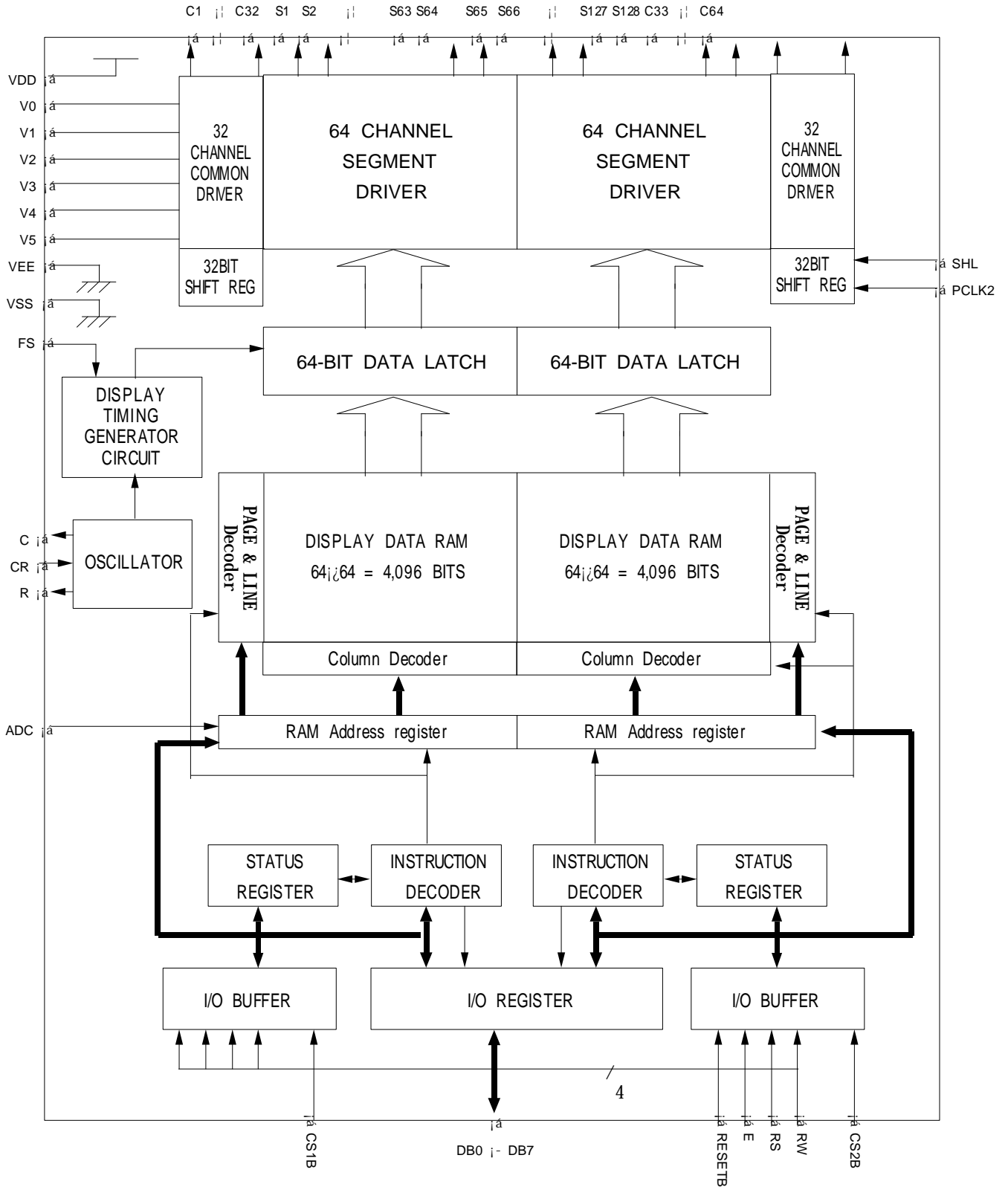
INTRODUCTION

KS0708 is a single-chip LCD driver LSI for liquid crystal dot-matrix graphic display systems. It incorporates 192 driver circuit for 64 common and 128 segment, and 64 × 128-bit bit-map RAM. It is capable of interfacing with the microprocessor, accepting 8-bit parallel display data directly from it, and storing data in an on-chip Display Data RAM. And it generates internal signals for using LCD driving independent of microprocessor clock.

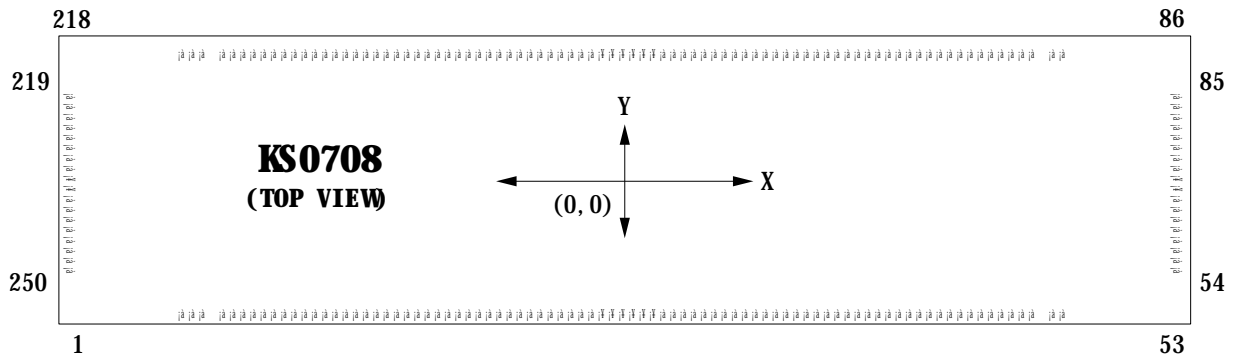
FEATURES

- 64-Channel COMMON & 128-Channel SEGMENT Driver for DOT matrix LCD
- On-chip display data RAM : 64 × 128 = 8192bits
- Display data is stored in display data RAM from MPU
 - RAM bit data : ON(1) , OFF(0)
- Internal timing generator circuit for dynamic display
- 8-bit parallel bi-directional data bus
- Applicable LCD duty : 1/64
- Power supply voltages : Power supply voltage range : 4.5 V - 5.5 V(VDD)
LCD Driving voltage range : 8.0 V - 17.0 V(VLCD = VDD - VEE)
- Wide operating temperature range : Ta = -30°C - 85°C
- High Voltage CMOS process
- Package : available bumped chip

BLOCK DIAGRAM



PAD CONFIGURATION



| ITEM | PAD NO. | SIZE | | UNIT |
|-------------------|-----------|--------|------|------|
| | | X | Y | |
| CHIP SIZE | - | 12590 | 3630 | S- |
| PAD PITCH | - | 90(MN) | | |
| BUMPED PAD SIZE | 1 ~ 53 | 56 | 140 | |
| | 54 ~ 85 | 140 | 56 | |
| | 86 ~ 218 | 56 | 140 | |
| | 219 ~ 250 | 140 | 56 | |
| BUMPED PAD HEIGHT | ALL PAD | 18 ± 3 | | |

PAD Center Coordinates

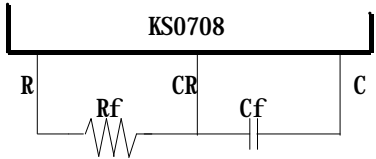
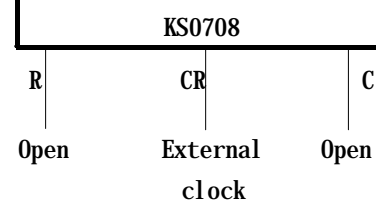
| PAD NO. | PAD NAME | X | Y | PAD NO. | PAD NAME | X | Y | PAD NO. | PAD NAME | X | Y | PAD NO. | PAD NAME | X | Y |
|---------|----------|-------|---------|---------|----------|------|--------|---------|----------|-------|-------|---------|----------|-------|---------|
| 1 | DUMMY | -6115 | -1600 | 64 | C11 | 6115 | -486.5 | 127 | S40 | 2205 | 163.5 | 190 | S103 | -3465 | 163.5 |
| 2 | DUMMY | -6025 | -1600 | 65 | C12 | 6115 | -396.5 | 128 | S41 | 2115 | 163.5 | 191 | S104 | -3555 | 163.5 |
| 3 | DUMMY | -5935 | -1600 | 66 | C13 | 6115 | -306.5 | 129 | S42 | 2025 | 163.5 | 192 | S105 | -3645 | 163.5 |
| 4 | VEE | -5477 | -1600 | 67 | C14 | 6115 | -216.5 | 130 | S43 | 1935 | 163.5 | 193 | S106 | -3735 | 163.5 |
| 5 | VEE | -5257 | -1600 | 68 | C15 | 6115 | -126.5 | 131 | S44 | 1845 | 163.5 | 194 | S107 | -3825 | 163.5 |
| 6 | VEE | -5037 | -1600 | 69 | C16 | 6115 | -36.5 | 132 | S45 | 1755 | 163.5 | 195 | S108 | -3915 | 163.5 |
| 7 | V5 | -4817 | -1600 | 70 | C17 | 6115 | 53.5 | 133 | S46 | 1665 | 163.5 | 196 | S109 | -4005 | 163.5 |
| 8 | V5 | -4597 | -1600 | 71 | C18 | 6115 | 143.5 | 134 | S47 | 1575 | 163.5 | 197 | S110 | -4095 | 163.5 |
| 9 | V5 | -4377 | -1600 | 72 | C19 | 6115 | 233.5 | 135 | S48 | 1485 | 163.5 | 198 | S111 | -4185 | 163.5 |
| 10 | V4 | -4157 | -1600 | 73 | C20 | 6115 | 323.5 | 136 | S49 | 1395 | 163.5 | 199 | S112 | -4275 | 163.5 |
| 11 | V4 | -3937 | -1600 | 74 | C21 | 6115 | 413.5 | 137 | S50 | 1305 | 163.5 | 200 | S113 | -4365 | 163.5 |
| 12 | V4 | -3717 | -1600 | 75 | C20 | 6115 | 503.5 | 138 | S51 | 1215 | 163.5 | 201 | S114 | -4455 | 163.5 |
| 13 | V3 | -3497 | -1600 | 76 | C23 | 6115 | 593.5 | 139 | S52 | 1125 | 163.5 | 202 | S115 | -4545 | 163.5 |
| 14 | V3 | -3277 | -1600 | 77 | C24 | 6115 | 683.5 | 140 | S53 | 1035 | 163.5 | 203 | S116 | -4635 | 163.5 |
| 15 | V3 | -3057 | -1600 | 78 | C25 | 6115 | 773.5 | 141 | S54 | 945 | 163.5 | 204 | S117 | -4725 | 163.5 |
| 16 | V2 | -2837 | -1600 | 79 | C26 | 6115 | 863.5 | 142 | S55 | 855 | 163.5 | 205 | S118 | -4815 | 163.5 |
| 17 | V2 | -2617 | -1600 | 80 | C27 | 6115 | 953.5 | 143 | S56 | 765 | 163.5 | 206 | S119 | -4905 | 163.5 |
| 18 | V2 | -2397 | -1600 | 81 | C28 | 6115 | 1043.5 | 144 | S57 | 675 | 163.5 | 207 | S120 | -4995 | 163.5 |
| 19 | V1 | -2177 | -1600 | 82 | C29 | 6115 | 1133.5 | 145 | S58 | 585 | 163.5 | 208 | S121 | -5085 | 163.5 |
| 20 | V1 | -1957 | -1600 | 83 | C30 | 6115 | 1223.5 | 146 | S59 | 495 | 163.5 | 209 | S122 | -5175 | 163.5 |
| 21 | V1 | -1737 | -1600 | 84 | C31 | 6115 | 1313.5 | 147 | S60 | 405 | 163.5 | 210 | S123 | -5265 | 163.5 |
| 22 | V0 | -1517 | -1600 | 85 | C32 | 6115 | 1403.5 | 148 | S61 | 315 | 163.5 | 211 | S124 | -5355 | 163.5 |
| 23 | V0 | -1297 | -1600 | 86 | DUMMY | 6115 | 163.5 | 149 | S62 | 225 | 163.5 | 212 | S125 | -5445 | 163.5 |
| 24 | V0 | -1077 | -1600 | 87 | DUMMY | 6025 | 163.5 | 150 | S63 | 135 | 163.5 | 213 | S126 | -5535 | 163.5 |
| 25 | VDD | -857 | -1600 | 88 | S1 | 5715 | 163.5 | 151 | S64 | 45 | 163.5 | 214 | S127 | -5625 | 163.5 |
| 26 | VDD | -637 | -1600 | 89 | S2 | 5625 | 163.5 | 152 | S65 | -45 | 163.5 | 215 | S128 | -5715 | 163.5 |
| 27 | VDD | -417 | -1600 | 90 | S3 | 5535 | 163.5 | 153 | S66 | -135 | 163.5 | 216 | DUMMY | -5935 | 163.5 |
| 28 | VSS | -197 | -1600 | 91 | S4 | 5445 | 163.5 | 154 | S67 | -225 | 163.5 | 217 | DUMMY | -6025 | 163.5 |
| 29 | VSS | 23 | -1600 | 92 | S5 | 5355 | 163.5 | 155 | S68 | -315 | 163.5 | 218 | DUMMY | -6115 | 163.5 |
| 30 | VSS | 243 | -1600 | 93 | S6 | 5265 | 163.5 | 156 | S69 | -405 | 163.5 | 219 | C64 | -6115 | 1403.5 |
| 31 | PCLK2 | 463 | -1600 | 94 | S7 | 5175 | 163.5 | 157 | S70 | -495 | 163.5 | 220 | C63 | -6115 | 1313.5 |
| 32 | FS | 683 | -1600 | 95 | S8 | 5085 | 163.5 | 158 | S71 | -585 | 163.5 | 221 | C62 | -6115 | 1223.5 |
| 33 | SHL | 903 | -1600 | 96 | S9 | 4995 | 163.5 | 159 | S72 | -675 | 163.5 | 222 | C61 | -6115 | 1133.5 |
| 34 | ADC | 1123 | -1600 | 97 | S10 | 4905 | 163.5 | 160 | S73 | -765 | 163.5 | 223 | C60 | -6115 | 1043.5 |
| 35 | CS2B | 1343 | -1600 | 98 | S11 | 4815 | 163.5 | 161 | S74 | -855 | 163.5 | 224 | C59 | -6115 | 953.5 |
| 36 | C | 1563 | -1600 | 99 | S12 | 4725 | 163.5 | 162 | S75 | -945 | 163.5 | 225 | C58 | -6115 | 863.5 |
| 37 | CR | 1783 | -1600 | 100 | S13 | 4635 | 163.5 | 163 | S76 | -1035 | 163.5 | 226 | C57 | -6115 | 773.5 |
| 38 | R | 2003 | -1600 | 101 | S14 | 4545 | 163.5 | 164 | S77 | -1125 | 163.5 | 227 | C56 | -6115 | 683.5 |
| 39 | DB0 | 2175 | -1600 | 102 | S15 | 4455 | 163.5 | 165 | S78 | -1215 | 163.5 | 228 | C55 | -6115 | 593.5 |
| 40 | DB1 | 2467 | -1600 | 103 | S16 | 4365 | 163.5 | 166 | S89 | -1305 | 163.5 | 229 | C54 | -6115 | 503.5 |
| 41 | DB2 | 2759 | -1600 | 104 | S17 | 4275 | 163.5 | 167 | S80 | -1395 | 163.5 | 230 | C53 | -6115 | 413.5 |
| 42 | DB3 | 3051 | -1600 | 105 | S18 | 4185 | 163.5 | 168 | S81 | -1485 | 163.5 | 231 | C52 | -6115 | 323.5 |
| 43 | DB4 | 3343 | -1600 | 106 | S19 | 4095 | 163.5 | 169 | S82 | -1575 | 163.5 | 232 | C51 | -6115 | 233.5 |
| 44 | DB5 | 3635 | -1600 | 107 | S20 | 4005 | 163.5 | 170 | S83 | -1665 | 163.5 | 233 | C50 | -6115 | 143.5 |
| 45 | DB6 | 3927 | -1600 | 108 | S21 | 3915 | 163.5 | 171 | S84 | -1755 | 163.5 | 234 | C49 | -6115 | 53.5 |
| 46 | DB7 | 4219 | -1600 | 109 | S22 | 3825 | 163.5 | 172 | S85 | -1845 | 163.5 | 235 | C48 | -6115 | -36.5 |
| 47 | RS | 4559 | -1600 | 110 | S23 | 3735 | 163.5 | 173 | S86 | -1935 | 163.5 | 236 | C47 | -6115 | -126.5 |
| 48 | RW | 4779 | -1600 | 111 | S24 | 3645 | 163.5 | 174 | S87 | -2025 | 163.5 | 237 | C46 | -6115 | -216.5 |
| 49 | E | 4999 | -1600 | 112 | S25 | 3555 | 163.5 | 175 | S88 | -2115 | 163.5 | 238 | C45 | -6115 | -306.5 |
| 50 | CS1B | 5219 | -1600 | 113 | S26 | 3465 | 163.5 | 176 | S89 | -2205 | 163.5 | 239 | C44 | -6115 | -396.5 |
| 51 | RESETB | 5439 | -1600 | 114 | S27 | 3375 | 163.5 | 177 | S90 | -2295 | 163.5 | 240 | C43 | -6115 | -486.5 |
| 52 | DUMMY | 6025 | -1600 | 115 | S28 | 3285 | 163.5 | 178 | S91 | -2385 | 163.5 | 241 | C42 | -6115 | -576.5 |
| 53 | DUMMY | 6115 | -1600 | 116 | S29 | 3195 | 163.5 | 179 | S92 | -2475 | 163.5 | 242 | C41 | -6115 | -666.5 |
| 54 | C1 | 6115 | -1386.5 | 117 | S30 | 3105 | 163.5 | 180 | S93 | -2565 | 163.5 | 243 | C40 | -6115 | -756.5 |
| 55 | C2 | 6115 | -1296.5 | 118 | S31 | 3015 | 163.5 | 181 | S94 | -2655 | 163.5 | 244 | C39 | -6115 | -846.5 |
| 56 | C3 | 6115 | -1206.5 | 119 | S32 | 2925 | 163.5 | 182 | S95 | -2745 | 163.5 | 245 | C38 | -6115 | -936.5 |
| 57 | C4 | 6115 | -1116.5 | 120 | S33 | 2835 | 163.5 | 183 | S96 | -2835 | 163.5 | 246 | C37 | -6115 | -1026.5 |
| 58 | C5 | 6115 | -1026.5 | 121 | S34 | 2745 | 163.5 | 184 | S97 | -2925 | 163.5 | 247 | C36 | -6115 | -1116.5 |
| 59 | C6 | 6115 | -936.5 | 122 | S35 | 2655 | 163.5 | 185 | S98 | -3015 | 163.5 | 248 | C35 | -6115 | -1206.5 |
| 60 | C7 | 6115 | -846.5 | 123 | S36 | 2565 | 163.5 | 186 | S99 | -3105 | 163.5 | 249 | C34 | -6115 | -1296.5 |
| 61 | C8 | 6115 | -756.5 | 124 | S37 | 2475 | 163.5 | 187 | S100 | -3195 | 163.5 | 250 | C33 | -6115 | -1386.5 |
| 62 | C9 | 6115 | -666.5 | 125 | S38 | 2385 | 163.5 | 188 | S101 | -3285 | 163.5 | | | | |
| 63 | C10 | 6115 | -576.5 | 126 | S39 | 2295 | 163.5 | 189 | S102 | -3375 | 163.5 | | | | |

PAD DESCRIPTION

Power Supply

| Name | I/O | Description |
|----------------------------|--------|--|
| VDD | Supply | Power supply |
| VSS | Supply | Ground |
| VEE | Supply | For LCD driver circuit |
| V0, V1 V2, V3 V4, V5 | Supply | LCD driver supply voltages The voltages must satisfy the following relationship $VDD \geq V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq VEE$ |

Oscillator

| Name | I/O | Description | | | | | | |
|--------------|-----------------------------|---|----|-----------------------|---|-----------------------------|---|-----------------------------|
| C CR R | O I O | <p>RC Oscillator</p> <p>i) Internal clock</p>  <p style="text-align: right;">$R_f : 47\text{K}\Omega$ $C_f : 20\text{nF}$</p> <p>ii) External clock</p>  | | | | | | |
| FS | I | <p>Frequency Selection.</p> <p>When the frame frequency is 70Hz, the oscillation frequency should be as following table.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>FS</th> <th>Oscillation Frequency</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>$f_{osc} = 430 \text{ kHz}$</td> </tr> <tr> <td>0</td> <td>$f_{osc} = 215 \text{ kHz}$</td> </tr> </tbody> </table> | FS | Oscillation Frequency | 1 | $f_{osc} = 430 \text{ kHz}$ | 0 | $f_{osc} = 215 \text{ kHz}$ |
| FS | Oscillation Frequency | | | | | | | |
| 1 | $f_{osc} = 430 \text{ kHz}$ | | | | | | | |
| 0 | $f_{osc} = 215 \text{ kHz}$ | | | | | | | |

Microprocessor Interface

| Name | I/O | Description | | | | | | |
|---------------|---|---|-------------|-------------|---|---|---|---|
| CS1B | I | First Chip(S1 ~ S64) Select input. Data input/output is enabled via E, RS, RW, and DB[0:7] when CS1B = Low. | | | | | | |
| CS2B | I | Second Chip(S65 ~ S128) Select input. Data input/output is enabled via E, RS, RW, and DB[0:7] when CS2B = Low. | | | | | | |
| RS | I | Register Selection i° HIGH : The data in DB[7:0] is display data i° LOW : The data in DB[7:0] is control data | | | | | | |
| RW | I | Read or Write | | | | | | |
| | | <table border="1"> <thead> <tr> <th>RW</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Data appears at DB<7:0> when E = High.</td> </tr> <tr> <td>L</td> <td>Display data DB<7:0> can be written at falling edge of E.</td> </tr> </tbody> </table> | RW | Description | H | Data appears at DB<7:0> when E = High. | L | Display data DB<7:0> can be written at falling edge of E. |
| | | RW | Description | | | | | |
| H | Data appears at DB<7:0> when E = High. | | | | | | | |
| L | Display data DB<7:0> can be written at falling edge of E. | | | | | | | |
| | | | | | | | | |
| E | I | Enable signal. | | | | | | |
| | | <table border="1"> <thead> <tr> <th>RW</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Read data in DB<7:0> appears the while E is high level.</td> </tr> <tr> <td>L</td> <td>Display data DB<7:0> is latched at falling edge of E.</td> </tr> </tbody> </table> | RW | Description | H | Read data in DB<7:0> appears the while E is high level. | L | Display data DB<7:0> is latched at falling edge of E. |
| | | RW | Description | | | | | |
| H | Read data in DB<7:0> appears the while E is high level. | | | | | | | |
| L | Display data DB<7:0> is latched at falling edge of E. | | | | | | | |
| | | | | | | | | |
| DB 0_i -DB7 | I / O | Data Bus [0 $_i$ -7] i° Bi-directional data bus | | | | | | |

Reset

| Name | I/O | Description |
|--------|-----|---|
| RESETB | I | Reset input i° Chip is initialized when RESETB is LOW |

LCD Driver Outputs

| Name | I/O | Description | | | | | | |
|-----------------------|---|---|---|--------------------------------------|---|---|---|---|
| C1 _j -C64 | O | LCD driver common output | | | | | | |
| S1 _j -S128 | O | LCD driver segment output | | | | | | |
| PCLK2 | I | Phase of internal shift clock(CLK2) | | | | | | |
| | | <table border="1"> <thead> <tr> <th>PCLK2</th> <th>Phase of Internal Shift Clock (CLK2)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Data shift at the falling edge of CLK2</td> </tr> <tr> <td>1</td> <td>Data shift at the rising edge of CLK2</td> </tr> </tbody> </table> | PCLK2 | Phase of Internal Shift Clock (CLK2) | 0 | Data shift at the falling edge of CLK2 | 1 | Data shift at the rising edge of CLK2 |
| | | PCLK2 | Phase of Internal Shift Clock (CLK2) | | | | | |
| | | 0 | Data shift at the falling edge of CLK2 | | | | | |
| 1 | Data shift at the rising edge of CLK2 | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| ADC | I | Address Control signal of Y address counter. | | | | | | |
| | | <table border="1"> <thead> <tr> <th>ADC</th> <th>Segment output direction</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>S1_j æ S2_j ¥¥¥ S63_j æ S64_j æ S65_j æ S66_j ¥¥¥ S127_j æ S128_j</td> </tr> <tr> <td>L</td> <td>S64_j æ S63_j ¥¥¥ S2_j æ S1_j æ S128_j æ S127_j ¥¥¥ S66_j æ S65_j</td> </tr> </tbody> </table> | ADC | Segment output direction | H | S1 _j æ S2 _j ¥¥¥ S63 _j æ S64 _j æ S65 _j æ S66 _j ¥¥¥ S127 _j æ S128 _j | L | S64 _j æ S63 _j ¥¥¥ S2 _j æ S1 _j æ S128 _j æ S127 _j ¥¥¥ S66 _j æ S65 _j |
| | | ADC | Segment output direction | | | | | |
| | | H | S1 _j æ S2 _j ¥¥¥ S63 _j æ S64 _j æ S65 _j æ S66 _j ¥¥¥ S127 _j æ S128 _j | | | | | |
| L | S64 _j æ S63 _j ¥¥¥ S2 _j æ S1 _j æ S128 _j æ S127 _j ¥¥¥ S66 _j æ S65 _j | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| SHL | I | Selection of data shift direction | | | | | | |
| | | <table border="1"> <thead> <tr> <th>SHL</th> <th>Data shift direction</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>C1_j æ C2_j æ C3_j ¥¥¥¥¥¥ C62_j æ C63_j æ C64_j</td> </tr> <tr> <td>L</td> <td>C64_j æ C63_j æ C62_j ¥¥¥¥¥¥ C3_j æ C2_j æ C1_j</td> </tr> </tbody> </table> | SHL | Data shift direction | H | C1 _j æ C2 _j æ C3 _j ¥¥¥¥¥¥ C62 _j æ C63 _j æ C64 _j | L | C64 _j æ C63 _j æ C62 _j ¥¥¥¥¥¥ C3 _j æ C2 _j æ C1 _j |
| | | SHL | Data shift direction | | | | | |
| | | H | C1 _j æ C2 _j æ C3 _j ¥¥¥¥¥¥ C62 _j æ C63 _j æ C64 _j | | | | | |
| L | C64 _j æ C63 _j æ C62 _j ¥¥¥¥¥¥ C3 _j æ C2 _j æ C1 _j | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |

FUNCTIONAL DESCRIPTION

Chip Select input

The KS0708 has two chip select pin, CS1B and CS2B. It can interface with a microprocessor when these pins(CS1B or CS2B) is Low. When both of these pins are set to High, DB0 to DB7 are high impedance and RS, RW, and E inputs are disabled. CS1B pin controls the display status of S1 to S64, and CS2B does that of S65 to S128. When CS1B and CS2B are Low at the same time, it is impossible to execute read operation. Therefore one of CS1B or CS2B should be set to Low((CS1B = "H" & CS2B = "L") or (CS1B = "L" & CS2B = "H")) in read operation. The RESETB signal is entered independent of the status of Chip Select.

| CS1B | CS2B | Read Operation | | Write Operation | |
|------|------|----------------|-----|-----------------|-----|
| | | CS1 | CS2 | CS1 | CS2 |
| H | H | iZ | iZ | iZ | iZ |
| L | H | iU | iZ | iU | iZ |
| H | L | iZ | iU | iZ | iU |
| L | L | - | - | iU | iU |

(- : Not Recommended, iU : Operation, X : No Operation)

Table 1. Relationship between Chip Select pins and Read/Write Operation

Microprocessor Interface

KS0708 transfers 8-bit parallel in either direction between the controlling microprocessor and the KS0708 through the 8-bit I/O buffer(DB0 to DB7).

RS, RW and E identify the type of parallel data transfer to be made as shown in table 2.

| RS | RW | Description |
|----|----|---|
| 1 | 1 | Display data read |
| 1 | 0 | Display data write |
| 0 | 1 | Status read |
| 0 | 0 | Writes to internal register (Instruction) |

Table 2. Microprocessor Interface

Busy flag

Busy flag indicates whether KS0708 is operating or not. When busy flag is high, KS0708 is in internal operation. When low, KS0708 can accept the data or instruction. DB7 indicates busy flag of the KS0708.

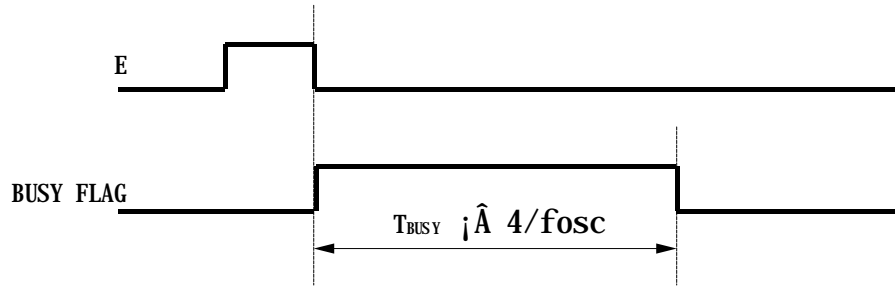


Figure 1. Busy timing

Display Timing Generator Circuit

This section explains how the timing generation circuit operates.

- ⊙ Signal generation to display start line counter and display data latch circuit.
- ⊙ The display clock(CLK2) generates a clock to the line counter . The display start line address of the display RAM is synchronized with the display clock. 128-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pin.
- ⊙ LCD AC signal(M) generation.

Display Data RAM

The Display Data RAM stores pixel data for the LCD. It is a 128-column \times 64-row addressable array as shown in Figure 3. The 64 rows are divided into 8 pages of 8 lines. Data is read from or written to the 8 lines of each page directly through DB0 to DB7.

The microprocessor reads from and writes to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written to RAM at the same time as data is being displayed, without causing the LCD to flick.

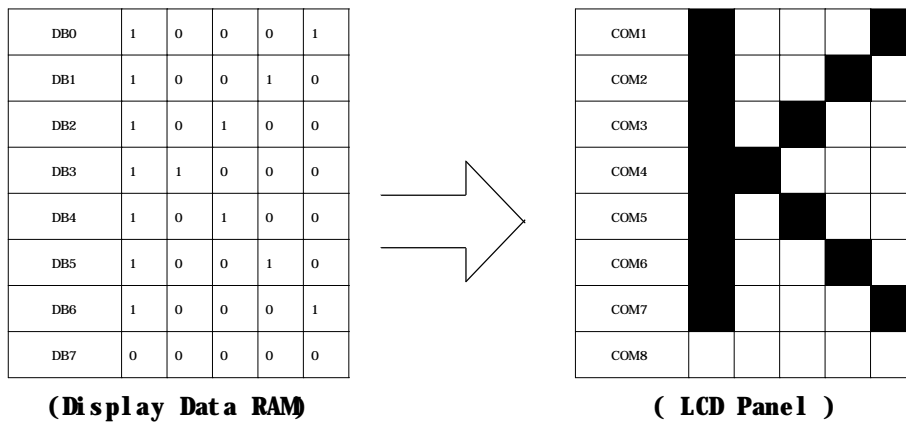


Figure 2. RAM-to-LCD data transfer

| Page address | Line address | SEGMENT OUTPUT(S1 ~ S64) | | | | | | | | DATA BUS | SEGMENT OUTPUT(S65 ~ S128) | | | | | | | | Line address | Page address | | |
|--------------|--|--------------------------|-----|-----|-----|---|-------|-------|-------|--------------------|--|-------|-------|-------|-------|---|---------|---------|--------------|--------------|--|---------|
| | | S 1 | S 2 | S 3 | S 4 | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | S 6 1 | S 6 2 | S 6 3 | | S 6 4 | S 6 5 | S 6 6 | S 6 7 | S 6 8 | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | S 1 2 5 | S 1 2 6 | | | S 1 2 7 | S 1 2 8 |
| 000 | 00 01 02 03 04 05 06 07 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | 00 01 02 03 04 05 06 07 | 000 |
| 001 | 08 09 10 11 12 13 14 15 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | 08 09 10 11 12 13 14 15 | 001 |
| 010 | 16 17 18 19 20 21 22 23 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | 16 17 18 19 20 21 22 23 | 010 |
| 011 | 24 25 26 27 28 29 30 31 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | 24 25 26 27 28 29 30 31 | 011 |
| 100 | 32 33 34 35 36 37 38 39 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | 32 33 34 35 36 37 38 39 | 100 |
| 101 | 40 41 42 43 44 45 46 47 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | 40 41 42 43 44 45 46 47 | 101 |
| 110 | 48 49 50 51 52 53 54 55 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | 48 49 50 51 52 53 54 55 | 110 |
| 111 | 56 57 58 59 60 61 62 63 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 | | | | | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | | | | | 56 57 58 59 60 61 62 63 | 111 |
| ADC | 1 | 0 | 1 | 2 | 4 | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | 6 0 | 6 1 | 6 2 | 6 3 | | 0 | 1 | 2 | 4 | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | 6 0 | 6 1 | 6 2 | 6 3 | 1 | ADC |
| | 0 | 6 3 | 6 2 | 6 1 | 6 0 | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | 3 | 2 | 1 | 0 | | 6 3 | 6 2 | 6 1 | 6 0 | $\bar{i} \bar{V}_1 \bar{V}_2 \bar{V}_3 \bar{V}_4$ | 3 | 2 | 1 | 0 | 0 | |
| | | Column address | | | | | | | | Column address | | | | | | | | | | | | |
| | | Chip Select (CS1B) | | | | | | | | Chip Select (CS2B) | | | | | | | | | | | | |

Figure 3. Display Data RAM



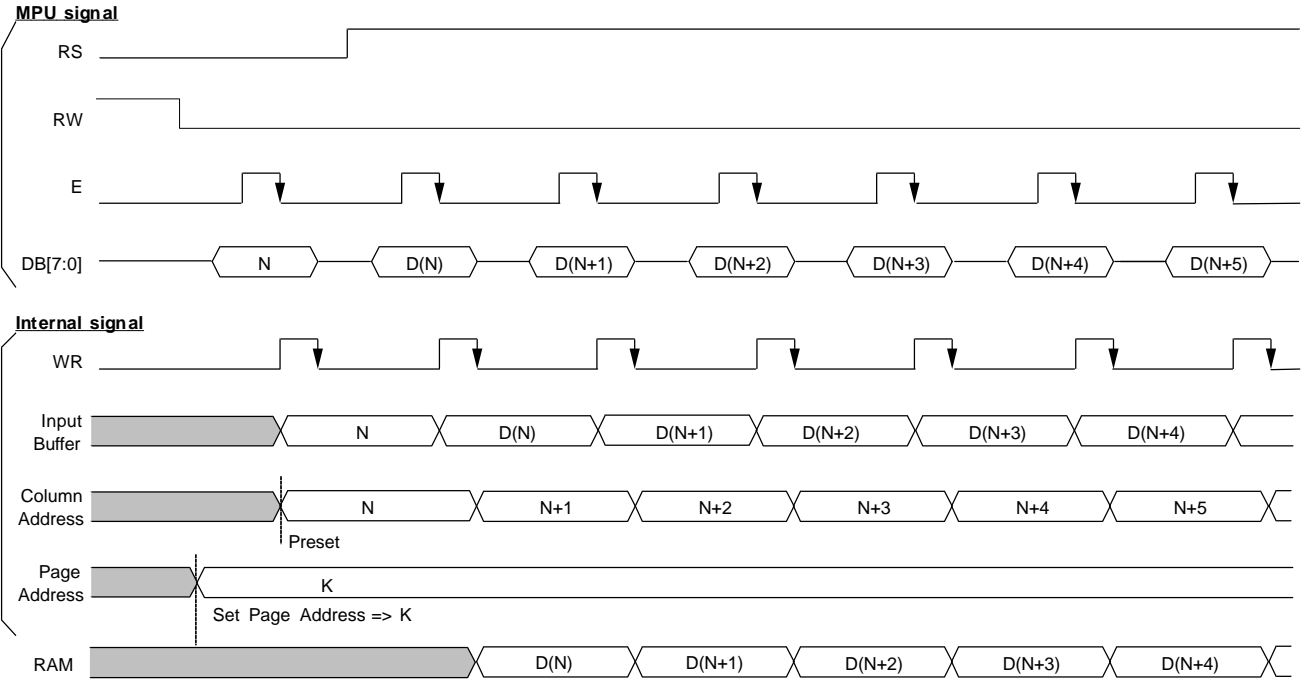


Figure 4. Write timing

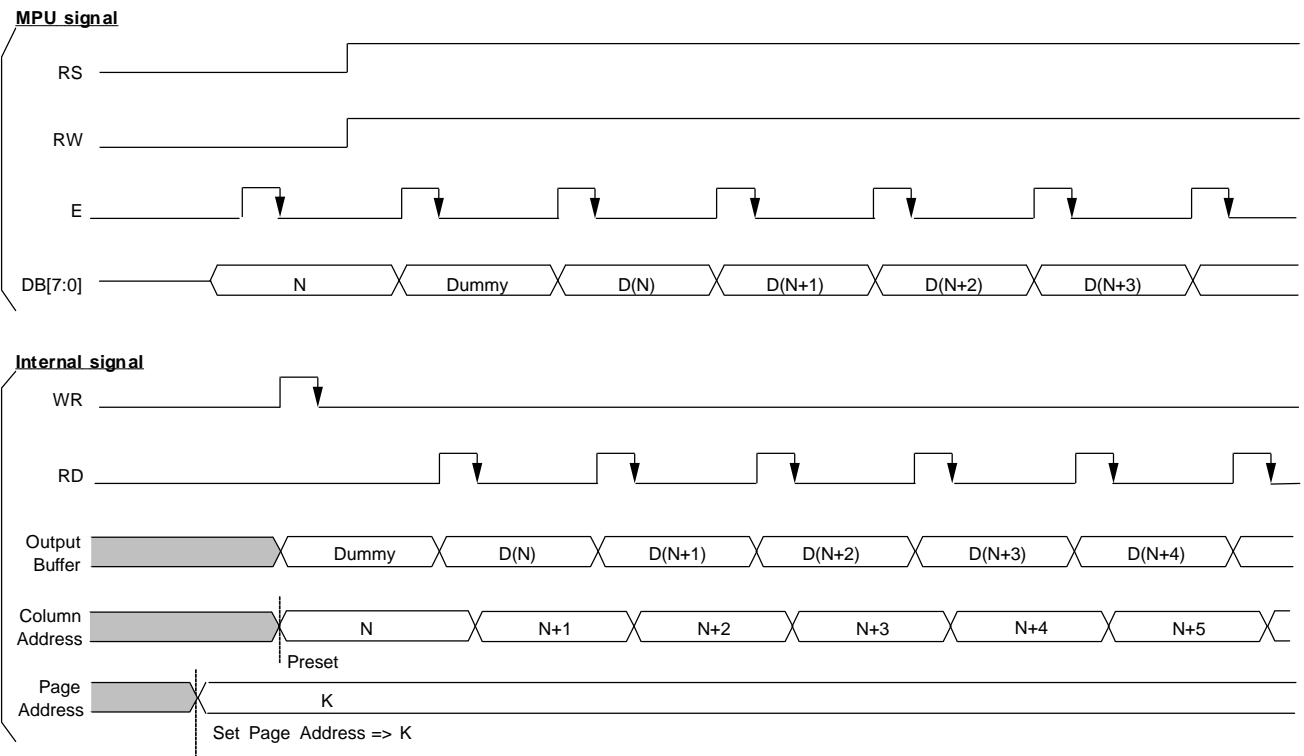


Figure 5. Read timing

Data Transfer

To match the timing of the display data RAM and registers to that of the controlling microprocessor, KS0708 uses an internal data bus and bus buffer. When the microprocessor reads the contents of display data RAM, the data for the initial read cycle is first stored in the bus buffer (dummy read cycle). On the next read cycle, the data is read from the bus buffer onto the microprocessor bus. At the same time, the next block of data is transferred from RAM to the bus buffer. Otherwise, when the microprocessor write data to display data RAM, the data is written to RAM after the falling edge of "E". Therefore, it is necessary to check Busy Flag to write or read the next data. (refer to Figure4, 5)

Page Address Register

The 3-bit Page Address register provides the page address to display data RAM (refer to Figure 3). The microprocessor issues Set Page Address instruction to change the page and to access another page.

Column Address Counter

The column address counter is a 6-bit presettable counter that provides column address to display data RAM (refer to Figure 3). It is incremented by 1 automatically after execution of each Read/Write Data instruction. The column address counter loops the values 0 to 127, and it is independent of page address register. The ADC pin is issued to change the relationship between RAM Column address and display segment output.

Display Start Line Register

The display start line register stores the line address of display data RAM that corresponds to the first (normally the top) line(COM1) of liquid crystal display(LCD) panel. See Figure 3. When displaying contents in display data RAM on the LCD panel, 6-bit data(DB[5:0]) of the Set Display Start Line is latched in display start line register. Latched data are transferred to the line address counter just before COM1 is active High, presetting the line address counter. The line counter is then incremented on the display latch clock signal once for every display line. It is used for vertical scrolling of the liquid crystal display screen.

LCD Driver

LCD driver circuit has 192 outputs of 128 segment outputs, 64 common outputs for LCD driving. Each common output has a shift register. LCD driving output voltage is determined by the combination of display data and internal AC signal.

| Display Data | Common output | Segment output |
|--------------|---------------|----------------|
| 0 | V1 | V2 |
| | V4 | V3 |
| 1 | V5 | V0 |
| | V0 | V5 |
| Display OFF | - | V2 or V3 |

Table 4. Relationship between data for each input signal and the LCD drive output.

Reset Circuit

Reset function can initialize system by setting RESETB terminal at Low level. When RESETB becomes low, following procedure occurs.

- i[©] Display start line : 0(First)
- i[©] Display ON/OFF : OFF

While RESETB is in Low level, no instruction except Status Read can be accepted. Reset status appears at DB4. Refers to Read Status of "INSTRUCTION DESCRIPTION".

The conditions of power supply at initial power up are shown in table 3.

| Item | Symbol | Min | Typ | Max | Unit |
|------------|--------------|-----|-----|-----|------|
| Reset time | t_{RESETB} | 1.0 | - | - | us |
| Rise time | tr | - | - | 200 | ns |

Table 5. Power supply initial Conditions.

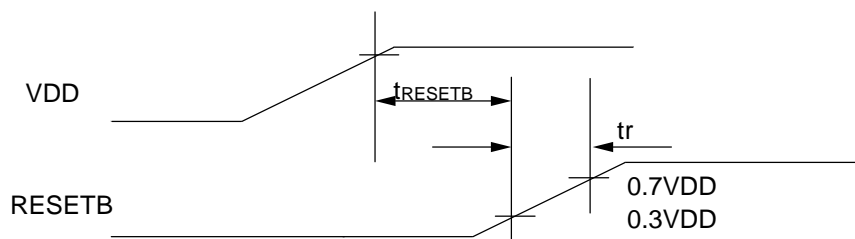


Figure 6. Reset Timing

INSTRUCTION DESCRIPTION

Instruction Table

| Instruction | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function |
|------------------------|----|----|------------|-----|------------------------------|-------|-----|--------------|-----|-----|--|
| Read display data | 1 | 1 | Read data | | | | | | | | Reads data (DB[0:7]) from display data RAM to the data bus. |
| Write display data | 1 | 0 | Write data | | | | | | | | Writes data(DB[0:7]) into display data RAM. After writing instruction, column address is incremented by 1 automatically. |
| Status Read | 0 | 1 | BUSY | 0 | ON/OFF | RESET | 0 | 0 | 0 | 0 | Reads status BUSY -0 : Ready -1 : In operation ON/OFF -0 : Display ON -1 : Display OFF RESET -0 : Normal -1 : Reset |
| Set Column Address | 0 | 0 | 0 | 1 | Column address (0 j- 63) | | | | | | Sets the Column address at the Column address counter |
| Set Display Start Line | 0 | 0 | 1 | 1 | Display Start Line (0 j- 63) | | | | | | Indicates the display data RAM displayed at the top of the screen. |
| Set Page Address | 0 | 0 | 1 | 0 | 1 | 1 | 1 | Page(0 j- 7) | | | Sets the Page address at the Page address register. |
| Display ON/OFF | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0/1 | Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON |

Instructions

Read Display Data

Reads 8-bit data from display data RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each read operation, the microprocessor can continue to read data of multiple words.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----------|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | Read data | | | | | | | |

Write Display Data

Writes 8-bit data in display data RAM. As the column address is incremented by 1 automatically after each write operation, the microprocessor can continue to write data of multiple words.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------------|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | Write data | | | | | | | |

Read Status

Indicates the internal status conditions of the device to the microprocessor.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------|-----|--------|-------|-----|-----|-----|-----|
| 0 | 1 | BUSY | 0 | ON/OFF | RESET | 0 | 0 | 0 | 0 |

| Flag | Description |
|--------|---|
| BUSY | The device is busy due to internal operation or reset. Any instruction is rejected until BUSY goes Low. |
| ON/OFF | Indicates whether the display is on or off. When goes Low, the display is on. When goes High, the display is off. This is the opposite of Display ON/OFF instruction. |
| RESET | Indicates the initialization is in progress by RESETB signal. When Low, the chip is in active. When High, the chip is being reset. |

¡á Set Page Address

Sets the page address of display RAM from the microprocessor into the page address register. Along with Column address register, Page address register assigns the address of the display RAM to be written to or read from display data. Changing the page address doesn't affect the display status.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | X2 | X1 | X0 |

| X2 | X1 | X0 | Page |
|----|----|----|------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| : | : | : | : |
| 1 | 1 | 1 | 7 |

¡á Set Column Address

Sets the Column address of display RAM from the microprocessor into the Column address register. When the microprocessor reads or writes display data to or from display RAM, the address are automatically incremented,

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 |

| Y5 | Y4 | Y3 | Y2 | Y1 | Y0 | Column address |
|----|----|----|----|----|----|----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

¡á Set Display Start Line

Sets the line address of display RAM to determine the display start line. The display data on the specified line of the display RAM is displayed at the top row COM1 of LCD panel. It is followed by the higher number of lines in ascending order corresponding to the determined duty cycle. When this instruction changes the display start line address, the LCD panel can be scrolled.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | Z5 | Z4 | Z3 | Z2 | Z1 | Z0 |

| Z5 | Z4 | Z3 | Z2 | Z1 | Z0 | Line address |
|----|----|----|----|----|----|--------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

¡á Display ON/OFF

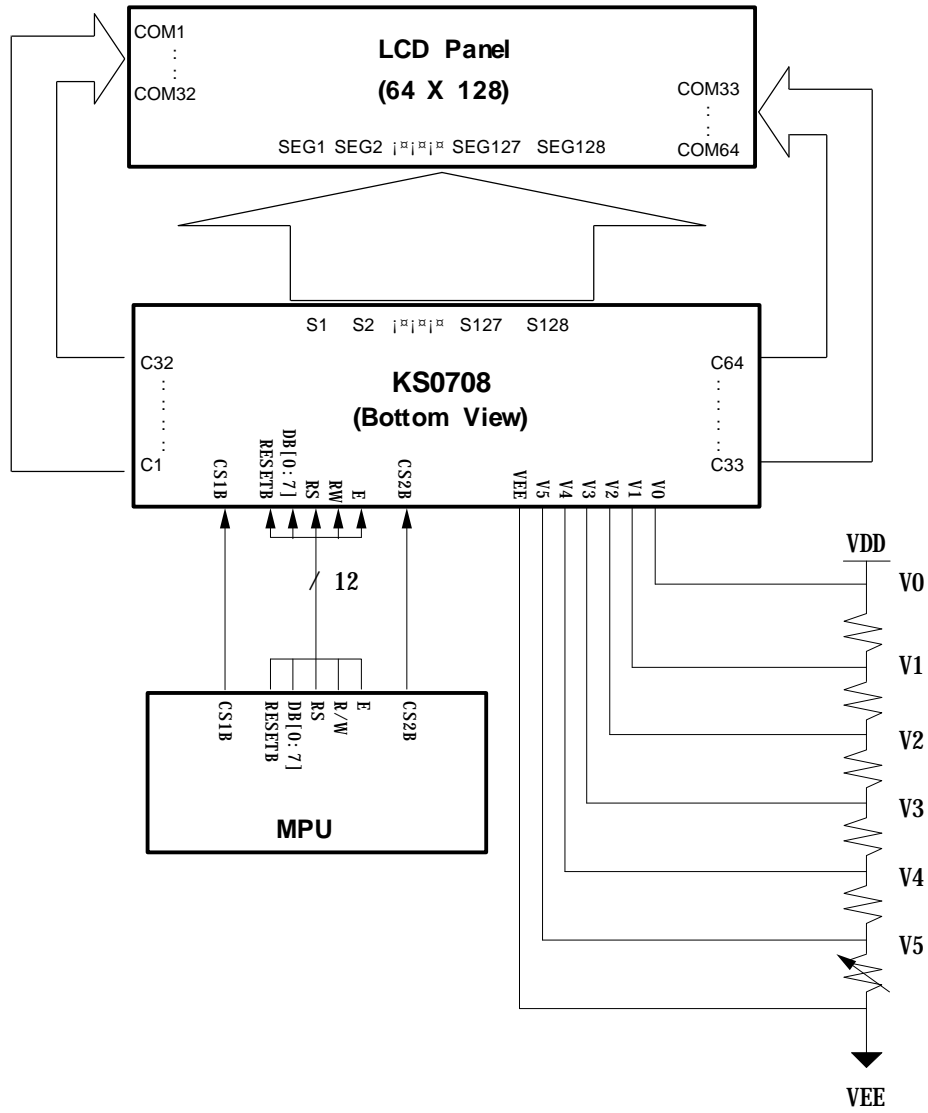
Turns the display ON or OFF.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | DO |

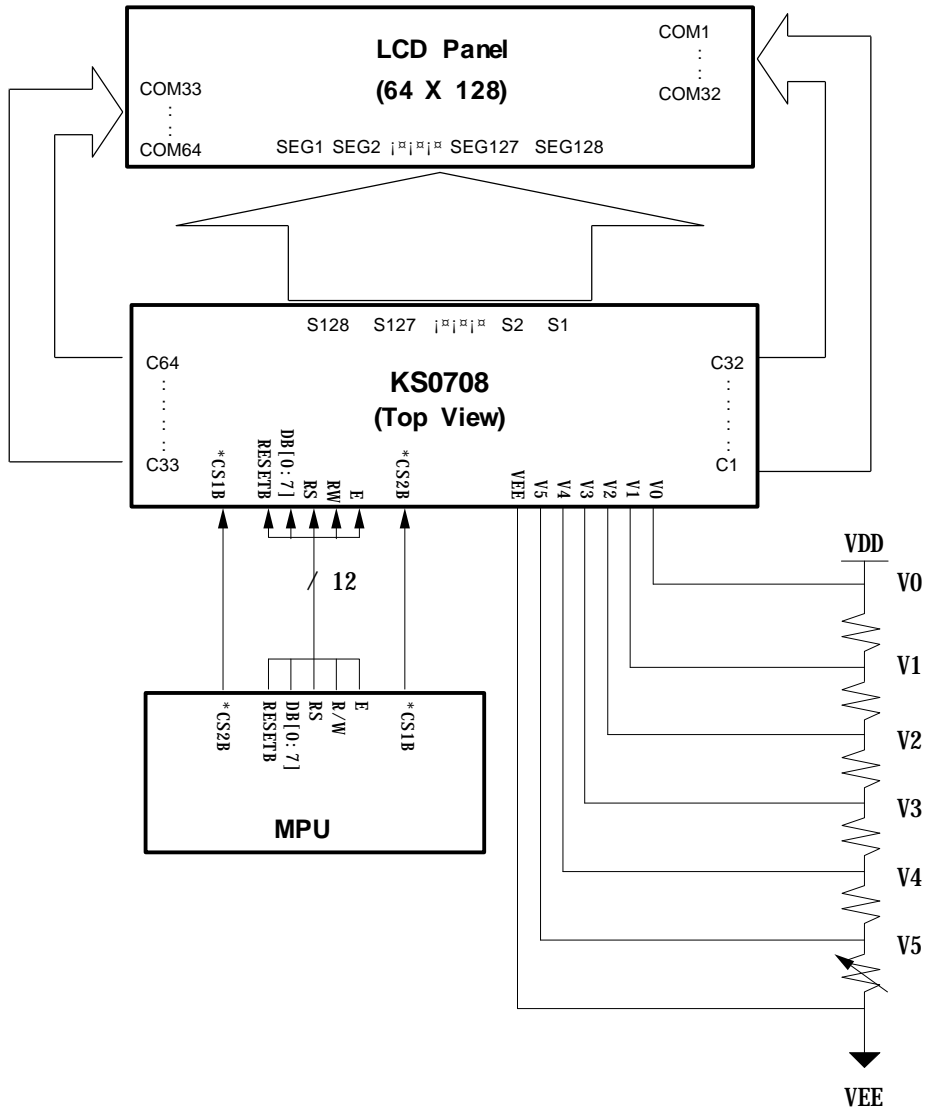
DO = 1 : Display ON

DO = 0 : Display OFF

APPLICATION DIAGRAM 1 (ADC = H, SHL = H)



APPLICATION DIAGRAM 2 (ADC = L, SHL = H)

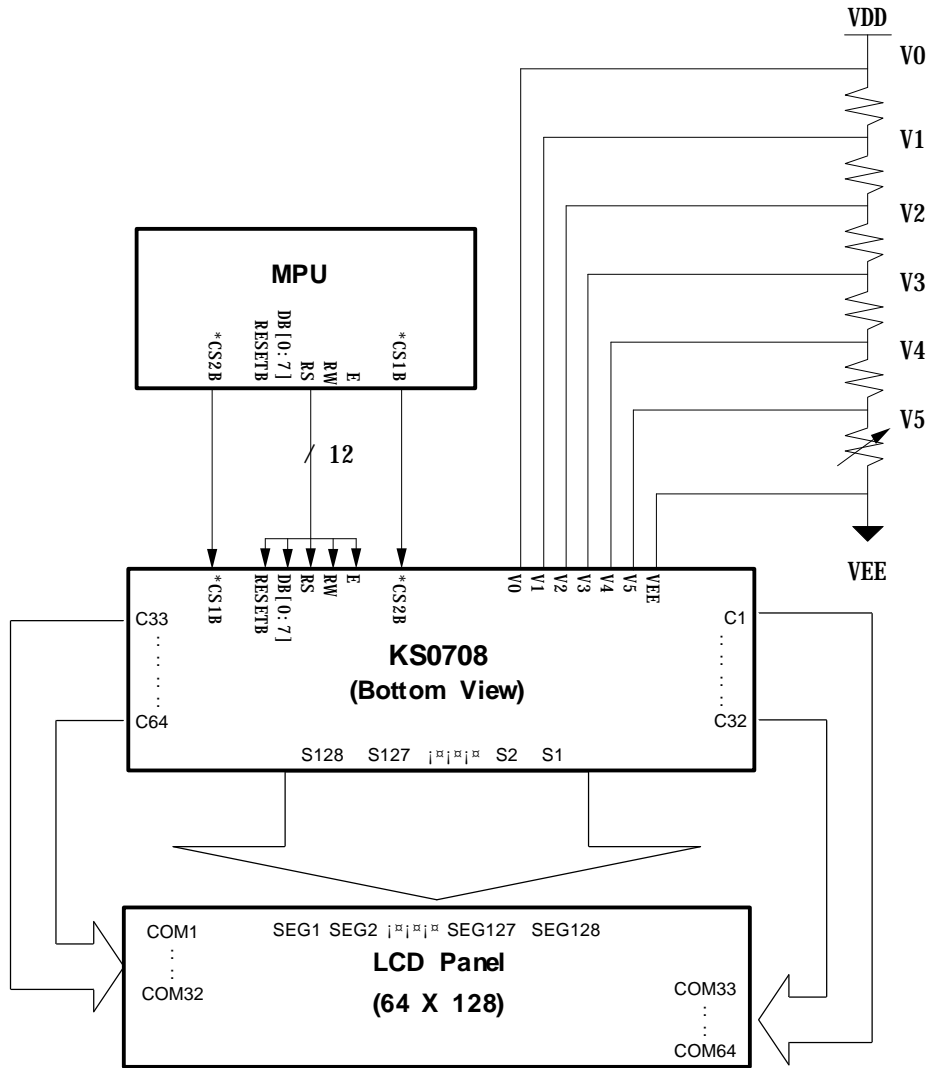


***Note**

When ADC = L, connects chip select pins(CS1B, CS2B) as following.

- CS1B(MPU) -> CS2B(KS0708)
- CS2B(MPU) -> CS1B(KS0708)

APPLICATION DIAGRAM 3 (ADC = L, SHL = L)

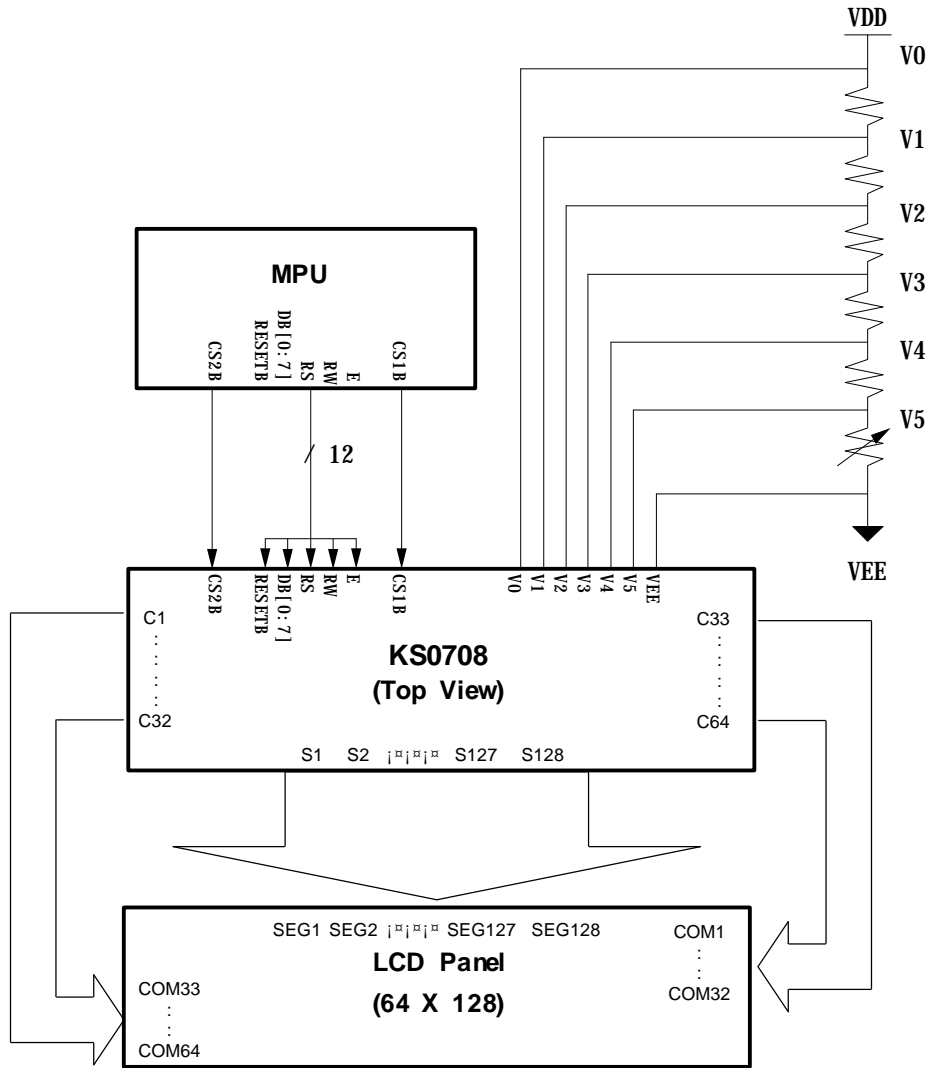


***Note**

When ADC = L, connects chip select pins(CS1B, CS2B) as following.

- CS1B(MPU) -> CS2B(KS0708)
- CS2B(MPU) -> CS1B(KS0708)

APPLICATION DIAGRAM 4 (ADC = H, SHL = L)



SPECIFICATIONS

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit | Note |
|-----------------------|------------------|--|------|-------|
| Operating voltage | V _{DD} | -0.3 ~ +7.0 | V | *1 |
| Supply Voltage | V _{EE} | V _{DD} -19.0 ~ V _{DD} +0.3 | | *4 |
| Driver Supply Voltage | V _B | -0.3 ~ V _{DD} +0.3 | | *1, 3 |
| | V _{LCD} | V _{EE} -0.3 ~ V _{DD} +0.3 | | *2 |

Note :

*1. Based on V_{SS} = 0V

*2. V_{LCD} = V_{DD} - V_{EE}

*3. Applies to SHL, FS, PCLK2, CR, RESETB, ADC, CS1B, CS2B, E, RW, RS and DB0_i-DB7.

*4. Voltage level

$$V_{DD} \text{ i}\tilde{\text{A}} V_0 \text{ i}\tilde{\text{A}} V_1 \text{ i}\tilde{\text{A}} V_2 \text{ i}\tilde{\text{A}} V_3 \text{ i}\tilde{\text{A}} V_4 \text{ i}\tilde{\text{A}} V_5 \text{ i}\tilde{\text{A}} V_{EE}$$

Temperature Characteristics

| Parameter | Symbol | Rating | Unit | Note |
|-----------------------|------------------|------------|------|------|
| Operating temperature | T _{opr} | -30 ~ +85 | °C | |
| Storage temperature | T _{stg} | -55 ~ +125 | | |

Electrical Characteristics

DC Characteristics

(VDD = 4.5~5.5V, Ta=-30~+85jÉ)

| Item | Symbol | Condition | Min | Typ | Max | Unit | Note | |
|------------------------------|--------|---|-----------------------------------|-----|--------|------|------|-----|
| Operating voltage | VDD | - | 4.5 | - | 5.5 | V | | |
| Input High Voltage | VIH1 | - | 0.7VDD | - | VDD | | *1 | |
| | VIH2 | - | 2.0 | - | VDD | | *2 | |
| Input Low Voltage | VIL1 | - | 0 | - | 0.3VDD | | *1 | |
| | VIL2 | - | 0 | - | 0.8 | | *2 | |
| Output High Voltage | VOH | IOH = -200uA | 2.4 | - | - | | *3 | |
| Output Low Voltage | VOL | IOL = 1.6mA | - | - | 0.4 | | | |
| Input Leakage Current | ILKG | VIN = VSS ~ VDD | -1.0 | - | +1.0 | uA | *4 | |
| Tri-state Leakage Current | ITSL | VIN = VSS ~ VDD | -5.0 | - | +5.0 | | *5 | |
| Driver Input Leakage Current | IDLKG | VIN = VEE ~ VDD | -10 | - | +10 | | *6 | |
| Operating Current | Idd1 | During Display | - | - | 0.8 | mA | *7 | |
| | Idd2 | During Access | - | - | 1.0 | | *8 | |
| On resistance | COM | RONC | VDD - VEE = 17V i¼LOAD = 0.1mA | - | - | 1.5 | SÜ | *9 |
| | SEG | RONS | | - | - | 7.5 | | *10 |
| Oscillation frequency | fosc | Ta=25jÉ, VDD = 5V Rf = 47SÜ i¼ 2% Cf = 20pF i¼ 5% | 315 | 450 | 585 | KHz | | |

Note :

- *1. FS, CR, ADC, SHL, PCLK2, RESETB
- *2. CS1B, CS2B, E, RW, RS, DB0 ~ DB7
- *3. DB0 ~ DB7
- *4. Excepted DB0 ~ DB7
- *5. DB0 ~ DB7 at High Impedence
- *6. V0, V1, V2, V3, V4, V5
- *7. C = 20pF, R = 47 SÜ, fosc = 450 KHz, DB0 ~ DB7 = VDD, Output = No Load
- *8. External Clock = 430 KHz, RAM Access Cycle = 1 MHz
- *9. V0 = 5V, V1 = 3.2V, V2 = 1.4V, V3 = -8.4V, V4 = -10.2V, V5 = -12V, C1 ~ C64
- *10. V0 = 5V, V1 = 3.2V, V2 = 1.4V, V3 = -8.4V, V4 = -10.2V, V5 = -12V, S1 ~ S128

AC Characteristics

(VDD = 4.5 to 5.5V, Ta = -30 to +85°C)

| Mbde | Item | Symbol | Min | Typ | Max | Unit |
|--------------------------------------|---------------------------|-----------------|------|-----|-----|------|
| Write Mbde (Refer to Figure 7) | E Cycle Time | tc | 1000 | - | - | μs |
| | E Rise / Fall Time | tr, tf | - | - | 25 | |
| | E Pulse Width (High, Low) | tw | 450 | - | - | |
| | RW and RS Setup Time | tsu1 | 140 | - | - | |
| | RW and RS Hold Time | th1 | 10 | - | - | |
| | Data Setup Time | tsu2 | 200 | - | - | |
| | Data Hold Time | th2 | 10 | - | - | |
| Read Mbde (Refer to Figure 8) | E Cycle Time | tc | 1000 | - | - | μs |
| | E Rise / Fall Time | tr, tf | - | - | 25 | |
| | E Pulse Width (High, Low) | tw | 450 | - | - | |
| | RW and RS Setup Time | tsu | 140 | - | - | |
| | RW and RS Hold Time | th | 10 | - | - | |
| | Data Output Delay Time | t _D | - | - | 320 | |
| | Data Hold Time | t _{DH} | 20 | - | - | |

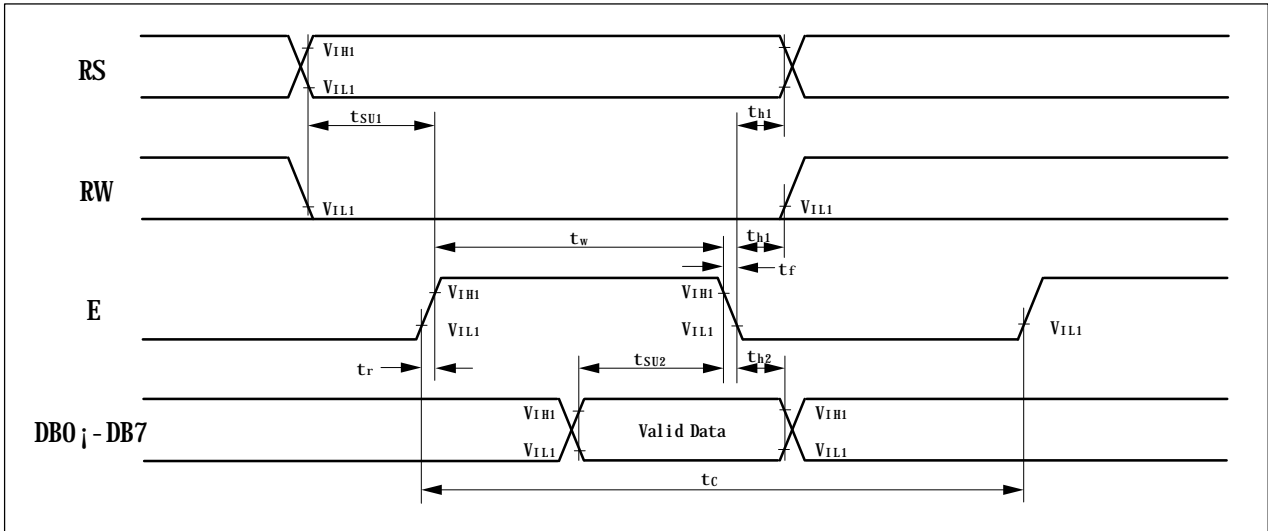


Figure 7. Write Mode Timing Diagram

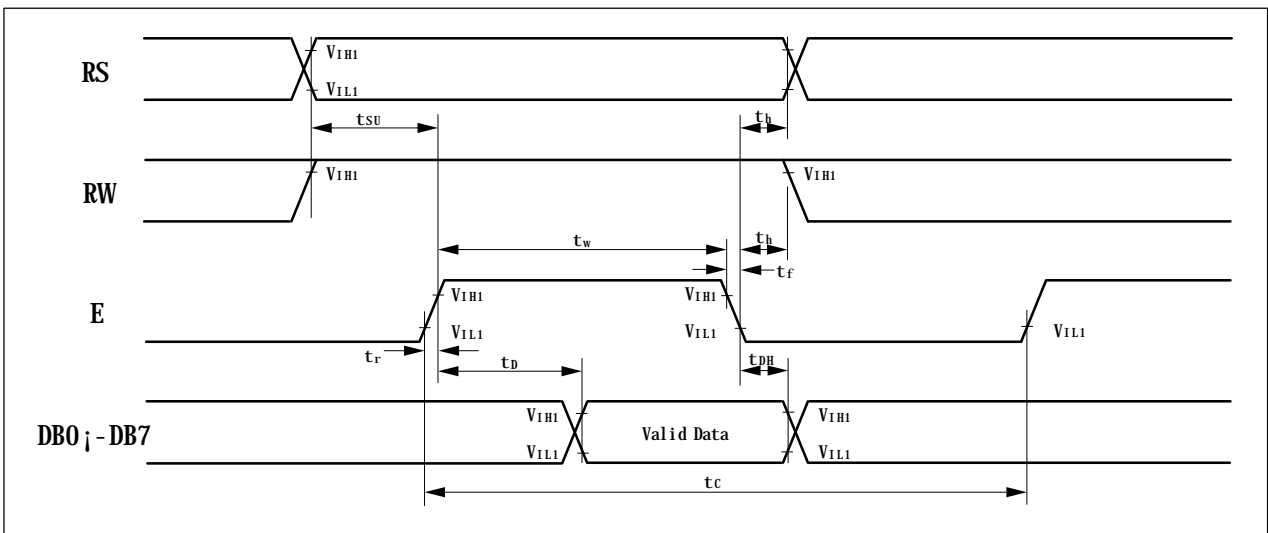


Figure 8. Read Mode Timing Diagram