

ON SCREEN DISPLAY PROCESSOR

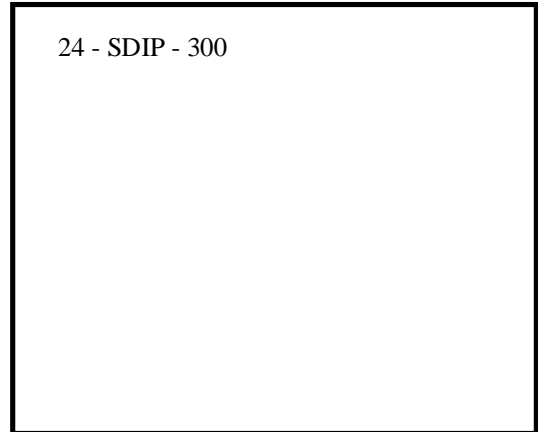
The KS5516 is a BICMOS LSI with on screen display function, sync separator & expander function.

FUNCTIONS

- On screen display
- Sync separator and sync detector
- General expander

FEATURES

- Character capacity : 240 (24 column × 10 row)
- Construction of character : 12 × 18 dots
- 128 kinds of character
- Display position : 62 horizontal position
: 64 vertical position
- Character size : 4 × 4 times of normal
- Blinking : character unit
- Background coloring : 8 colors
- Synchronous ways : automatic selection internal
or external synchronization
- General output : 4 bit (by serial data)
- Built-in sync separator & sync detector
- Built-in 4 fsc oscillation circuit
- NTSC / PAL / SECAM mode
- Clamp circuit



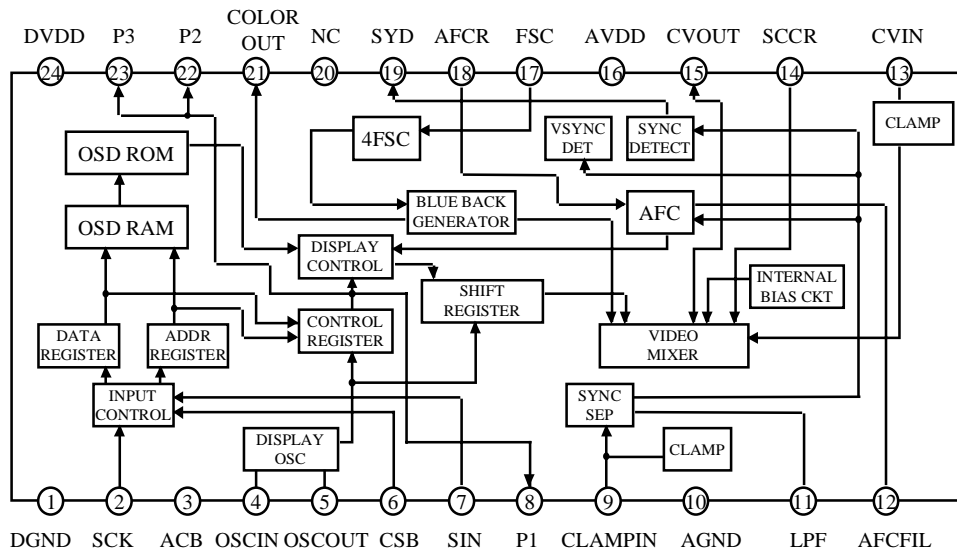
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5516-XX	24-SDIP-300	- 20°C ~ +70°C

OPTION CODE INFORMATION

Code No.	Remark
- 01	English, Russian
- 04	Chinese
- 08	Arabian

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
1	DGND	-	Digital Ground
2	SCK	I	Serial clock input. When CSB pin is $\bar{0}$ then serial data is inputted by micom. Hysterisis input.
3	ACB	I	Auto clear pin. If $\bar{0}$ then all circuits are reset. Built-in pull up resistor. Hysterisis input.
4	OSCIN	I	LC oscillation pin. Standard frequency is 7MHz & the horizontal start position is controlled by the clock of oscillation block.
5	OSCOUT	O	
6	CSB	I	While pin 6 is low, serial data input is active. Built - in pull up resistor
7	SIN	I	Serial data input pin. Built-in pull up resistor
8	P1	P	General output port 1
9	CLAMPIN	I	Clamp input pin of composite video signal
10	AGND	-	Analog ground
11	LPF	-	Low pass filter
12	AFCFIL	-	AFC filter output
13	CVIN	I	Composite video signal input
14	SCCR	I	SECAM chroma input
15	CVOUT	O	Composite video output : 2 Vp-p
16	AVDD	-	Analog VDD
17	FSC	I	FSC input
18	AFCR	I	VCO oscillation frequency control
19	SYD	O	When sync signal is inputted, then SYD is high.

PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Function
20	NC	-	No connection
21	COLOR OUT	O	Blueback color signal output
22	P2	O	General output port 2
23	P3	O	General output port 3
24	DVDD	-	Digital VDD

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD	- 0.3 ~ 6.0	V
Input Voltage	VIN	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$ 300	V
Power Dissipation	PD	- 20 ~ + 70	mW
Operating Temperature	Topr	- 40 ~ + 125	°C
Storage Temperature	Tstg		°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, AVDD = DVDD = 5V)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	DVDD	4.5	5.0	5.5	V
Operating Voltage	AVDD	4.5	5.0	5.5	V
Operating Current	Icc	10	18	25	mA
Pin 12 DC Voltage	Vpi2	2.25	2.5	2.75	V
Pin 13 DC Voltage	Vpi3	1.3	1.45	1.6	V
AFC Freerun Frequency	Ffr	15.5	15.7	15.9	KHz
AFC Pulse Width	twd	3.7	4.0	4.3	usec
AFC Delay Time	td	1.0	2.5	4.0	usec
AFC Lock Range H	Falh	+600	-	-	Hz
AFC Lock Range L	Fall	-	-	-900	Hz
AFC Capture Range H	Fach	+400	-	-	Hz
AFC Capture Range L	Fac1	-	-	-700	Hz
SYNC DET. Lock Range H	Flh	143	153	163	KHz
SYNC DET. Lock Range L	Fll	6.7	7.7	8.7	KHz
SYNC DET. Capture Range H	Fch	100	107	114	KHz
SYNC DET. Capture Range L	Fcl	14.3	15.3	16.3	KHz
V-SYNC Delay Time	tvd	10	14	-	usec
Oscillation Level	Vosc	3.0	3.5	4.0	Vpp
Oscillation Frequency	Fosc	6.3	7.0	7.7	MHz
Blueback Sync Tip Level	Vbst	1.1	1.3	1.5	V
Blueback Pedestal Level	Vbpd	1.75	1.95	2.15	V
Blueback Color Burst Level H	Vbbh	2.0	2.2	2.4	V
Blueback Color Level H	Vbch	2.55	2.75	2.95	V
Fsc Input Level	VFSC	1.2	1.5	2.0	Vpp

OPERATION DESCRIPTION

MEMORY STRUCTURE

After recording the serial data from μ -COM to RAM and control register, it is need by H-sync and V sync that detecting from composite video signal, and then mix the character data of ROM to composite video signal.

When composite video signal is input, KS5516 outputs the blueback signal by divide and mixture the 4 fsc signal.

The following table is data structure from MICOM.

- Memory address consists of 16 bit
- The data of address 0 - 239 is character data which is display on the screen.
- The address 240 - 244 is the control register
- The upper 4 bit don't care bit

Bit Addr	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	0	0	0	0	P	CH2	CH1	CH0	BLI	C6	C5	C4	C3	C2	C1	C0
.
239	0	0	0	0	P	CH2	CH1	CH0	BLI	C6	C5	C4	C3	C2	C1	C0
240	0	0	0	0	P	INT/ NON	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0
241	0	0	0	0	P	BLI2	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0
242	0	0	0	0	P	DSP 3	DSP 2	DSP 1	RAM ERS	TEST	TC	LEV 1	LEV 0	PH2	PH1	PH0
243	0	0	0	0	P	-	LE BK	LE CHA	DSP ON	BLK 1	BLK 0	BLI 1	BLI 0	EX	YM	BCO
244	0	0	0	0	P	SECAM	NT/ PAL	-	PD3	PD2	-	PD0	PC3	PC2	PC1	PC0

CONTROL REGISTER

1) Register 240

DA0 ~ DAA	Register	Content		Remark																	
		State	Function																		
0	HP0	0	HS is horizontal display start position $HS = Tc * \{ 4 * \sum_{n=0}^5 (HPn * 2^n) + N \}$	Horizontal Start Position																	
		1																			
1	HP1	0	Tc : osc. period (1/7MHz = 143 nsec)																		
		1																			
2	HP2	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>HSZ11</td> <td>HSZ10</td> <td rowspan="2">N</td> </tr> <tr> <td>HSZ21</td> <td>HSZ20</td> </tr> <tr> <td>0</td> <td>0</td> <td>9</td> </tr> <tr> <td>0</td> <td>1</td> <td>10</td> </tr> <tr> <td>1</td> <td>0</td> <td>11</td> </tr> <tr> <td>1</td> <td>1</td> <td>12</td> </tr> </table>		HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	9	0	1	10	1	0	11	1	1	12
		HSZ11			HSZ10	N															
HSZ21	HSZ20																				
0	0	9																			
0	1	10																			
1	0	11																			
1	1	12																			
3	HP3	0																			
		1																			
4	HP4	0																			
		1																			
5	HP5	0																			
		1																			
6	HSZ10	0	1뿔t line	1뿔t line character size control to horizontal-direction																	
		1																			
7	HSZ11	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>HSZ10</td> <td>0</td> <td>1</td> </tr> <tr> <td>HSZ11</td> <td>0</td> <td>1X</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>		HSZ10	0	1	HSZ11	0	1X	0	1X	2X	1	3X	4X					
		HSZ10			0	1															
HSZ11	0	1X																			
0	1X	2X																			
1	3X	4X																			
8	HSZ20	0	2nd ~ 10th line		2nd ~ 10th line character size control to horizontal-direction																
		1																			
9	HSZ21	0	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>HSZ20</td> <td>0</td> <td>1</td> </tr> <tr> <td>HSZ21</td> <td>0</td> <td>1X</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>			HSZ20	0	1	HSZ21	0	1X	0	1X	2X	1	3X	4X				
		HSZ20		0		1															
HSZ21	0	1X																			
0	1X	2X																			
1	3X	4X																			
A	INT/ NON	0	Interlace Mode	—																	
		1	Non-interlace Mode																		

2) Register 241

DA0 ~ DAA	Register	Content		Remark									
		State	Function										
0	VP0	0	VS is vertical start position $VS = H * \{ 4 * \sum_{n=0}^5 (VPn * 2^n) + 3 \}$ H : horizontal synchronous pulse time 	Vertical Start Position									
		1											
1	VP1	0											
		1											
2	VP2	0											
		1											
3	VP3	0											
		1											
4	VP4	0											
		1											
5	VP5	0											
		1											
6	VSZ10	0	<table border="1"> <tr> <td>VSZ11 \ VSZ10</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>	VSZ11 \ VSZ10	0	1	0	1X	2X	1	3X	4X	1st line character size control to vertical direction
		VSZ11 \ VSZ10		0	1								
0	1X	2X											
1	3X	4X											
1													
7	VSZ11	0											
		1											
8	VSZ20	0	<table border="1"> <tr> <td>VSZ21 \ VSZ20</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1X</td> <td>2X</td> </tr> <tr> <td>1</td> <td>3X</td> <td>4X</td> </tr> </table>	VSZ21 \ VSZ20	0	1	0	1X	2X	1	3X	4X	2nd ~ 10th line character size control to vertical direction
		VSZ21 \ VSZ20		0	1								
0	1X	2X											
1	3X	4X											
1													
9	VSZ21	0											
		1											
A	BLI2	0	V - SYNC 64 divide (= 1 sec)	Control the blink period									
		1	V - SYNC 32 divide (= 0.5 sec)										

3) Register 242

DA0 ~ DAA	Register	Content			Remark																
		State	Function																		
0	PH0	0	<table border="1"> <tr> <td>P2 P1 P0</td> <td>NTSC</td> <td>PAL</td> </tr> <tr> <td>0 0 0</td> <td>black</td> <td>black</td> </tr> </table>			P2 P1 P0	NTSC	PAL	0 0 0	black	black	Back ground color control bit									
		P2 P1 P0				NTSC	PAL														
0 0 0	black	black																			
1	0 0 1	$\pi/2$	$\pi/2$																		
1	PH1	0	<table border="1"> <tr> <td>P2 P1 P0</td> <td>NTSC</td> <td>PAL</td> </tr> <tr> <td>0 1 0</td> <td>$7\pi/4$</td> <td>$+\pi/4$</td> </tr> <tr> <td>0 1 1</td> <td>0</td> <td>0</td> </tr> </table>			P2 P1 P0	NTSC	PAL	0 1 0	$7\pi/4$	$+\pi/4$	0 1 1	0	0	Back ground color control bit						
		P2 P1 P0				NTSC	PAL														
0 1 0	$7\pi/4$	$+\pi/4$																			
0 1 1	0	0																			
1	0 1 1	0	0																		
2	PH2	0	<table border="1"> <tr> <td>P2 P1 P0</td> <td>NTSC</td> <td>PAL</td> </tr> <tr> <td>1 0 0</td> <td>π</td> <td>$\pm\pi$</td> </tr> <tr> <td>1 0 1</td> <td>$3\pi/4$</td> <td>$3\pi/4$</td> </tr> <tr> <td>1 1 0</td> <td>$3\pi/2$</td> <td>$3\pi/2$</td> </tr> <tr> <td>1 1 1</td> <td>white</td> <td>white</td> </tr> </table>			P2 P1 P0	NTSC	PAL	1 0 0	π	$\pm\pi$	1 0 1	$3\pi/4$	$3\pi/4$	1 1 0	$3\pi/2$	$3\pi/2$	1 1 1	white	white	Back ground color control bit
		P2 P1 P0				NTSC	PAL														
1 0 0	π	$\pm\pi$																			
1 0 1	$3\pi/4$	$3\pi/4$																			
1 1 0	$3\pi/2$	$3\pi/2$																			
1 1 1	white	white																			
1	1 0 1	$3\pi/4$	$3\pi/4$																		
3	LEVEL0	0	<table border="1"> <tr> <td>level 0 \ level 1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Internal bias 1</td> <td>Internal bias 2</td> </tr> <tr> <td>1</td> <td>-</td> <td>Internal bias 3</td> </tr> </table>			level 0 \ level 1	0	1	0	Internal bias 1	Internal bias 2	1	-	Internal bias 3	Color level control						
		level 0 \ level 1				0	1														
0	Internal bias 1	Internal bias 2																			
1	-	Internal bias 3																			
1	1	-	Internal bias 3																		
4	LEVEL1	0	<table border="1"> <tr> <td>level 0 \ level 1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Internal bias 1</td> <td>Internal bias 2</td> </tr> <tr> <td>1</td> <td>-</td> <td>Internal bias 3</td> </tr> </table>			level 0 \ level 1	0	1	0	Internal bias 1	Internal bias 2	1	-	Internal bias 3	Color level control						
		level 0 \ level 1				0	1														
0	Internal bias 1	Internal bias 2																			
1	-	Internal bias 3																			
1	1	-	Internal bias 3																		
5	TC	0	1H = 454Tc Tc = 2fosc																		
		1	1H = 455Tc																		
6	TEST	0	Active mode																		
		1	Test mode																		
7	RAM ERS	0	RAM no erase																		
		1	RAM erase																		
8	DSP1	0	Display method of the 1월t is fixed by BLK0 & BLK1																		
		1	Display method of the 1월t is vriable																		
9	DSP2	0	Display method of 2nd - 9th is fixed by BLK0 & BLK1																		
		1	Display method of 2nd - 9th is variable																		
A	DSP3	0	Display method of 10 th is fixed by BLK0 & BLK1																		
		1	Display method of 10 th is variable																		

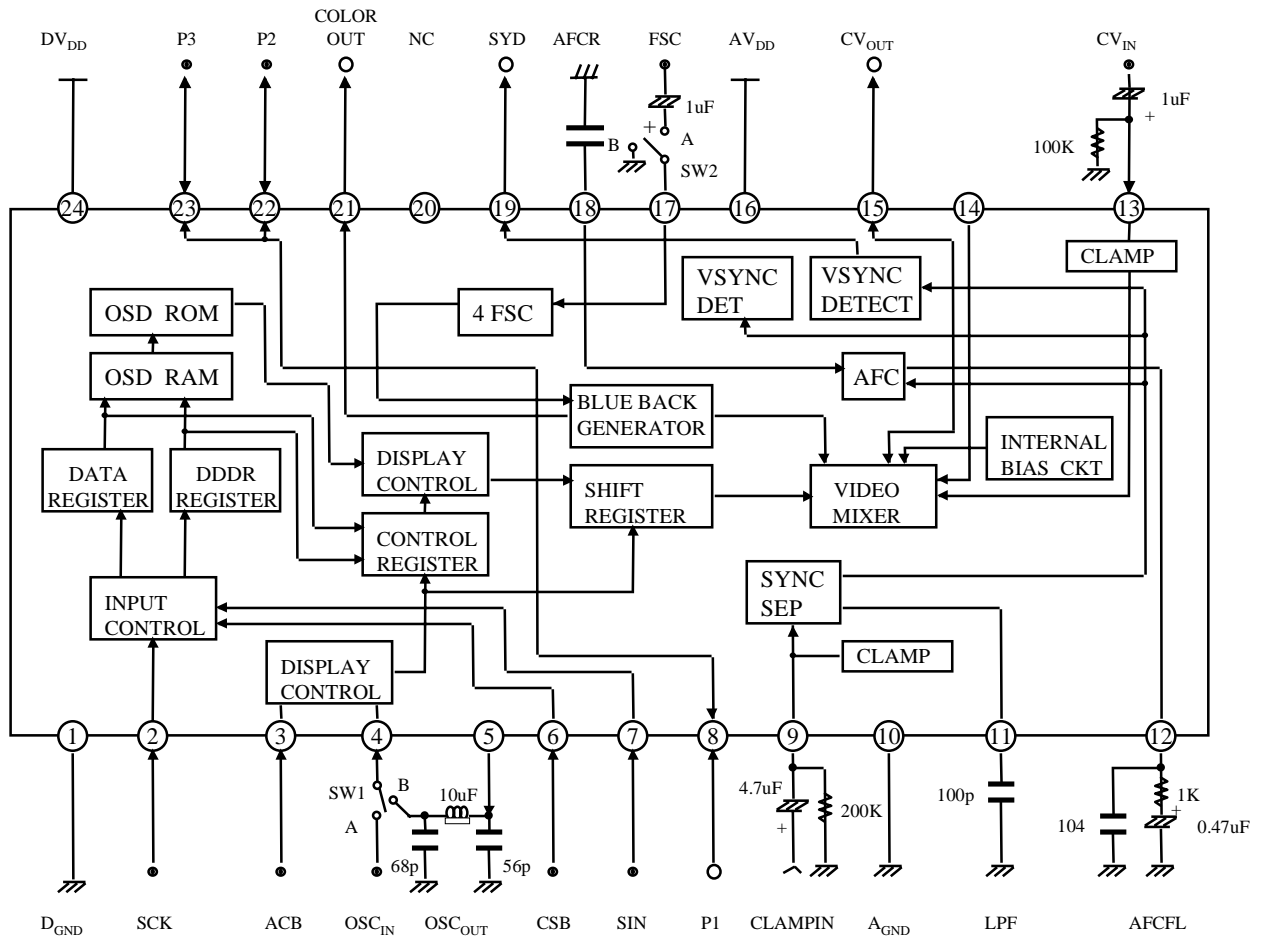
4) Register 243

DA0 ~ DAA	Register	Content		Remark									
		State	Function										
0	BCO	0	Blanking area coloring	Determined by BLK0 & BLK1									
		1	Full TV screen coloring										
1	YM	0	The same character and back ground	Determined BYBCO, BLK0 & BLK1									
		1	Variable back available										
2	EX	0	External mode available	-									
		1	Internal mode available										
3	BLI0	0	Blinking mode control <table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>BLI0 \ BLI1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>OFF</td> <td>DUTY 25%</td> </tr> <tr> <td>1</td> <td>DUTY 50%</td> <td>DUTY 75%</td> </tr> </table>	BLI0 \ BLI1	0	1	0	OFF	DUTY 25%	1	DUTY 50%	DUTY 75%	Blinking duty control
BLI0 \ BLI1	0	1											
0	OFF	DUTY 25%											
1	DUTY 50%	DUTY 75%											
4	BLI1	0											
		1											
5	BLK0	0	Blinking mode control <table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>BLI0 \ BLI1</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>OFF</td> <td>C</td> </tr> <tr> <td>1</td> <td>O</td> <td>R</td> </tr> </table>	BLI0 \ BLI1	0	1	0	OFF	C	1	O	R	C : character O : outline R : raster
BLI0 \ BLI1	0	1											
0	OFF	C											
1	O	R											
6	BLK1	0											
		1											
7	DSP ON	0	Display off										
		1	Display on										
8	LECHA	0	Character luminance level 1										
		1	Character luminance level 2										
9	LEBK	0	Blank luminance level 1										
		1	Blank luminance level 2										
A	-	0	-										
		1	-										

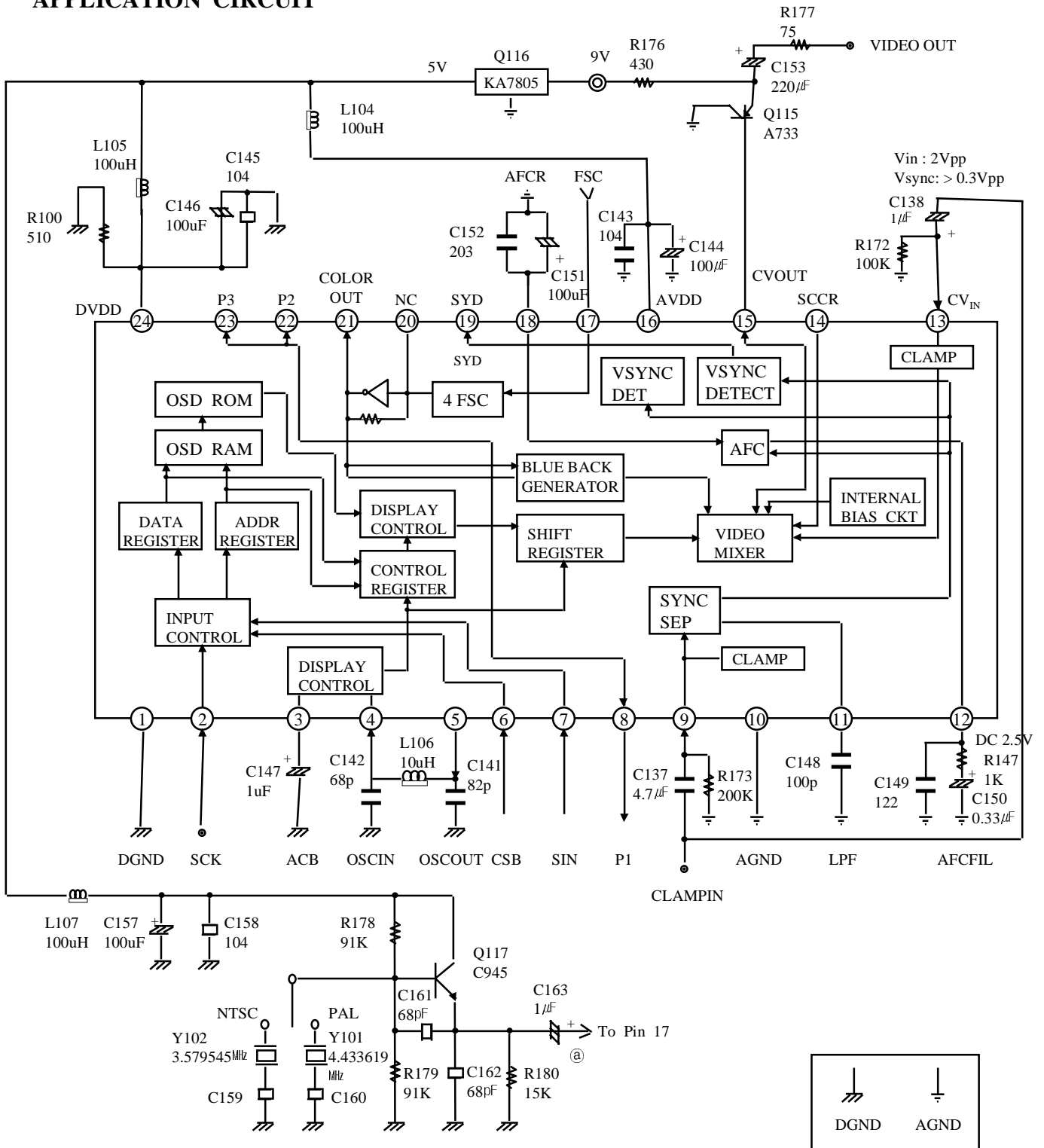
5) Register 244

DA0 ~ DAA	Register	Content			Remark									
		State	Function											
0	PC0	0	<table border="1"> <tr> <td>PC1 \ PC0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Hsync/Vsync output</td> <td>-</td> </tr> <tr> <td>1</td> <td>Port output</td> <td>CH1 output</td> </tr> </table>		PC1 \ PC0	0	1	0	Hsync/Vsync output	-	1	Port output	CH1 output	Pin 8 output mode setting
		PC1 \ PC0			0	1								
0	Hsync/Vsync output	-												
1	Port output	CH1 output												
1														
1	PC1	0	<table border="1"> <tr> <td>PC3 \ PC2</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Hsync/Vsync output</td> <td>Test mode</td> </tr> <tr> <td>1</td> <td>Port output</td> <td>CH2, BLI2 output</td> </tr> </table>		PC3 \ PC2	0	1	0	Hsync/Vsync output	Test mode	1	Port output	CH2, BLI2 output	Pin 22/23 output mode setting
		PC3 \ PC2			0	1								
0	Hsync/Vsync output	Test mode												
1	Port output	CH2, BLI2 output												
1														
2	PC2	0	<table border="1"> <tr> <td>PC3 \ PC2</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Hsync/Vsync output</td> <td>Test mode</td> </tr> <tr> <td>1</td> <td>Port output</td> <td>CH2, BLI2 output</td> </tr> </table>		PC3 \ PC2	0	1	0	Hsync/Vsync output	Test mode	1	Port output	CH2, BLI2 output	Pin 22/23 output mode setting
		PC3 \ PC2			0	1								
0	Hsync/Vsync output	Test mode												
1	Port output	CH2, BLI2 output												
1														
3	PC3	0	<table border="1"> <tr> <td>PC3 \ PC2</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>Hsync/Vsync output</td> <td>Test mode</td> </tr> <tr> <td>1</td> <td>Port output</td> <td>CH2, BLI2 output</td> </tr> </table>		PC3 \ PC2	0	1	0	Hsync/Vsync output	Test mode	1	Port output	CH2, BLI2 output	Pin 22/23 output mode setting
		PC3 \ PC2			0	1								
0	Hsync/Vsync output	Test mode												
1	Port output	CH2, BLI2 output												
1														
4	PD0	0	L output		Pin 8 output data setting									
		1	H output											
5	-	0	-		-									
		1	-											
6	PD2	0	L output		Pin 22 output data setting									
		1	H output											
7	PD3	0	L output		Pin 23 output data setting									
		1	H output											
8	-	0	-											
		1	-											
9	NT/ PAL	0	NTSC mode											
		1	PAL mode											
A	SECAM	0	NTSC or PAL mode											
		1	SECAM mode											

TEST CIRCUIT



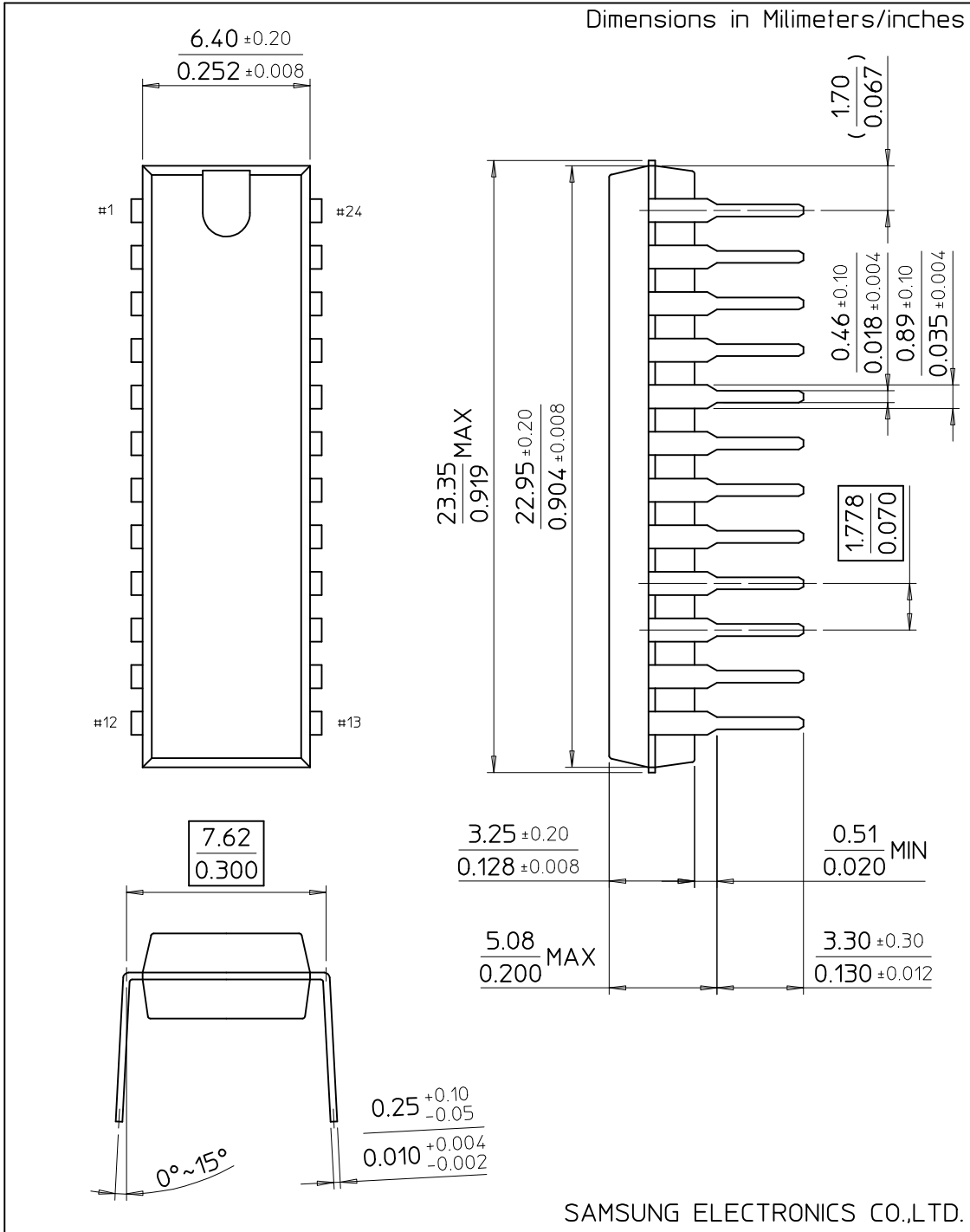
APPLICATION CIRCUIT



The circuit drawn above is for Demo Board.

- fsc X-TAL → NTSC : 3.579545MHz(Y102)
PAL : 4.433619MHz (Y101)
- C159 / C160 : The load Capacitor of X-TAL Y101/Y102 has a difference each according to its manufacturer.

24-SDIP-300



SAMSUNG ELECTRONICS CO.,LTD.