1 PRODUCT OVERVIEW

The KS57C0404/C0408 single-chip CMOS microcontroller has been designed for very high-performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

The KS57P0408 is the microcontroller which has 8K-bytes one-time-programmable ROM and the functions are same to KS57C0404/C0408.

With two 8-bit timer/counters, an 8-bit serial I/O interface, and eight software n-channel open-drain I/O pins, the KS57C0404/C0408 offers an excellent design solution for a wide variety of general-purpose applications.

Up to 36 pins of the 42-pin SDIP or 44-pin QFP package can be dedicated to I/O. Seven vectored interrupts provide fast response to internal and external events.

In addition, the KS57C0404/C0408's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

FEATURES SUMMARY

Memory

- 512 × 4-bit RAM
- 4096 × 8-bit ROM: KS57C0404
- 8192 × 8-bit ROM: KS57C0408

36 I/O Pins

- Input only: 4 pins
- I/O: 24 pins
- N-channel open-drain I/O: 8 pins

Memory-Mapped I/O Structure

- Data memory bank 15

8-Bit Basic Timer

- 4 interval timer functions

Two 8-Bit Timer/Counters

- Programmable interval timer
- External event counter function
- Timer/counters clock outputs to TCLO0 and TCLO1 pins

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 4.19 MHz
- 4 frequency outputs to the BUZ pin

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Interrupts

- 3 external interrupt vectors
- 4 internal interrupt vectors
- 2 quasi-interrupts

Power-Down Modes

- Idle: Only CPU clock stops
- Stop: System clock stops

Oscillation Sources

- Crystal or Ceramic for system clock
- Oscillation frequency : 0.4 – 6.0MHz
- CPU clock divider circuit (by 4. 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 0.67, 1.33, 10.7 µs at 6.0 MHz

Operating Temperature

- - 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V (Main)
- 2.0 V to 5.5 V (OTP)

Package Types

- 42-pin SDIP, 44-pin QFP

BLOCK DIAGRAM

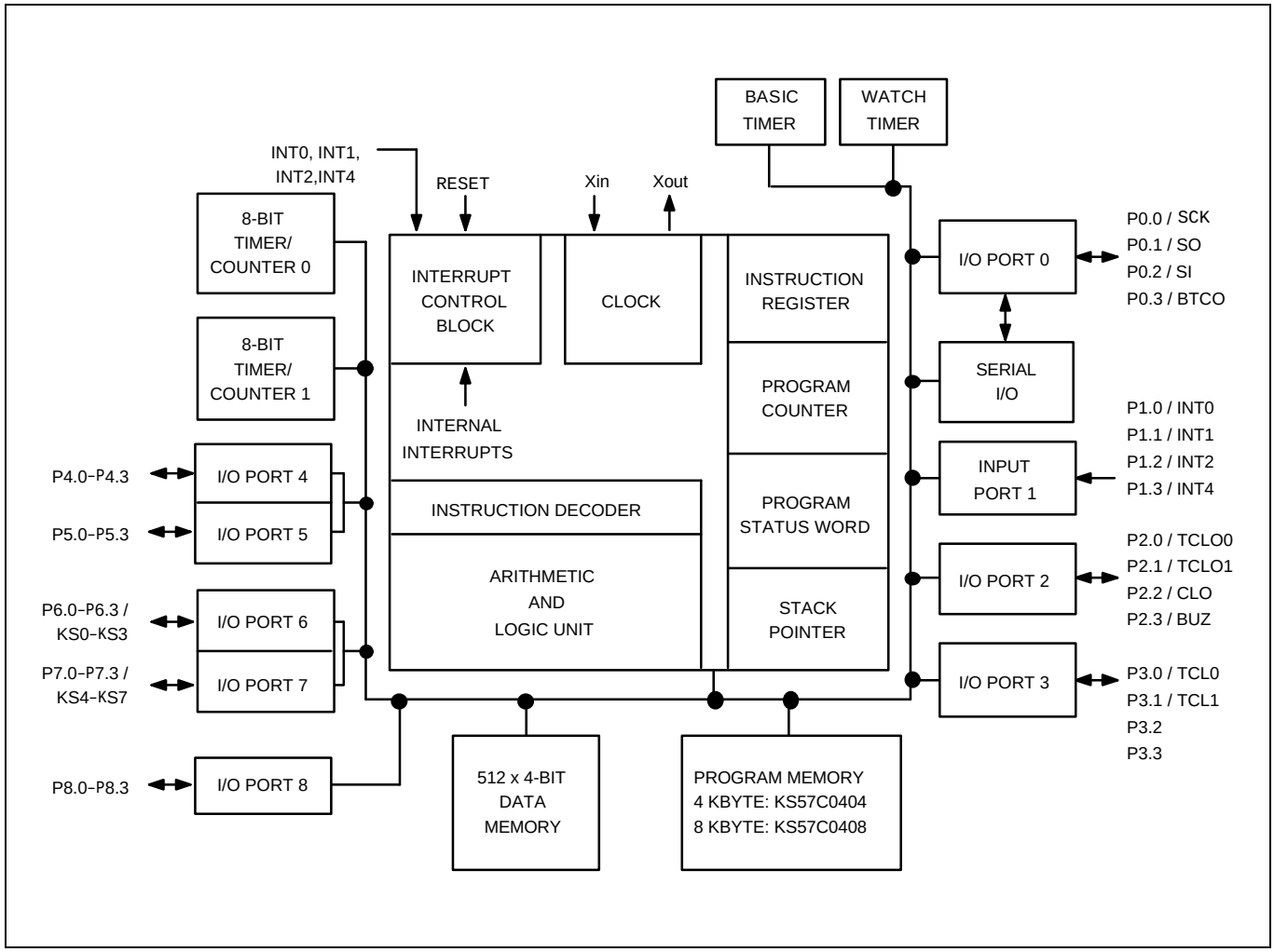

Figure 1–1. KS57C0404/C0408/P0408 Block Diagram

PIN ASSIGNMENTS

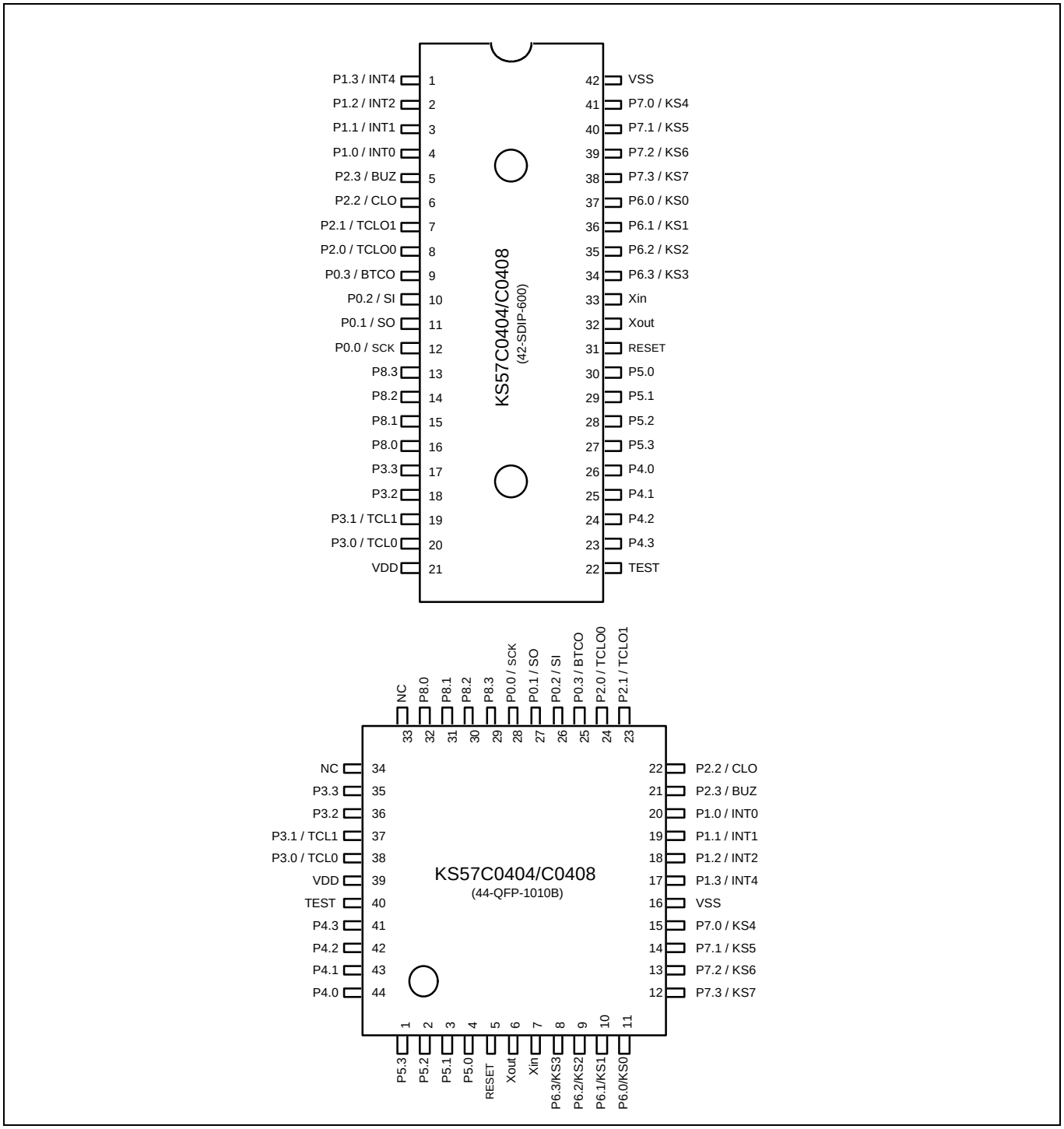

Figure 1–2. KS57C0404/C0408 Pin Assignment Diagrams

PIN DESCRIPTI/ONS

Table 1–1. KS57C0404/C0408/P0408 Pin Description

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	12 (28) 11 (27) 10 (26) 9 (25)	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are assignable by software to pins P1.0, P1.1, and P1.2.	4 (20) 3 (19) 2 (18) 1 (17)	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0.	8 (24) 7 (23) 6 (22) 5 (21)	TCLO0 TCLO1 CLO BUZ
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	20 (38) 19 (37) 18 (36) 17 (35)	TCL0 TCL1
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. N-channel open-drain output up to 9 volts. 1-bit and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to support 8-bit data transfer. 8-bit unit pull-up resistors are assignable by mask option.	26–23 (44–41) 30–27 (4–1)	–
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. 1-bit or 4-bit read/write and test is possible. Port 6 pins are individually software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins (port 6 only). Ports 6 and 7 can be paired to enable 8-bit data transfer.	37–34 (11–8) 41–38 (15–12)	KS0–KS3 KS4–KS7
P8.0–P8.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Pins are individually software configurable as input or output. 4-bit pull-down resistors are software assignable; pull-down resistors are automatically disabled for output pins.	16–13 (32–29)	–

NOTE: Parentheses indicate pin number for 44 QFP package.

Table 1–1. KS57C0404/C0408 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
SCK	I/O	Serial I/O interface clock signal	12 (28)	P0.0
SO	I/O	Serial data output	11 (27)	P0.1
SI	I/O	Serial data input	10 (26)	P0.2
BTCO	I/O	Basic timer clock output (2 Hz, 16 Hz, 64 Hz, or 256 Hz at 4.19 MHz)	9 (25)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. INT0 is synchronized to system clock.	4, 3 (20, 19)	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	2 (18)	P1.2
INT4	I	External interrupt with detection of rising and falling edges.	1 (17)	P1.3
TCLO0	I/O	Timer/counter 0 clock output	8 (24)	P2.0
TCLO1	I/O	Timer/counter 1 clock output	7 (23)	P2.1
CLO	I/O	Clock output	6 (22)	P2.2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at 4.19 MHz for buzzer sound	5 (21)	P2.3
TCL0	I/O	External clock input for timer/counter 0	20 (38)	P3.0
TCL1	I/O	External clock input for timer/counter 1	19 (37)	P3.1
KS0–KS3 KS4–KS7	I/O	Quasi-interrupt inputs with falling edge detection	37–34 (11–8) 41–38 (15–12)	P6.0–P6.3 P7.0–P7.3
V_{DD}	–	Power supply	21 (39)	–
V_{SS}	–	Ground	42 (16)	–
RESET	I	Reset signal	31 (5)	–
X_{in}, X_{out}	–	Crystal, ceramic, or RC oscillator signal for system clock (For external clock input, use X_{in} and input X_{in}'s reverse phase to X_{out})	33, 32 (7, 6)	–
TEST	–	Test signal input (must be connected to V_{SS})	22 (40)	–
NC	–	No connection (must be connected to V_{SS})	(33, 34)	–

NOTE: Parentheses indicate pin number for 44 QFP package.

Table 1–2. Overview of KS57C0404/C0408 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.0–P0.3	SCK, SO, SI, BTCO	I/O	Input	D-1
P1.0–P1.2	INT0, INT1, INT2	I	Input	A-3
P1.3	INT4	I	Input	B-4
P2.0–P2.3	TCLO0, TCLO1, CLO, BUZ	I/O	Input	D
P3.0–P3.1	TCL0, TCL1	I/O	Input	D-1
P3.2–P3.3	–	I/O	Input	D
P4.0–P4.3 P5.0–P5.3	–	I/O	(NOTE)	E-2
P6.0–P6.3 P7.0–P7.3	KS0–KS3 KS4–KS7	I/O	Input	D-1
P8.0–P8.3	–	I/O	Input	D-2
X_{in}, X_{out}	–	–	–	–
RESET	–	I	–	B
TEST	–	I	–	–
NC	–	–	–	–
V_{DD}, V_{SS}	–	–	–	–

NOTE: When pull-up resistors are provided, port 4 and port 5 pins are reset to high level; with no pull-ups, they are reset to high impedance.