KS57C2016
4-BIT CMOS Microcontroller

Product Specification

OVERVIEW

The KS57C2016 single-chip CMOS microcontroller is designed for very high performance using Samsung's newest 4-bit CPU core. With an up-to-20-digit LCD direct drive capability and up to 40 pins for LCD segment data output, a versatile 16-bit timer/counter with pulse width modulation and data capture functions, and its large ROM size, the "2016" offers you an excellent design solution for a wide variety of LCD applications.

Up to 56 pins of the 100-pin QFP package can be dedicated to I/O. Eight vectored interrupts provide fast response to internal and external events. In addition, the 2016's advanced CMOS technology ensures low power consumption and a wide operating voltage range.

FEATURES

Memory

- 512 × 4-bit RAM
- 16,384 × 8-bit ROM

56 I/O Pins

- I/O: 40 pins (8 n-channel open-drain pins)
- Input only: 4 pins
- Output only: 12 pins

LCD Controller/Driver

- Maximum 20-digit LCD direct drive capability
- 28, 32, 36, and 40 segment outputs selectable
- Display modes: Static, 1/2 duty (1/2 bias)
- 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-Bit Basic Timer

- 4 interval timer functions

8-Bit Timer/Counter

- Programmable 8-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider
- Serial I/O interface clock generator

16-Bit Timer/Counter

- Programmable 16-bit timer
- External event counter
- Arbitrary clock output
- External clock signal divider
- Capture function
- 16-bit PWM output function

Watch Timer

- Time interval generation: 0.5s, 3.9 ms at 32768 Hz
- 4 frequency outputs (BUZ)
- Clock generation for LCD

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal/external clock source

Interrupts

- 5 internal vectored interrupts
- 3 external vectored interrupts
- 2 quasi-interrupts

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle (only CPU clock stops)
- Stop (system clock stops)

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 μs at 4.19 MHz
- 122 μs at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 2.7 V to 6.0 V

Package Type

- 100-pin QFP

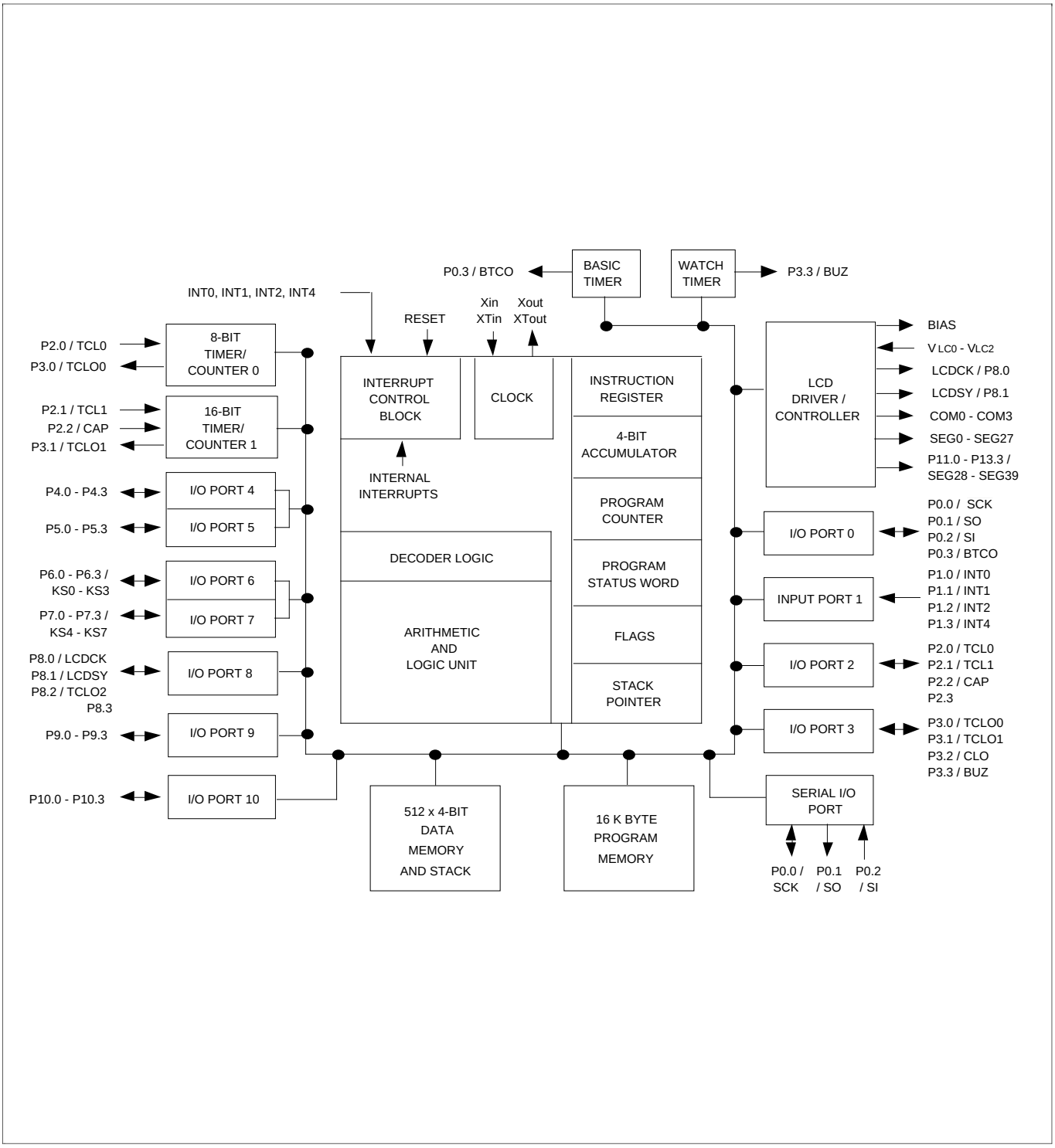

Figure 1. KS57C2016 Block Diagram

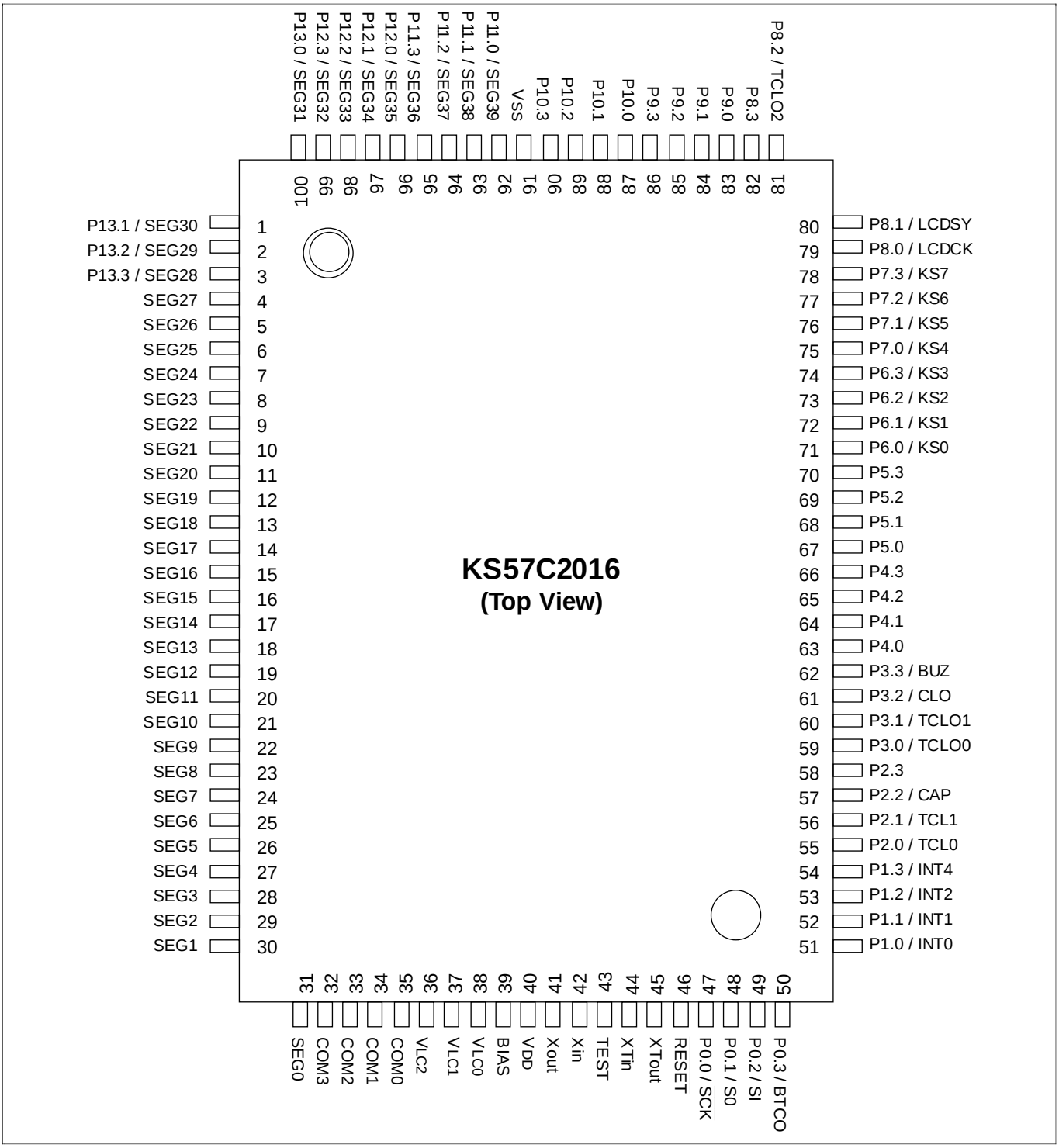

Figure 2. KS57C2016 Pin Assignments (100-QFP)

Table 1. KS57C2016 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable	47 48 49 50	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are assignable by software to pins P1.0, P1.1, and P1.2.	51 52 53 54	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0	55 56 57 58	TCL0 TCL1 CAP —
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0	59 60 61 62	TCLO0 TCLO1 CLO BUZ
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. N-channel open-drain output up to 9volts. 1-, 4-, and 8-bit read/write and test is possible. Ports 4 and 5 can be paired to support 8-bit data transfer. Pull-up resistors are assignable to individual pins by mask option.	63–66 67–70	— —
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. Port 6 pins are individually software configurable as input or output. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable. Ports 6 and 7 can be paired to enable 8-bit data transfer.	71–74 75–78	KS0–KS3 KS4–KS7
P8.0 P8.1 P8.2 P8.3	I/O	Same as port 0.	79 80 81 82	LCDCK LCDSY TCLO2 —
P9.0–P9.3 P10.0–P10.3	I/O	Same as port 0.	84–86 87–90	— —
P11.0–P13.3	O	Output port for 1-bit data (for use as CMOS driver only)	92–100, 1–3	SEG28– SEG39
SCK	I/O	Serial I/O interface clock signal	47	P0.0
SO	I/O	Serial data output	48	P0.1
SI	I/O	Serial data input	49	P0.2
BTCO	I/O	Basic interval timer clock output	50	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	51–52	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	53	P1.2
INT4	I	External interrupt with detection of rising or falling edges	54	P1.3

Table 1. KS57C2016 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
TCL0	I/O	External clock input for timer/counter 0	55	P2.0
TCL1	I/O	External clock input for timer/counter 1	56	P2.1
CAP	I/O	Capture pin for timer/counter 1 data capture values and external clock input for 8-bit timer/counter 1B	57	P2.2
TCLO0	I/O	Timer/counter 0 clock output	59	P3.0
TCLO1	I/O	Timer/counter 1 clock output	60	P3.1
TCLO2	I/O	8-bit timer/counter 1B clock output	81	P8.2
CLO	I/O	System clock output	61	P3.2
BUZ	I/O	2 kHz or 4 kHz frequency output for buzzer sound	62	P3.3
KS0–KS7	I/O	Quasi-interrupt input with falling edge detection	71–78	P6.0–P7.3
LCDCK	I/O	LCD clock output for display expansion	79	P8.0
LCDSY	I/O	LCD syncronization clock output for display expansion	80	P8.1
SEG0–SEG27	O	LCD segment data output	31, 30–4	—
SEG28–SEG39	O	1-bit LCD segment data output	92–100, 1–3	P11.0–P13.3
COM0–COM3	O	Common signal output for LCD display	35–32	—
V_{LC0}–V_{LC2}	—	LCD power supply. Voltage dividing resistors are assignable by mask option	38–36	—
TEST	I	Test signal input (must be connected to V_{SS})	43	—
V_{DD}	—	Main power supply	40	—
V_{SS}	—	Ground	91	—
RESET	I	Reset signal	46	—
BIAS	—	LCD power control	39	—
X_{in}, X_{out}	—	Crystal, ceramic, or R/C oscillator signal for main system clock. (For external clock input, use X_{in} and input X_{in}'s reverse phase to X_{out})	42, 41	—
XT_{in}, XT_{out}	—	Crystal oscillator signal for subsystem clock. (For external clock input, use XT_{in} and input XT_{in}'s reverse phase to XT_{out})	44, 45	—

NOTE: Pull-up resistors for ports 0, 2, 3, and 6–10 are automatically disabled when they are configured to output mode.

Table 2. Supplemental KS57C2016 Pin Data

Pin Numbers	Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
1–3	P13.1–P13.3	SEG30–SEG28	O	Low	9
4–31	SEG27–SEG0	—	O	Low	7
35–32	COM0–COM3	—	O	Low	8
38–36	V_{LC0}–V_{LC2}	—	—	—	—
39	BIAS	—	—	—	—
40	V_{DD}	—	—	—	—
42, 41	X_{in}, X_{out}	—	—	—	—
43	TEST	—	I	—	—
44, 45	XT_{in}, XT_{out}	—	—	—	—
46	RESET	—	I	—	2
47–50	P0.0–P0.3	SCK, SO, SI, BTCO	I/O	Input	6
51–53	P1.0–P1.2	INT0, INT1, INT2	I	Input	3
54	P1.3	INT4	I	Input	2
55–58	P2.0–P2.2	TCL0, TCL1, CAP	I/O	Input	6
58	P2.3	—	I/O	Input	6
59–62	P3.0–P3.3	TCLO0, TCLO1, CLO, BUZ	I/O	Input	5
63–66	P4.0–P4.3	—	I/O	(1)	10
67–70	P5.0–P5.3	—	I/O	(1)	10
71–74	P6.0–P6.3	KS0–KS3	I/O	Input	6
75–78	P7.0–P7.3	KS4–KS7	I/O	Input	6
79–81	P8.0–P8.2	LCDCK, LCDSY, TCLO2	I/O	Input	5
82	P8.3	—	I/O	Input	5
83–86	P9.0–P9.3	—	I/O	Input	5
87–90	P10.0–P10.3	—	I/O	Input	5
91	V_{SS}	—	—	—	—
92–95	P11.0–P11.3	SEG39–SEG36	O	Low	9
96–99	P12.0–P12.3	SEG35–SEG32	O	Low	9
100	P13.0	SEG31	O	Low	9

NOTES:
1. When pull-up resistors are provided, high level; when pull-up resistors are not provided, high impedance.
2. Pin circuit diagrams are provided below.