1 PRODUCT OVERVIEW

OVERVIEW

The KS57C4104/KS57C4204/KS57C4304 single-chip CMOS microcontroller has been designed for very high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontroller).

With an A/D converter, LED direct drive pins, an 8-bit serial I/O interface, and an 8-bit timer/counter, the KS57C4104/KS57C4204/KS57C4304 offers you an excellent design solution for a wide variety of home appliance applications —electric fans, cookers, boilers, and air conditioners, for example.

Up to 35 pins of the 42-pin SDIP or 44-pin QFP package can be dedicated to I/O. Seven vectored interrupts provide fast response to internal and external events.

In addition, the KS57C4104/KS57C4204/KS57C4304's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The KS57C4104/KS57C4204/KS57C4304 microcontroller is also available in OTP (One Time Programmable) version, KS57P4104/KS57P4204/KS57P4304. KS57P4104/KS57P4204/KS57P4304 microcontroller has an on-chip 4-Kbyte one-time-programmable EPROM instead of masked ROM. The KS57P4104/KS57P4204/KS57P4304 is comparable to KS57C4104/KS57C4204/KS57C4304, in function, in D.C. electrical characteristics and in pin configuration.

DEVELOPMENT SUPPORT

The Samsung Microcontroller Development System, SMDS, provides you with a complete PC-based development environment for KS57-series microcontrollers that is powerful, reliable, and portable. In addition to its window-based program development structure, the SMDS toolset includes versatile debugging, trace, instruction timing, and performance measurement applications.

The Samsung Generalized Assembler (SAMA) has been designed specifically for the SMDS environment and accepts assembly language sources in a variety of microprocessor formats. SAMA generates industry-standard hex files that also contain program control data for SMDS compatibility.

FEATURES SUMMARY

Memory

- 256 × 4-bit RAM
- 4,096 × 8-bit ROM

35 I/O Pins

- I/O: 31 pins including 8 LED direct drive pins (KS57C4104/C4304)
  18 pins including 8 LED direct drive pins (KS57C4204)
- Input only: 4 pins

A/D Converter

- 6-channel with 8-bit resolution
- 22.89 µs conversion speed at 4.19 MHz

Basic Timer

- One 8-bit basic timer
- Watchdog timer functions
- Four interval clock selection

Timer/Counters

- Two 8-bit timer/counter (TC0, TC1)
- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- PWM output mode (TC1)

Watch Timer

- One watch timer 8-bit
- Time interval generation: 0.5 s, 3.9 ms at 4.19 MHz
- Four frequency outputs to BUZ pin

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Built-in reset circuit (KS57C4304 only)

- Built-in power-on reset circuit

Interrupts

- Five internal vectored interrupts (INTB, INTT0, INTT1, INTS, INTAD)
- Three external vectored interrupts (INT0, INT1, INT4)
- Two quasi-interrupts (INT2, INTW)

Bit Sequential Carrier

- Supports 16-bit serial data transfer in arbitrary format

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (system oscillation stops)

Oscillation Sources

- Crystal, Ceramic, or RC for system clock
- Crystal, Ceramic: 0.4–6.0 MHz
- RC: 4 MHz (typ)
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 µs at 4.19 MHz
- 0.67, 1.33, 10.7 µs at 6.0 MHz

Operating Temperature

- –40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V (KS57C4104/C4204)
- 2.5 V to 5.5 V (KS57C4304)

Package Type

- 42-pin SDIP, 44-pin QFP (KS57C4104/C4304)
  30-pin SDIP, 28-pin SOP (KS57C4204)

Table 1-1. Comparision Table

Feature	KS57C4104	KS57C4204	KS57C4304
Core	SAM47	SAM47	SAM47
ROM	4 K bytes	Same	Same
RAM	256 nibbles	Same	Same
I/O	35 (4 input only)	21 (3 input only)	35 (4 input only)
POR (1)	None	None	Built in/ Typ: 2.0 V
SIO	8-bit SIO x 1	Same	Same
Timer0	8-bit timer/counter	Same	Same
Timer1(PWM)	8-bit timer/counter (8-bit PWM x 1)	Same	Same
Watchdog timer	Watch-dog 4 selectable interval	Same	Same
ADC	8-bit x 6	8-bit x 4	8-bit x 6
AV_{SS}	None (2)	Same	Same
Interrupt	External x 3 Internal x 5 Quasi x 2 (KS0–KS3)	External x 2 Internal x 5 Quasi x 1 (–)	External x 3 Internal x 5 Quasi x 2 (KS0–KS3)
Power down	Stop/Idle	Same	Same
Oscillator	Crystal, Ceramic, RC	Same	Same
Operating frequency	0.4–6 MHz	Same	Same
Operating voltage	1.8–5.5 V	1.8–5.5 V	2.5–5.5 V
OTP/MTP	OTP	Same	Same
Package	42SDIP/44QFP	30SDIP/28SOP	42SDIP/44QFP

NOTES

1. POR (power on reset)/Typ 2.0 V low voltage detector.
2. Internal A/D converter ground (bonded to V_{SS} internally)

BLOCK DIAGRAM

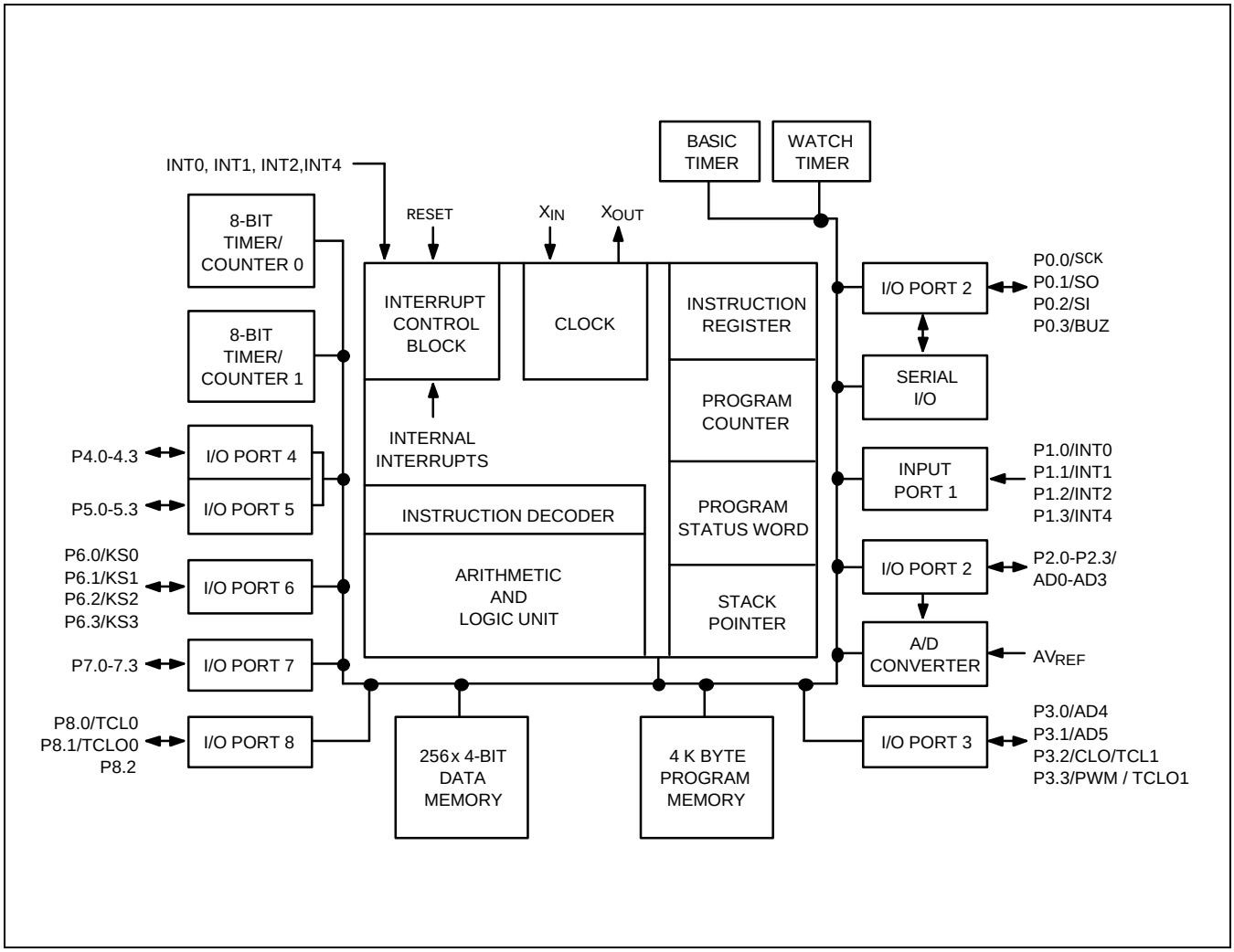

Figure 1-1. KS57C4104/C4204/C4304 Simplified Block Diagram

PIN ASSIGNMENTS

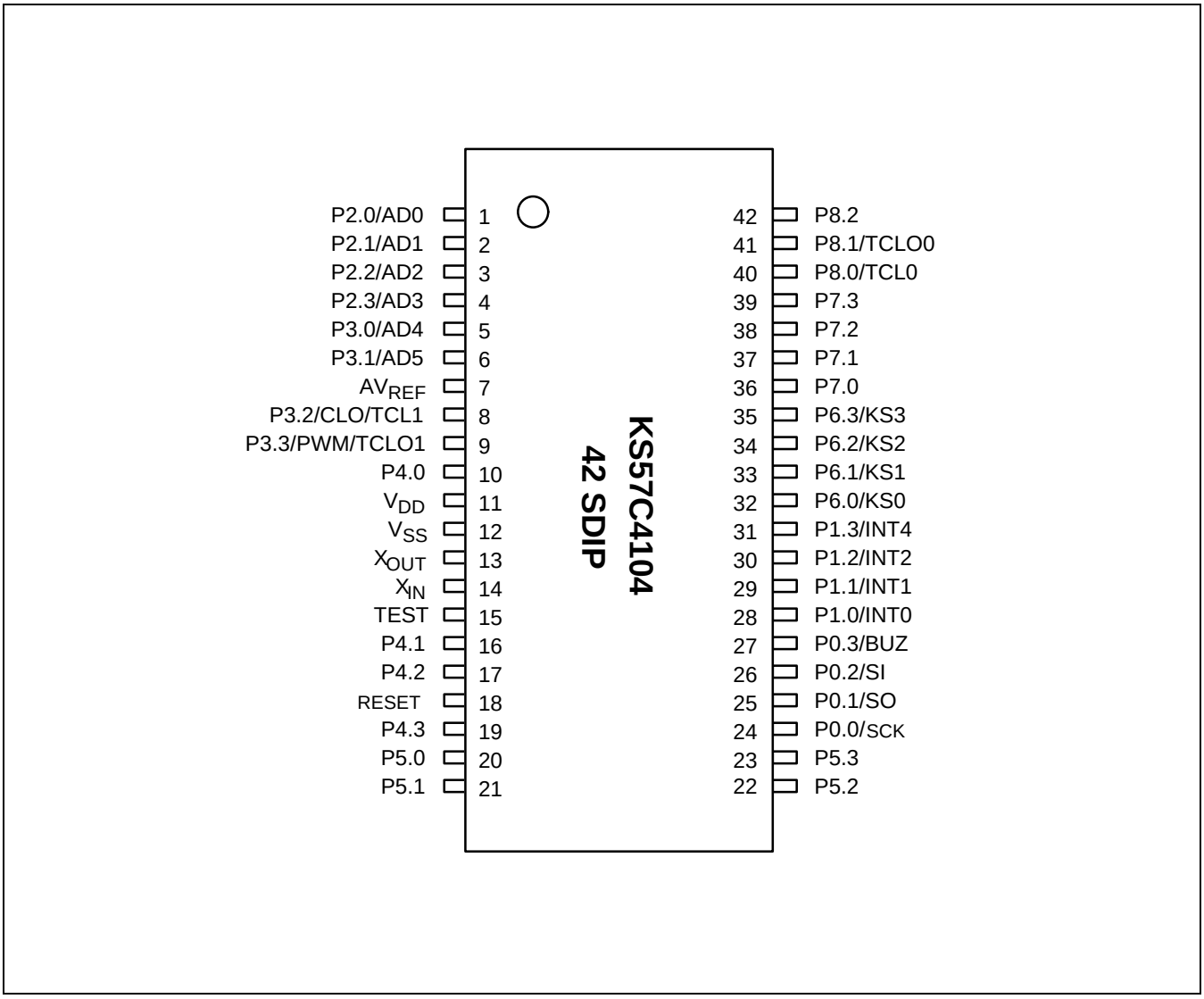

Figure 1-2. KS57C4104 Pin Assignment (42-SDIP)

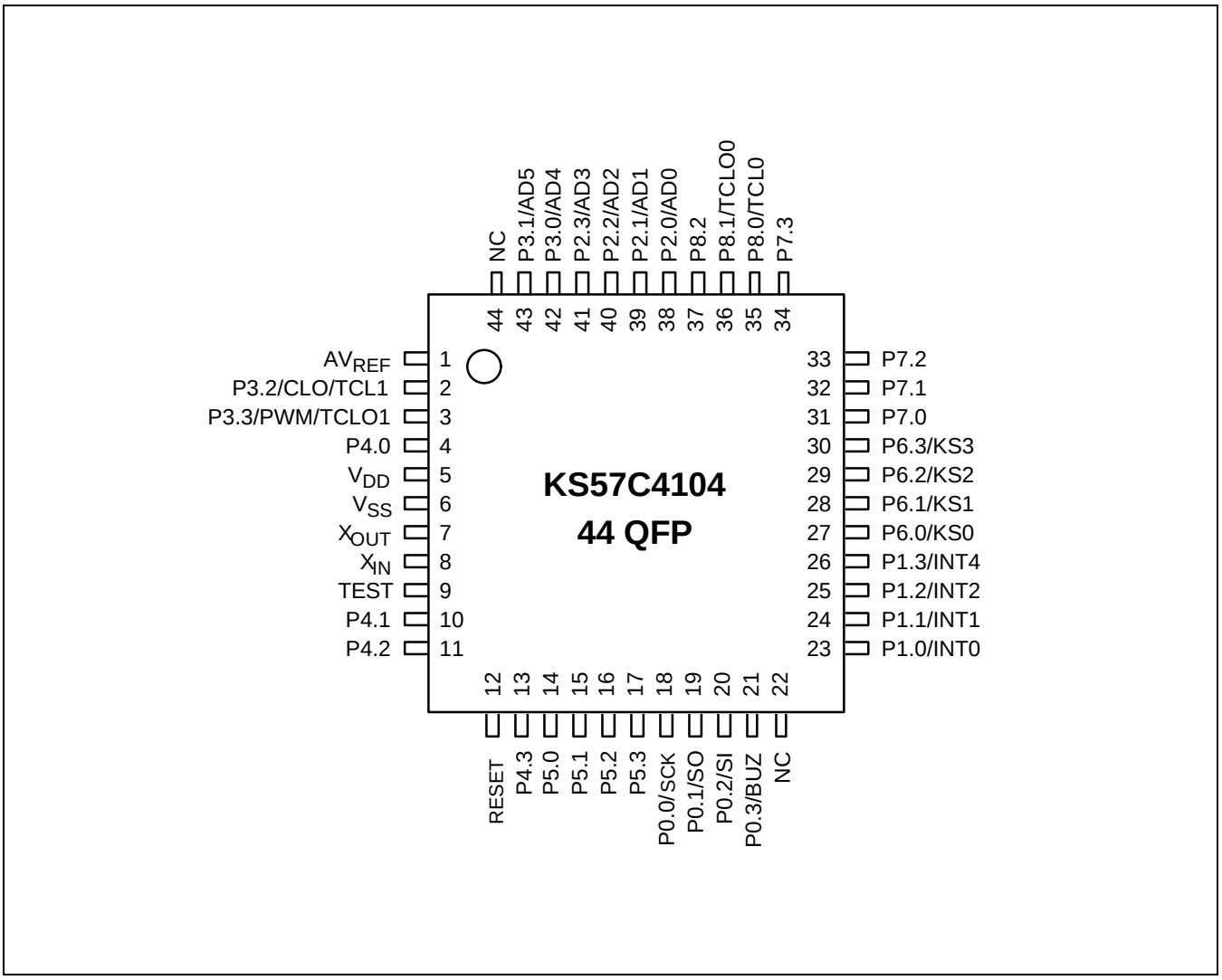

Figure 1-3. KS57C4104 Pin Assignment (44-QFP)

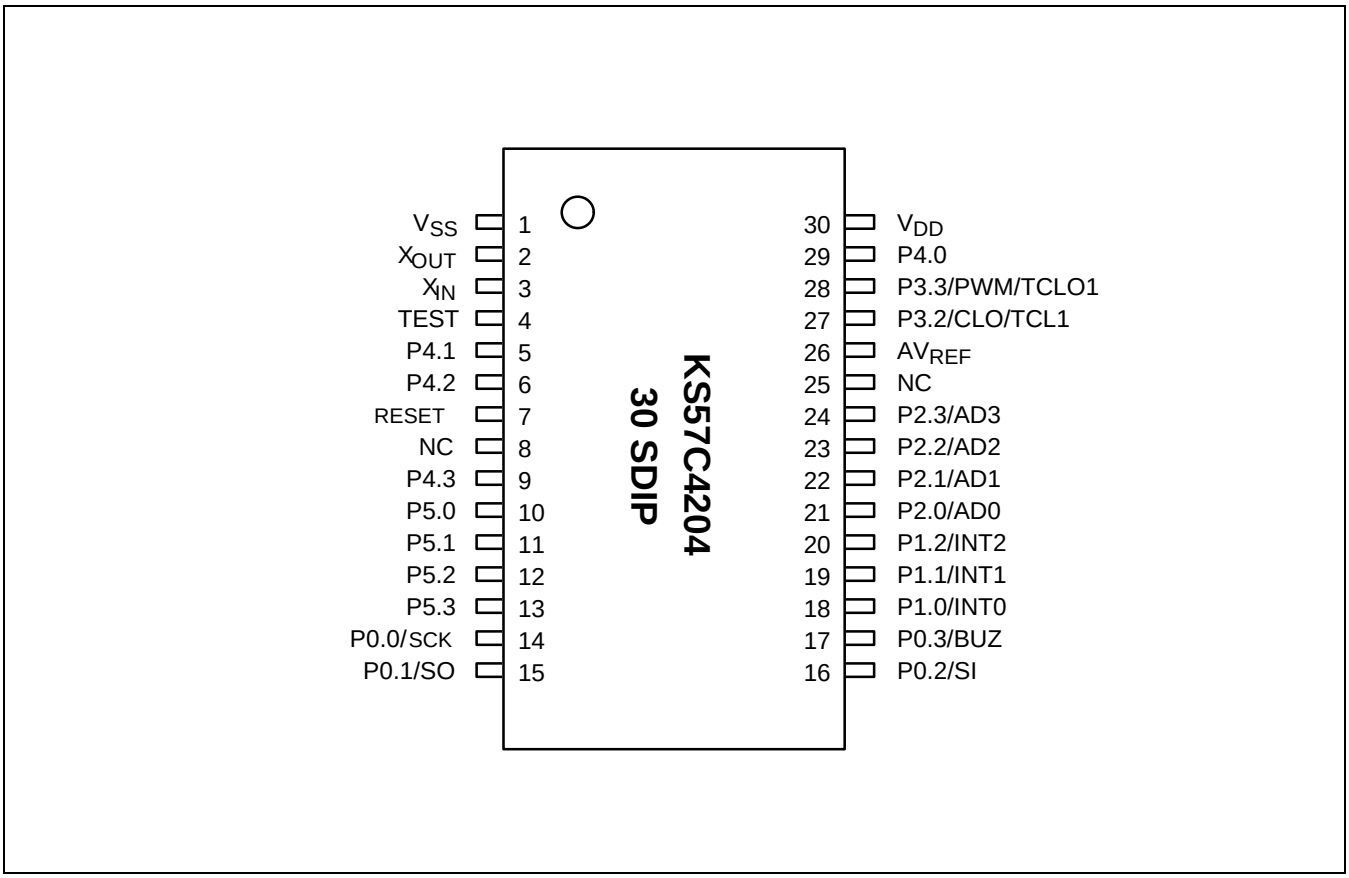

Figure 1-4. KS57C4204 Pin Assignment (30-SDIP)

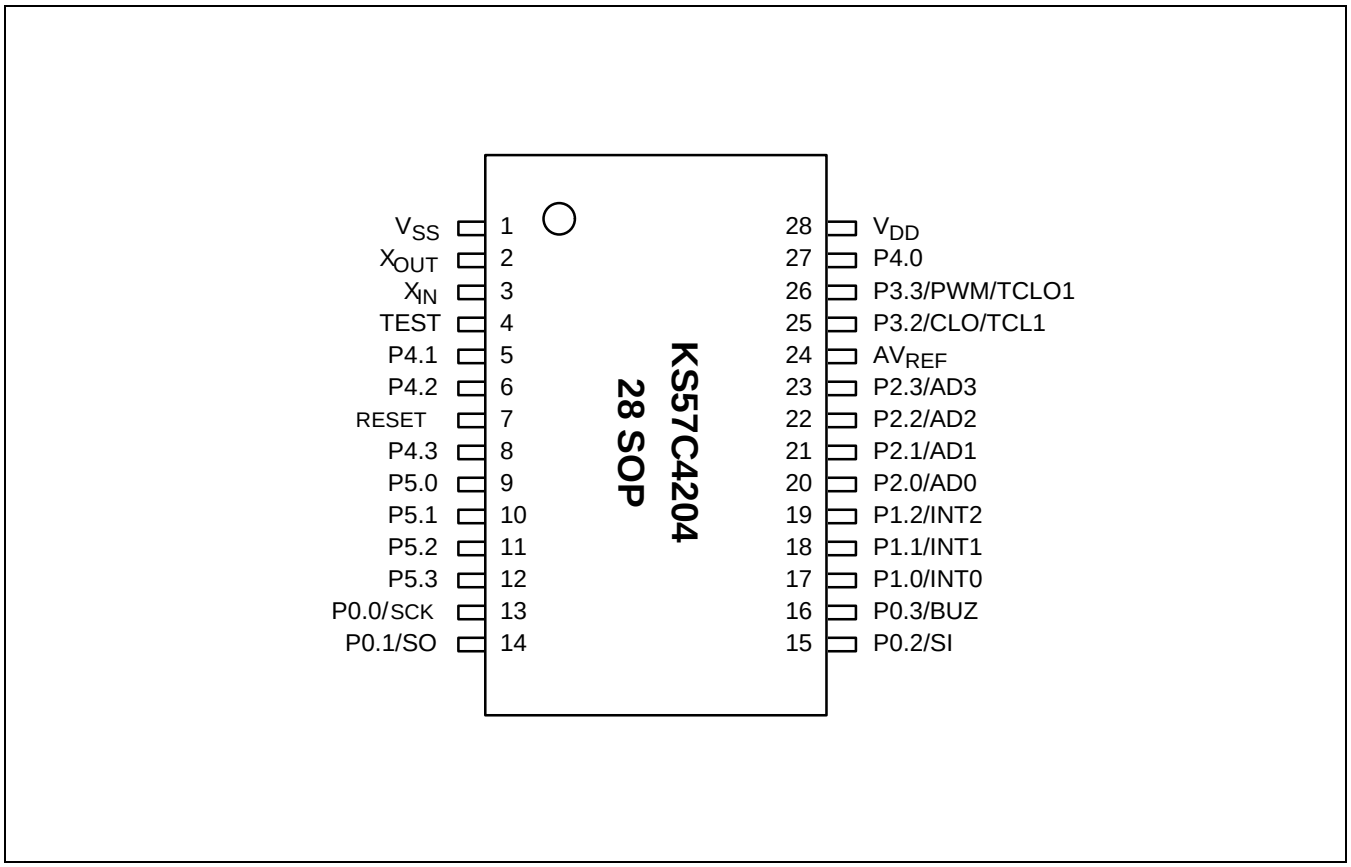

Figure 1-5. KS57C4204 Pin Assignment (28-SOP)

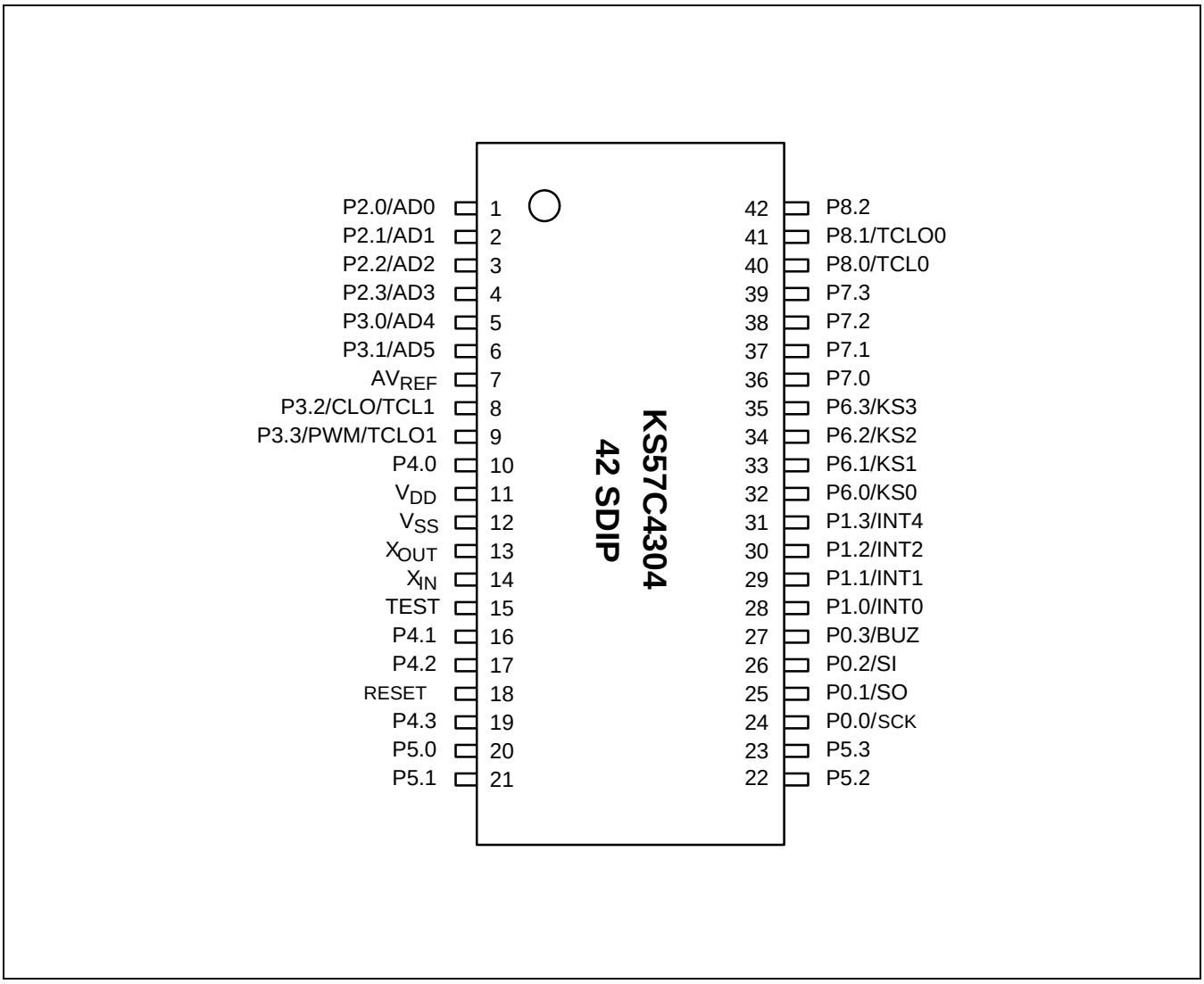

Figure 1-6. KS57C4304 Pin Assignment (42-SDIP)

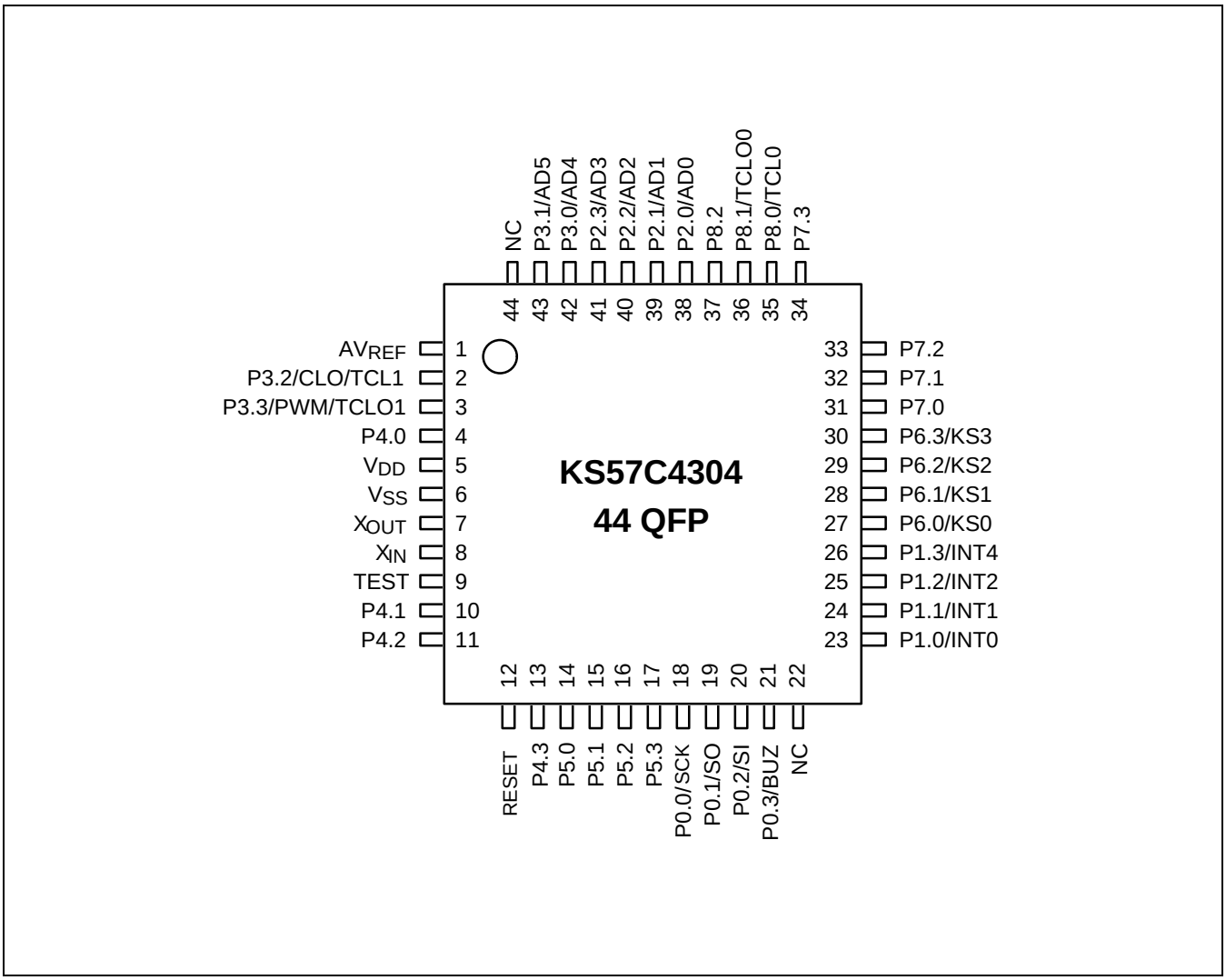

Figure 1-7. KS57C4304 Pin Assignment (44-QFP)

PIN DESCRIPTIONS

Table 1-2. KS57C4104/C4304 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	24 (18) 25 (19) 26 (20) 27 (21)	SCK SO SI BUZ
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are individually assignable by software to pins P1.0, P1.1, and P1.2.	28 (23) 29 (24) 30 (25) 31 (26)	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. N-channel open-drain output. 1-bit or 4-bit write and test is possible. Individual pins are software configurable as AD input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	1 (38) 2 (39) 3 (40) 4 (41)	AD0 AD1 AD2 AD3
P3.0 P3.1 P3.2 P3.3	I/O	Same as Port 0 (P0.0–P0.3)	5 (42) 6 (43) 8 (2) 9 (3)	AD4 AD5 CLO/TCL1 PWM/TCLO1
P4.0 P4.1 P4.2 P4.3 P5.0–P5.3	I/O	4-bit I/O ports. Ports 4 and 5 can be configured individually as n-channel open-drain or as CMOS push-pull output by software. 1-bit and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to enable 8-bit data transfer. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	10 (4) 16 (10) 17 (11) 19 (13) 20–23 (14–17)	–
P6.0–P6.3 P7.0–P7.3 P8.0 P8.1 P8.2	I/O	Same as Port 0 except port 8 is a 3-bit I/O port	32–35 (27–30) 36–39 (31–34) 40 (35) 41 (36) 42 (37)	KS0–KS3 – TCL0 TCLO0 –

Table 1-2. KS57C4104/C4304 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
SCK	I/O	Serial I/O interface clock signal	24 (18)	P0.0
SO	I/O	Serial data output	25 (19)	P0.1
SI	I/O	Serial data input	26 (20)	P0.2
BUZ	I/O	2 kHz, 4kHz, 8kHz, or 16 kHz frequency output at the watch timer clock frequency of 32.768 kHz	27 (21)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	28–29 (23–24)	P1.0, P1.1
INT2	I	Quasi-interrupt input with rising edge detection	30 (25)	P1.2
INT4	I	External interrupts with detection of rising and falling edges	31 (26)	P1.3
AD0–AD3 AD4–AD5	I/O	A/D converter analog inputs	1–4 (38–41) 5–6 (42–43)	P2.0–P2.3 P3.0–P3.1
TCL0	I/O	External clock input for timer/counter0	40 (35)	P8.0
TCLO0	I/O	Timer/counter clock output	41 (36)	P8.1
CLO	I/O	Clock output	8 (2)	P3.2
TCL1	I/O	External clock input for timer/counter1	8 (2)	P3.2
PWM	I/O	PWM output	9 (3)	P3.3
TCLO1	I/O	Timer/counter clock output1	9 (3)	P3.3
KS0–KS3	I/O	Quasi-interrupt input with falling edge detection	32–35 (27–30)	P6.0–P6.3
V_{DD}	–	Main power supply	11 (5)	–
V_{SS}	–	Ground	12 (6)	–
RESET	I	Reset signal	18 (12)	–
X_{IN}, X_{out}	–	Crystal, ceramic, or RC oscillator signal for system clock.	14, 13 (8, 7)	–
AV_{REF}	–	A/D converter analog reference voltage	7 (1)	–
TEST	I	Test signal input (must be connected to V_{SS})	15 (9)	–
NC	–	No connection (no bonding pin)	(22, 44)	–

NOTE: Parentheses indicate 44-QFP pin number.

Table 1-3. KS57C4204 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	14 (13) 15 (14) 16 (15) 17 (16)	SCK SO SI BUZ
P1.0 P1.1 P1.2	I	4-bit input port. 1-bit and 4-bit read and test is possible. 3-bit pull-up resistors are individually assignable by software to pins P1.0, P1.1, and P1.2.	18 (17) 19 (18) 20 (19)	INT0 INT1 INT2
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. N-channel open-drain output. 1-bit or 4-bit write and test is possible. Individual pins are software configurable as AD input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	21 (20) 22 (21) 23 (22) 24 (23)	AD0 AD1 AD2 AD3
P3.2 P3.3	I/O	Same as Port 0 (P0.0–P0.3)	27 (25) 28 (26)	CLO/TCL1 PWM/TCLO1
P4.0 P4.1 P4.2 P4.3 P5.0–P5.3	I/O	4-bit I/O ports. Ports 4 and 5 can be configured individually as n-channel open-drain or as CMOS push-pull output by software. 1-bit and 4-bit read/write and test is possible. Ports 4 and 5 can be paired to enable 8-bit data transfer. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	29 (27) 5 (5) 6 (6) 9 (8) 10–13 (9–12)	–

Table 1-3. KS57C4204 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
SCK	I/O	Serial I/O interface clock signal	14 (13)	P0.0
SO	I/O	Serial data output	15 (14)	P0.1
SI	I/O	Serial data input	16 (15)	P0.2
BUZ	I/O	2 kHz, 4kHz, 8kHz, or 16 kHz frequency output at the watch timer clock frequency of 32.768 kHz	17 (16)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	18, 19 (17, 18)	P1.0, P1.1
INT2	I	Quasi-interrupt input with rising edge detection	20 (19)	P1.2
AD0–AD3	I/O	A/D converter analog inputs	21–24 (20–23)	P2.0–P2.3
CLO	I/O	Clock output	27 (25)	P3.2
TCL1	I/O	External clock input for timer/counter1	27 (25)	P3.2
PWM	I/O	PWM output	28 (26)	P3.3
TCLO1	I/O	Timer/counter clock output1	28 (26)	P3.3
V_{DD}	–	Main power supply	30 (28)	–
V_{SS}	–	Ground	1 (1)	–
RESET	I	Reset signal	7 (7)	–
X_{IN}, X_{OUT}	–	Crystal, ceramic, or RC oscillator signal for system clock.	3, 2 (3, 2)	–
AV_{REF}	–	Internal A/D converter analog reference voltage	26 (24)	–
TEST	I	Test signal input (must be connected to V_{SS})	4 (4)	–
NC	–	No connection (no bonding pin)	8, 25	–

NOTE: Parentheses indicate 28-SOP pin number.

Table 1-4. Overview of KS57C4104/C4204/C4304 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.0–P0.3	SCK, SO, SI, BUZ	I/O	Input	Type D
P1.0 P1.1 P1.2	INT0 (note) INT1 (note) INT2 (note)	I	Input	Type A-1
P1.3	INT4	I	Input	Type A
P2.0–P2.3	AD0–AD3	I/O	AD input	Type F-3
P3.0 P3.1 P3.2 P3.3	AD4 AD5 CLO/TCL1 TCLO1/PWM	I/O	Input	Type F Type F Type D Type D
P4.0–P4.3 P5.0–P5.3	–	I/O	Input	Type E
P6.0 P6.1 P6.2 P6.3	KS0 (note) KS1 (note) KS2 (note) KS3 (note)	I/O	Input	Type D
P7.0–P7.3	–	I/O	Input	Type D
P8.0 P8.1 P8.2	TCL0 (note) TCLO0 –	I/O	Input	Type D
V_{DD}, V_{SS}	–	–	–	–
X_{IN}, X_{OUT}	–	–	–	–
RESET	–	I	–	Type B-2 (note)
AV_{REF}	–	–	–	–
TEST	–	I	–	–
NC	–	–	–	–

NOTE: A noise filter circuit is built-in.