1 PRODUCT OVERVIEW

The KS57C5204/C5208/C5304/C5308 single-chip CMOS microcontroller has been designed for high-performance using SAM 47 (Samsung Arrangeable Microcontrollers). SAM 47, Samsung's newest 4-bit CPU core is notable for its low energy consumption and low operating voltage.

You can select from two ROM sizes: 4K or 8K bytes
Except for the difference in ROM size, the features and functions of the KS57C5204 and the KS57C5208, the KS57C5304 and the KS57C5308 are identical.

With it's DTMF generator, watchdog timer function, and versatile 8-bit timer/counters, theKS57C5204/C5208 /C5304/C5308 offers an excellent design solution for a wide variety of telecommunication applications.

Up to 35 pins of the available 42-pin SDIP or 44-pin QFP package for the KS57C5204/C5208, and up to 23 pins of the available 30-pin SDIP or 32-pin SOP package for the KS57C5304/C5308 can be assign to I/O. Six vectored interrupts for KS57C5204/C5208 and four vectored interrupts for KS57C5304/C5308 provide fast response to internal and external events. In addition, the KS57C5204/C5208/C5304/C5308 's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The KS57C5204/C5208 microcontroller is also available in OTP (One Time Programmable) version, KS57P5208. The KS57C5304/C5308 microcontroller is also available in OTP (One Time Programmable) version, KS57P5308. The KS57P5208/P5308 microcontroller has an on-chip 8K-byte one-time-programable EPROM instead of masked ROM. The KS57P5208 is comparable to KS57C5204/C5208, both in function and in pin configuration. Also, the KS57P5308 is comparable to the KS57C5304/C5308, both in function and in pin configuration.

FEATURES SUMMARY

Memory

- 768 × 4-bit RAM
- 4,096 × 8-bit ROM (KS57C5204/C5304)
  8,192 × 8-bit ROM (KS57C5208/C5308)

35 I/O Pins

- Input only: 4 pins (KS57C5204/C5208)
  1 pins (KS57C5304/C5308)
- I/O: 23 pins (KS57C5204/C5208)
  14 pins (KS57C5304/C5308)
- N-channel open-drain I/O: 8 pins

Memory-Mapped I/O Structure

- Data memory bank 15

DTMF Generator

- 16 dual-tone frequencies for tone dialing

8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

Two 8-Bit Timer/Counters

- Programmable 8-bit timer
- External event counter function
- Arbitrary clock frequency output

Watch Timer

- Real-time and interval time measurement
- Four frequency outputs to the BUZ pin

Bit Sequential Carrier

- Supports 8-bit serial data transfer in arbitrary format

Interrupts

- 3 external interrupt vectors (KS57C5204/C5208)
  1 external interrupt vectors (KS57C5304/C5308)
- 3 internal interrupt vectors
- 2 quasi-interrupts

Power-Down Modes

- Idle: Only CPU clock stops
- Stop: System clock stops

Oscillation Sources

- Crystal, or ceramic for main system clock
- Main system clock frequency: 0.4–6.0 MHz (typical)
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, and 15.3 μs at 4.19 MHz
- 1.12, 2.23, 17.88 μs at 3.58 MHz
- 0.67, 1.33, 10.7 μs at 6.0 MHz

Operating Temperature

- – 40 °C to 85 °C

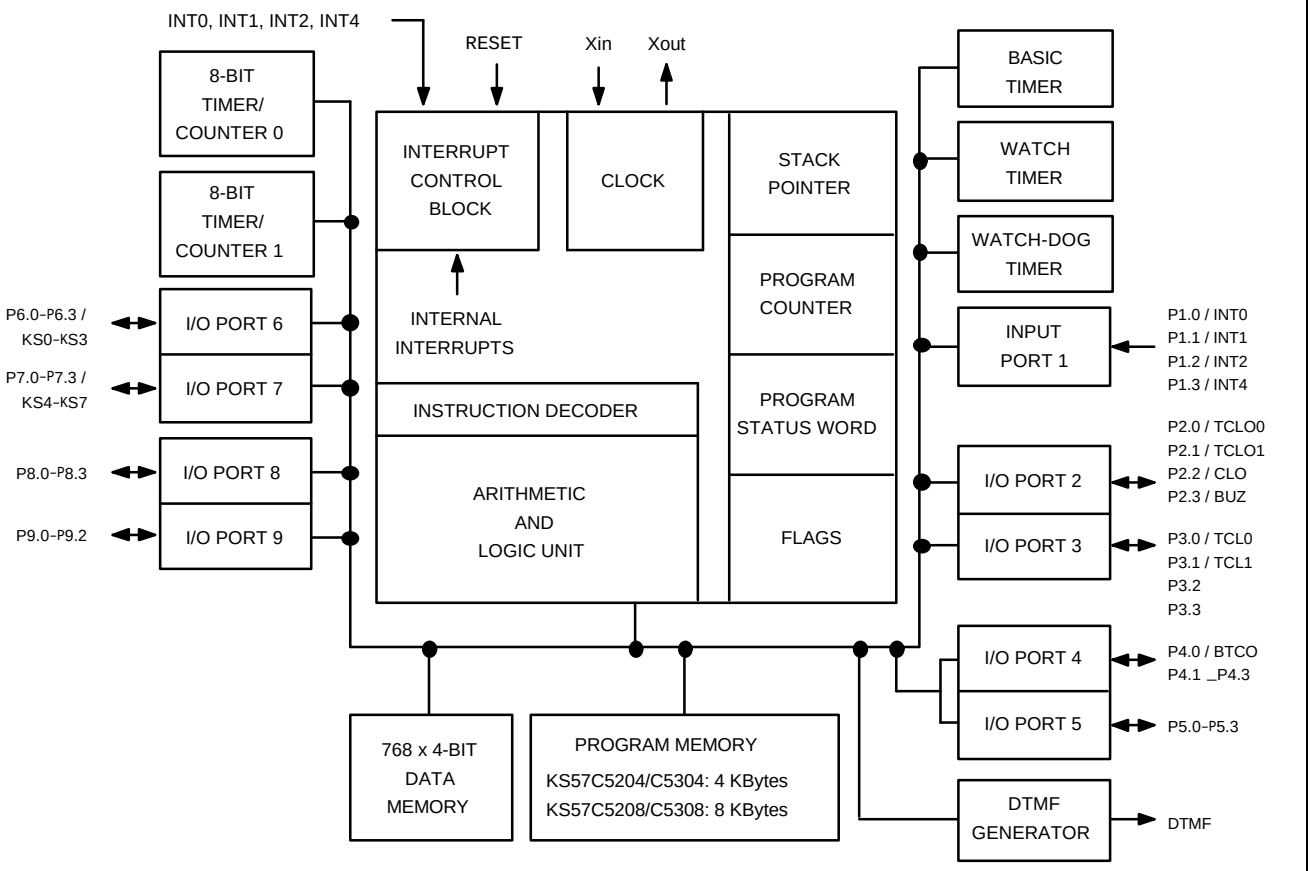
Operating Voltage Range

- 2.0 V to 5.5 V

Package Types

- 42 SDIP, 44 QFP (KS57C5204/C5208)
- 30 SDIP, 32 SOP (KS57C5304/C5308)

BLOCK DIAGRAM



NOTE: KS57C5304/C5308 does not use P1.1/INT1, P1.2/INT2, P1.3/INT3, P3.2, P3.3, INT1, INT2, INT4, P8.0-P8.3, and P9.0-P9.2.

Figure 1–1. KS57C5204/C5208 Simplified Block Diagram

PIN ASSIGNMENTS

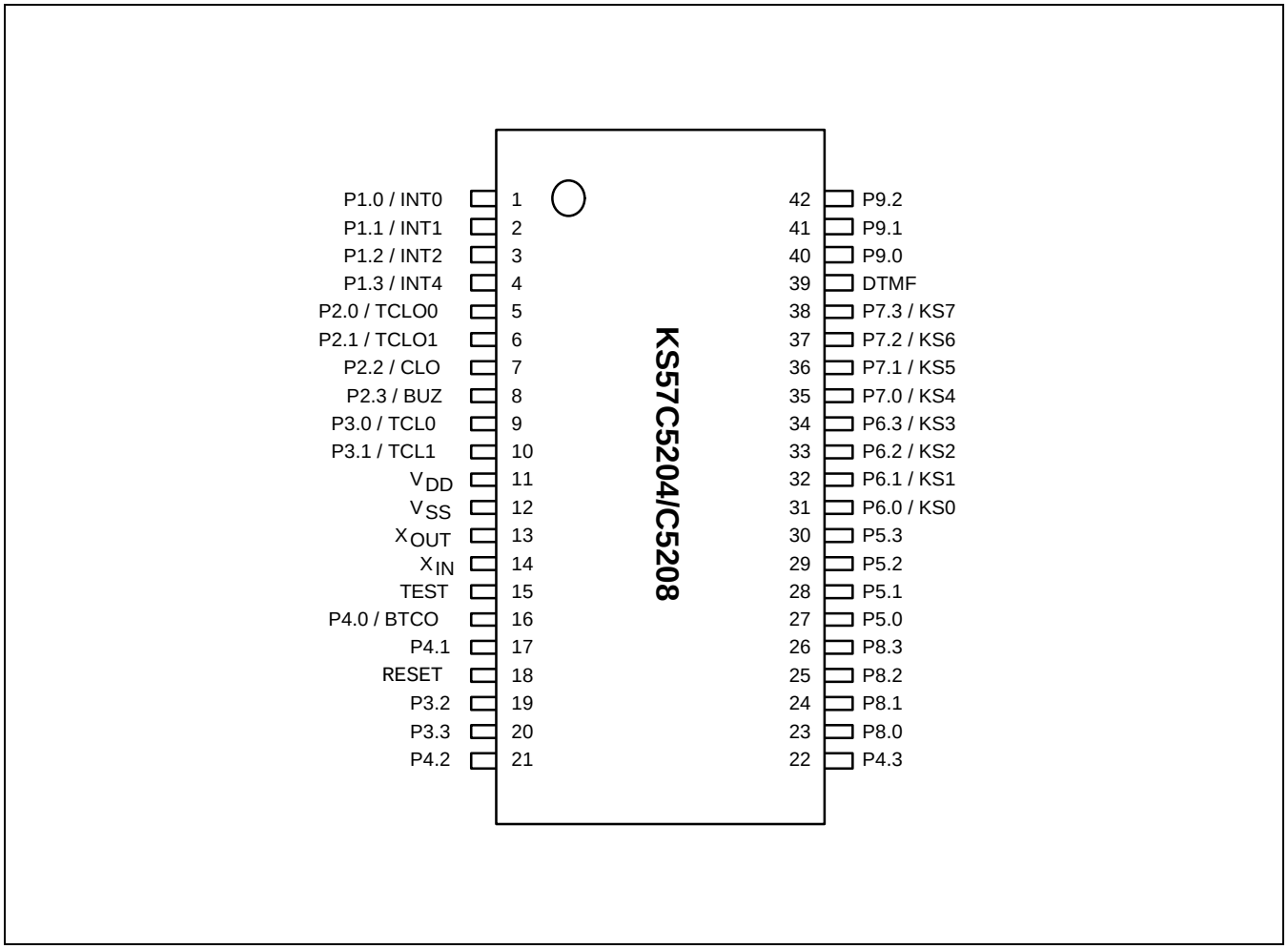


Figure 1–2. KS57C5204/C5208 Pin Assignment Diagrams (42–SDIP)

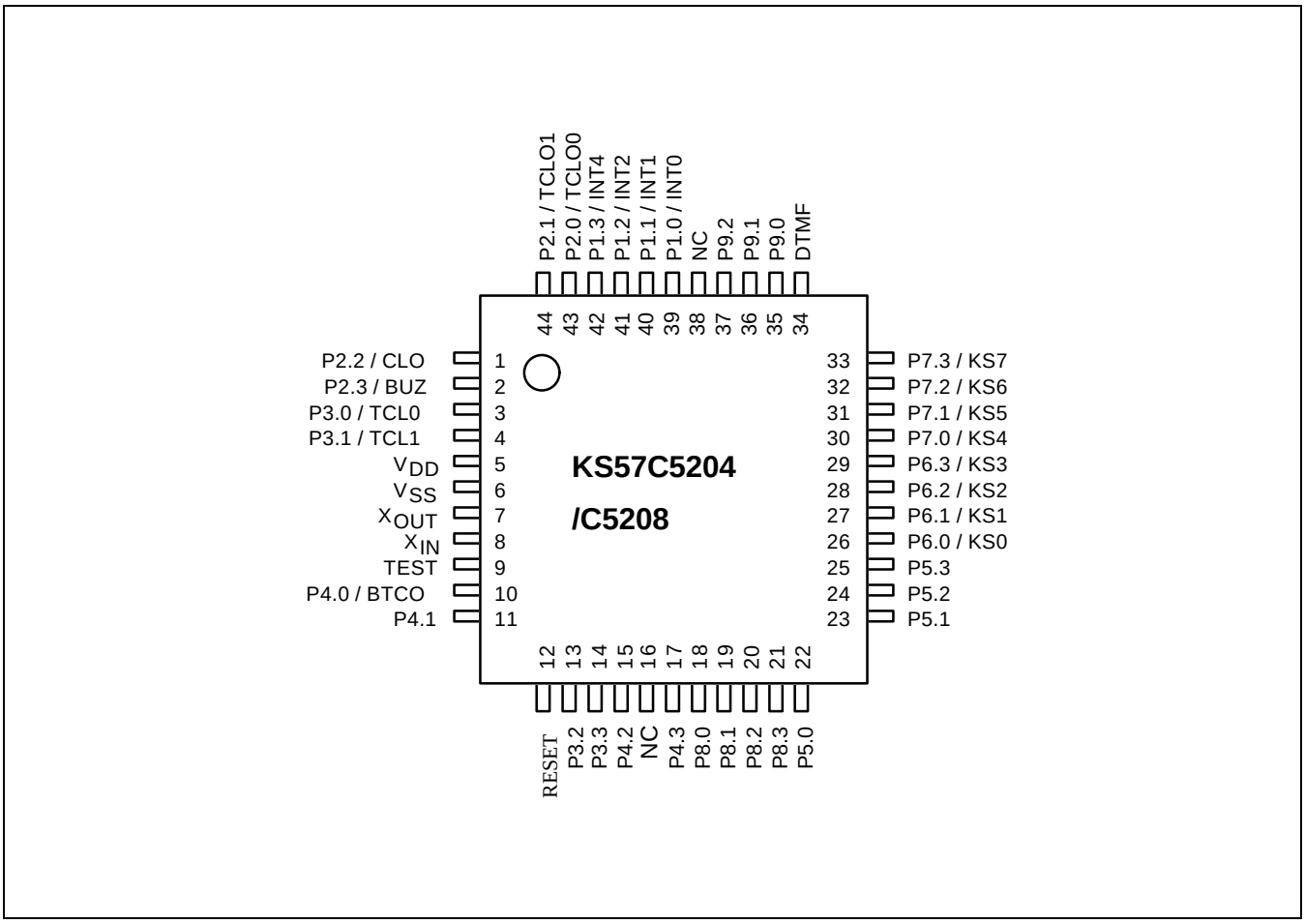


Figure 1–3. KS57C5204/C5208 Pin Assignment Diagrams (44–QFP)

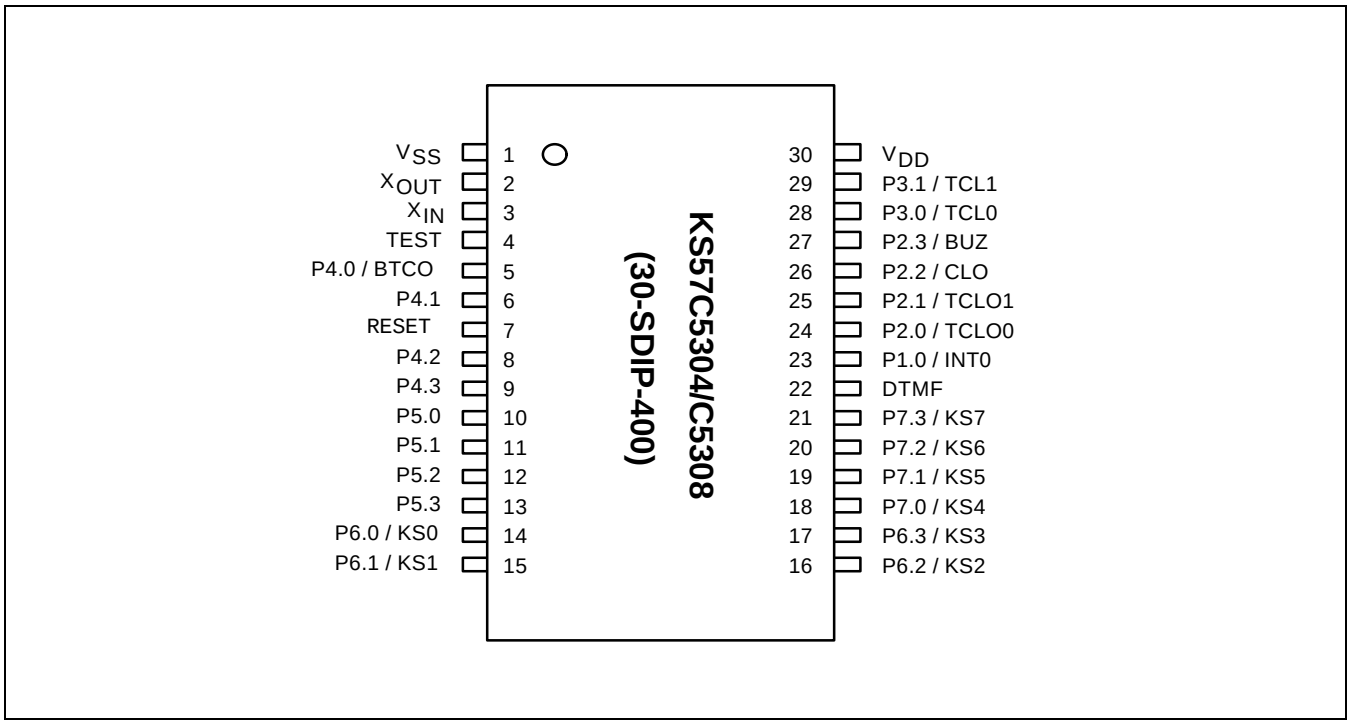


Figure 1–4. KS57C5304/C5308 Pin Assignment Diagrams (30–SDIP)

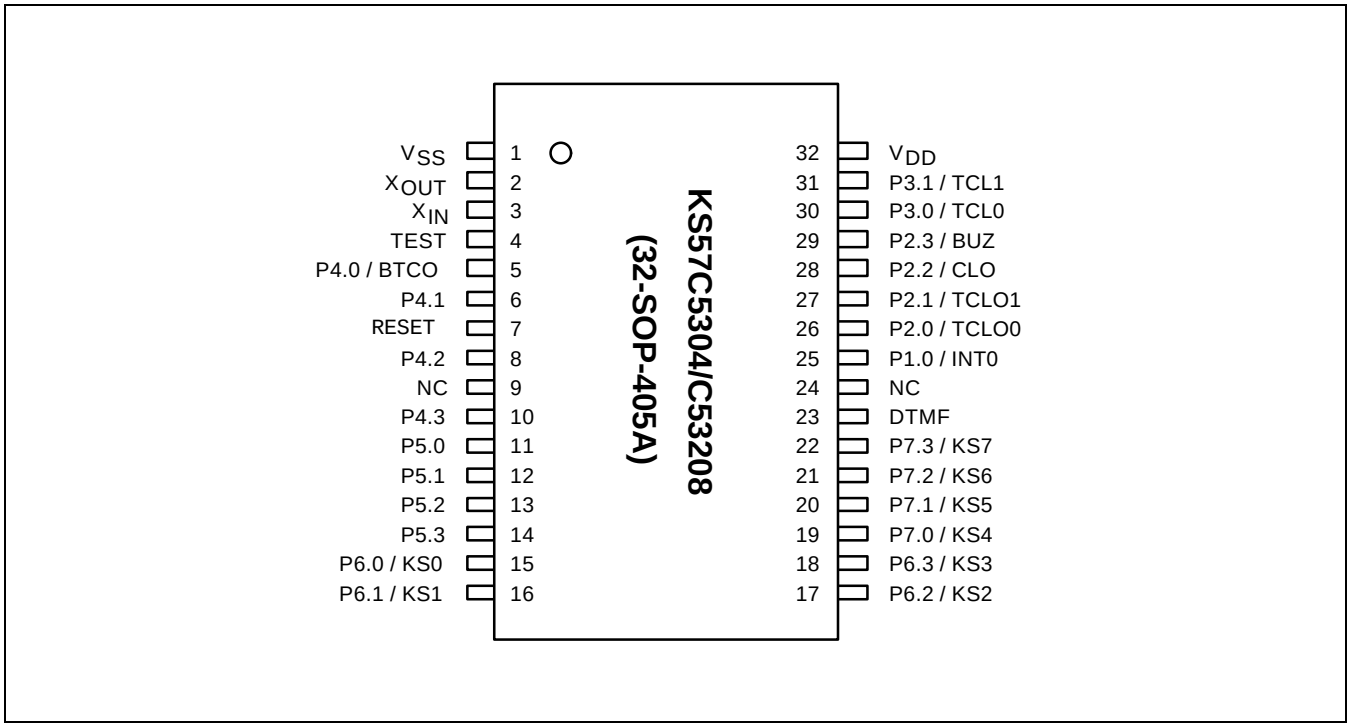


Figure 1–5. KS57C5304/C5308 Pin Assignment Diagrams (32–SOP)

PIN DESCRIPTIONS

Table 1-1. KS57C5204/C5208 Pin Descriptions

Pin Name	Pin Type	Reset Value	Description	Pin Number	Share Pin	Circuit Type
P1.0 P1.1 P1.2 P1.3	I	I	4-bit input port. 1-bit and 4-bit read and test is possible. Each pull-up resistors are assignable by software.	1 (39) 2 (40) 3 (41) 4 (42)	INT0 INT1 INT2 INT4	A-4
P2.0 P2.1 P2.2 P2.3	I/O	I	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output.	5 (43) 6 (44) 7 (1) 8 (2)	TCLO0 TCLO1 CLO BUZ	D-2
P3.0 P3.1 P3.2 P3.3			4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 2 and 3 can be paired to enable 8-bit data transfer.	9 (3) 10 (4) 19 (13) 20 (14)	TCL0 TCL1	D-4
P4.0 P4.1 P4.2 P4.3 P5.0–P5.3	I/O	I	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. N-channel open-drain or push-pull output can be selected by software (1-bit unit) Ports 4 and 5 can be paired to support 8-bit data transfer.	16 (10) 17 (11) 21 (15) 22 (17) 27–30 (22–25)	BTCO	E-2
P6.0–P6.3 P7.0–P7.3	I/O	I	4-bit I/O ports. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 6 and 7 can be paired to enable 8-bit data transfer.	31–34 (26–29) 35–38 (30–33)	KS0–KS3 KS4–KS7	D-4
P8.0–P8.3 P9.0–P9.2	I/O	I	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. Ports 8 and 9 can be paired to enable 8-bit data transfer.	23–26 (18–21) 40–42 (35–37)	–	D-2

Table 1-1. KS57C5204/C5208 Pin Descriptions (Continued)

Pin Name	Pin Type	Reset Value	Description	Pin Number	Share Pin	Circuit Type
DTMF	O	–	DTMF output.	39 (34)	–	G-6
BTCO	I/O	I	Basic timer clock output	16 (10)	P4.0	E-2
INT0 INT1	I	I	External interrupts. The triggering edge for INT0 and INT1 is selectable.	1 (39) 2 (40)	P1.0 P1.1	A-3
INT2	I	I	Quasi-interrupt with detection of rising edges	3 (41)	P1.2	A-3
INT4	I	I	External interrupt with detection of rising and falling edges.	4 (42)	P1.3	A-3
TCLO0	I/O	I	Timer/counter 0 clock output	5 (43)	P2.0	D-2
TCLO1	I/O	I	Timer/counter 1 clock output	6 (44)	P2.1	D-2
CLO	I/O	I	Clock output	7 (1)	P2.2	D-2
BUZ	I/O	I	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at the watch timer clock frequency of 4.19 MHz for buzzer sound	8 (2)	P2.3	D-2
TCL0	I/O	I	External clock input for timer/counter 0	9 (3)	P3.0	D-4
TCL1	I/O	I	External clock input for timer/counter 1	10 (4)	P3.1	D-4
KS0–KS3 KS4–KS7	I/O	I	Quasi-interrupt inputs with falling edge detection	31–34 (26–29) 35–38 (30–33)	P6.0–P6.3 P7.0–P7.3	D-4
V_{DD}	–	–	Power supply	11 (5)	–	–
V_{SS}	–	–	Ground	12 (6)	–	–
RESET	–	–	RESET signal	18 (12)	–	B
X_{in} X_{out}	–	–	Crystal, or ceramic oscillator signal for main system clock. (For external clock input, use X_{in} and input X_{in}'s reverse phase to X_{out})	14 (8) 13 (7)	–	–
TEST	–	–	Test signal input	15 (9)	–	–
NC	–	–	No connection	(16, 38)	–	–

NOTE: Parentheses indicate pin number for 44 QFP package.

Table 1-2. KS57C5304/C5308 Pin Descriptions

Pin Name	Pin Type	Description	Pin Number	Share Pin	Circuit Type
P1.0	I	4-bit input port. 1-bit and 4-bit read and test is possible. Each bit pull-up resistors are assignable.	23 (25)	INT0	A-4
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test is possible. Each individual pin can be assignable as input or output. 4-bit pull-up resisters are software assignable to input pins and are automatically disabled for output pins. Ports 2 and 3 can be paired to enable 8-bit data transfer.	24 (26) 25 (27) 26 (28) 27 (29)	TCLO0 TCLO1 CLO BUZ	D-2
P3.0 P3.1			28 (30) 29 (31)	TCL0 TCL1	D-4
P4.0 P4.1 P4.2 P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Each individual pin can be assignable as input or output. 4-bit pull-up resisters are software assignable to input pins and are automatically disabled for output pins. The N-channel open-drain or push-pull output can be selected by software (1-bit unit). Ports 4 and 5 can be paired to enable 8-bit data transfer.	5 (5) 6 (6) 8 (8) 9 (10) 10–13 (11–14)	BTCO	E-2
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. Each individual pin can be assignable as input or output. 4-bit pull-up resisters are software assignable to input pins and are automatically disabled for output pins. Ports 6 and 7 can be paired to enable 8-bit data transfer.	14–17 (15–18) 18–21 (19–22)	KS0–KS3 KS4–KS7	D-4

Table 1-1. KS57C5304/C5308 Pin Descriptions (Continued)

Pin Name	I/O Type	Description	Pin Number	Share Pin	Circuit Type
DTMF	O	DTMF output.	22 (23)	–	G-6
INT0	I	External interrupt input. The triggering edge for INT0 is selectable.	23 (25)	P1.0	A-3
TCLO0	I/O	Timer/counter 0 clock output	24 (26)	P2.0	D-2
TCLO1	I/O	Timer/counter 1 clock output	25 (27)	P2.1	D-2
CLO	I/O	Clock output	26 (28)	P2.2	D-2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at the watch timer clock frequency of 4.19 MHz for buzzer sound	27 (29)	P2.3	D-2
TCL0	I/O	External clock input for timer/counter 0	28 (30)	P3.0	D-4
TCL1	I/O	External clock input for timer/counter 1	29 (31)	P3.1	D-4
BTCO	I/O	Basic timer clock output	5 (5)	P4.0	E-2
V_{DD}	–	Power supply	30 (32)	–	–
V_{SS}	–	Ground	1 (1)	–	–
X_{in} X_{out}	–	Crystal, or ceramic oscillator signal for main system clock. (For external clock input, use X_{in} and input X_{in}'s reverse phase to X_{out})	3 (3) 2 (2)	–	–
NC	–	No connection	(9, 24)	–	–
TEST	–	Test signal input	4 (4)	–	–
RESET	–	RESET signal	7 (7)	–	B
KS0–KS3 KS4–KS7	I/O	Quasi-interrupt inputs with falling edge detection	14–17 (15–18) 18–21 (19–22)	P6.0– P6.3 P7.0– P7.3	D-4

NOTE: Parentheses indicate the pin number for 32-SOP package.