1 PRODUCT OVERVIEW

The KS57C5404/P5404 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With a versatile 8-bit timer/counter and a D/A converter, the KS57C5404/P5404 offers an excellent design solution for a wide variety of general-purpose applications.

Up to 17 pins of the 24-pin SOP packages can be dedicated to I/O. Four vectored interrupts provide fast response to internal and external events. In addition, the KS57C5404/P5404's advanced CMOS technology provides for very low power consumption and a wide operating voltage range.

FEATURES

Memory

512 × 4-bit RAM

4096 × 8-bit ROM

I/O Pins

17 Pins I/O

8-Bit Basic Timer

Programmable interval timer

Watch-dog timer

Interval 8-Bit Timer/Counter

Programmable interval timer

External event counter function

Timer/counter clock output to TCLO0 pin

Buzzer output

Four frequency outputs to BUZ pin

D/A Converter

8-bit D/A Converter

Interrupts

Two external interrupt vectors

Two internal interrupt vectors

One quasi-interrupt

Memory-Mapped I/O Structure

Data memory bank 15

Bit Sequential Carrier

Power-Down Modes

Idle mode (only CPU clock stops)

Stop mode (system clock stops)

Oscillation Sources

Crystal, ceramic for system clock

Crystal, ceramic:

0.4 ~ 6.0 MHz

CPU clock divider circuit
(by 4, 8, or 64)

Instruction Execution Times

0.95, 1.91, 15.3 µs

at 4.19 MHz

0.67, 1.33, 10.7 µs

at 6.0 MHz

Operating Temperature

- 40 °C to 85 °C

Operating Voltage Range

1.8 V to 5.5 V (at 4.19MHz)

2.7 V to 5.5 V (at 6MHz)

Package Type

24 SOP-375

24SDIP-300

OTP INTERFACE PROTOCOL SPEC

Serial OTP Ç Ý Ø ÈÂ Á ¶

BLOCK DIAGRAM

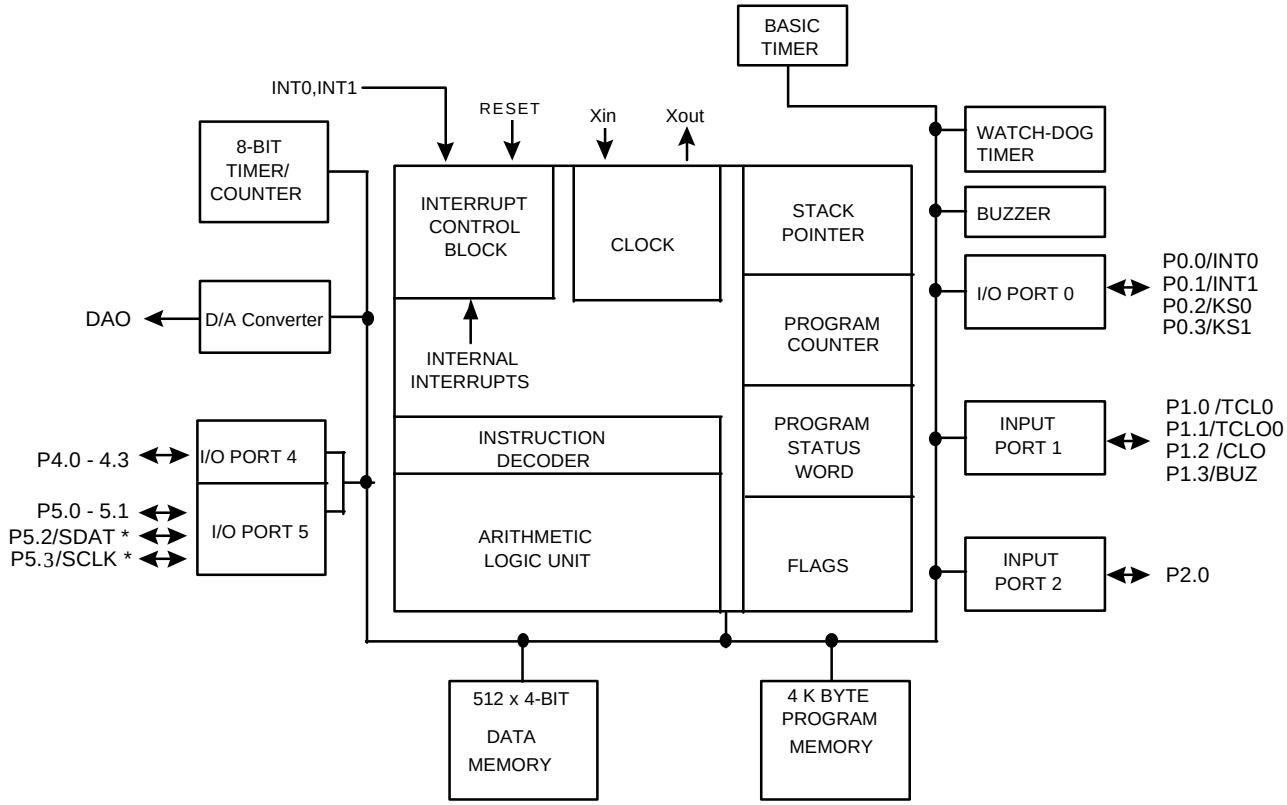

Figure 1 - 1. KS57C5404/P5404 Block Diagram

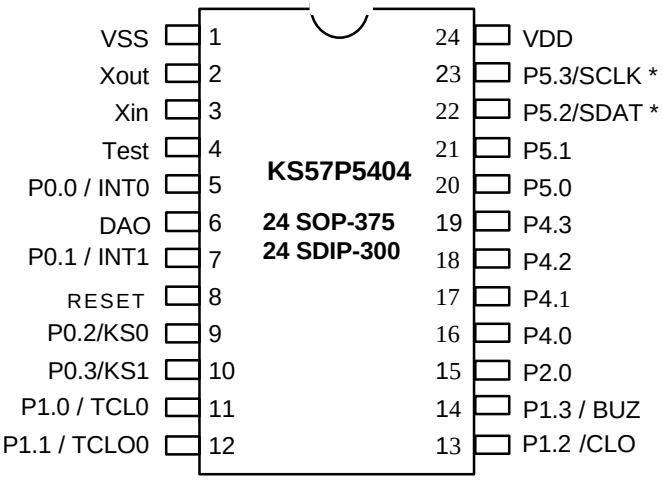

Figure 1 - 2. KS57C5404/P5404 Pin Assignment Diagrams

* : SDAT and SCLK is available in OTP version

PIN DESCRIPTIONS

Table 1 - 1. KS57C5404/P5404 Pin Descriptions

Pin Name	Pin Type	Description	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	INT0 INT1 KS0 KS1
P1.0 P1.1 P1.2 P1.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Pins are individually configurable as input or output.	TCL0 TCLO0 CLO BUZ
P2.0	I/O	1-bit I/O port. 1-bit or 4-bit read/write and test is possible. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins.	
P4.0-P4.3 P5.0-P5.1 P5.2 P5.3	I/O	4-bit I/O ports. 1-, 4-, or 8-bit read/write and test is possible. Pins are individually configurable as input or output. Pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. The N-Channel open drain or push-pull output can be selected by software(1-bit unit).	- - SDAT SCLK
INT0	I/O	External interrupts with rising/falling edge detection	P0.0
INT1	I/O	External interrupts with rising/falling edge detection	P0.1
KS0 KS1	I/O	Quasi-interrupt input with falling edge detection	P0.2 P0.3
TCL0	I/O	External clock input for timer/counter	P1.0
TCLO0	I/O	Timer/counter clock output	P1.1
CLO	I/O	CPU clock output	P1.2
BUZ	I/O	0.5kHz, 1 kHz, 2 kHz, or 4 kHz frequency output at 4.19 MHz for buzzer sound	P1.3
DAO	O	8 Bit D/A Converter output	-
SDAT *	I/O	Serial data Read/Write	P5.2
SCLK *	I/O	Serial clock input	P5.3
V_{DD}	-	Main power supply	-
V_{SS}	-	Ground	-
RESET	I	Reset signal	-
TEST	I	Test signal input (must be connected to V_{SS})	-
X_{in}, X_{out}	-	Crystal, ceramic oscillator signal for system clock	-

* : SDAT and SCLK is available in OTP version

Table 1- 2. Overview of KS57C5404/P5404 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
V_{SS}	-	-	-	-
Xout, Xin	-	-	-	-
TEST	-	I	-	-
P0.0, P0.1	INT0, INT1	I/O	Input	D-4
RESET	-	I	-	B
P0.2 P0.3	KS0 KS1	I/O	Input	D-4
P1.0 P1.1 P1.2 P1.3	TCL0 TCLO0 CLO BUZ	I/O	Input	D-2
P2.0	-	I/O	Input	D-2
DAO	-	O	Output	-
P4.0 - P4.3	-	I/O	Input	E-2
P5.0 - P5.3	-	I/O	Input	E-2
V_{DD}	-	-	-	-