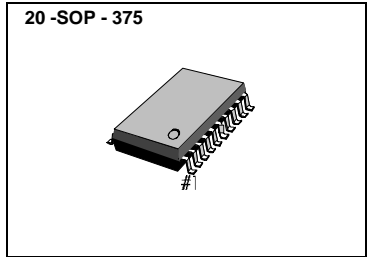


KS7220

VERTICAL DRIVER FOR CCD

GENERAL DESCRIPTION

The KS7220 is designed for Driving Vertical register of CCD Image Sensor.



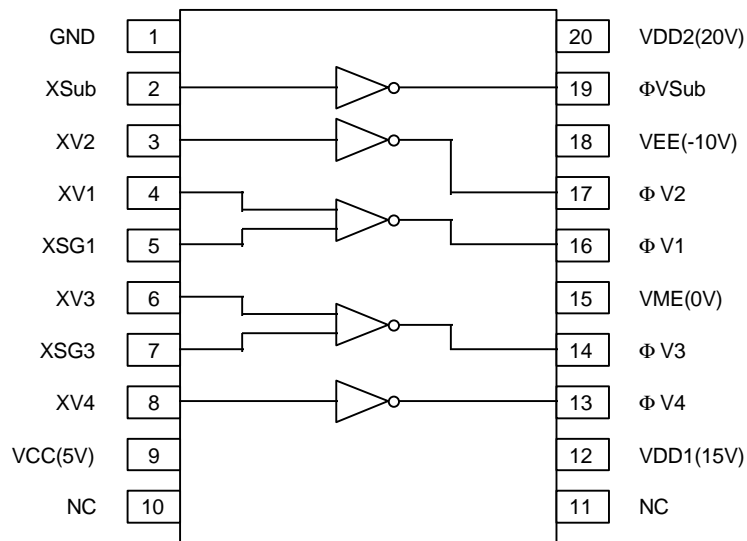
FEATURES

- Includes 4-Channel Vertical Clock Driver
- Includes 1-Channel Sub Driver
- Applied to B/W & Color
- Applied to NTSC & PAL

ORDERING INFORMATION

Device	Package	Operating Temperature
KS7220	20-SOP-375	- 20 °C ~ +75 °C

BLOCK DIAGRAM



PIN DESCRIPTION

No	Symbol	I/O	Description	Remark
1	GND	-	GROUND	
2	XSUB	I	OUTPUT CONTROL (Vsub)	
3	XV2	I	OUTPUT CONTROL (ϕ V2)	
4	XV1	I	OUTPUT CONTROL (ϕ V1)	
5	XSG1	I	OUTPUT CONTROL (ϕ V1)	
6	XV3	I	OUTPUT CONTROL (ϕ V3)	
7	XSG3	I	OUTPUT CONTROL (ϕ V3)	
8	XV4	I	OUTPUT CONTROL (ϕ V4)	
9	VCC	I	POWER (5V)	
10	NC	-	NO CONNECTION	
11	NC	-	NO CONNECTION	
12	VDD1	-	POWER (15V)	
13	ϕ V4	O	High Voltage Output (2 level :VME, VEE)	
14	ϕ V3	O	High Voltage Output (3 level :VME, VEE, VHH)	
15	VME	-	POWER (0V)	
16	ϕ V1	O	High Voltage Output (3 level :VME, VEE, VHH)	
17	ϕ V2	O	High Voltage Output (2 level : VME, VEE)	
18	VEE	-	POWER (-10V)	
19	ϕ VSub	O	High Voltage Output (2 level :VEE, VHH)	
20	VDD2	-	POWER (20V)	

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	GND,VCC,VME,VDD1,VEE	VDD2-35	VDD2+0.3	V
Input Voltage	VIN	GND-0.3	VDD2+0.3	
Output Voltage	ϕ V1,V3	VEE-0.3	VDD2+0.3	
	ϕ V2,V4	VEE-0.3	VDD2+0.3	
	ϕ VSub	VEE-0.3	VDD2+0.3	
Operating Temperature	Topr	-20	+75	°C
Storage Temperature	Tstg	-40	+125	

LOGIC FUNCTION TABLE

XSG1,3	XV1,3	ϕ V1, 3
H	L	VME
H	H	VEE
L	L	VDD1
L	H	HIMP

XV2,4	ϕ V2, 4
H	VEE
L	VME

XSub	ϕ Vsub
H	VEE
L	VDD2

- * HIMP = HIGH IMPEDANCE
- * VME = 0V
- * VDD1 = 15V
- * VDD2 = 20V



ELECTRICAL CHARACTERISTICS(V_{CC} = 5V, V_{EE} = -10V, V_{ME} = 0V, V_{DD1} = 15V, V_{DD2} = 20V, T_a = 25 °C)

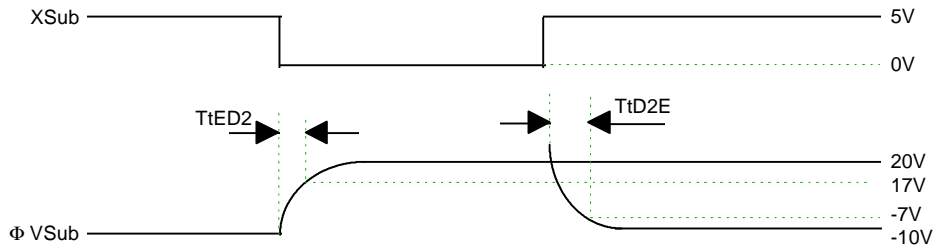
Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Input High Voltage	V _{IH}		3.5	-	-	V
Input Low Voltage	V _{IL}		-	-	1.0	
Input Current	I _{IN}		-	1.0	-	μA
Output Current	I _{OEE}	ΦV ₁₋₄ =-9.5V	-	-36	-24	mA
	I _{OME1}	ΦV ₁₋₄ =-0.5V	10	15	-	
	I _{OME2}	ΦV _{1.3} = 0.5V	-	-15	-10	
	I _{ODD1}	ΦV _{1.3} =14.5V	12	18	-	
	I _{OSDD2}	ΦV _{sub} =19.5V	8	12	-	
	I _{OSEE}	ΦV _{sub} =-9.5V	-	-18	-12	

TRANSIENT CHARACTERISTICS(V_{CC}=5V, V_{EE}=-10V, V_{ME}=0V, V_{DD1}=15V, V_{DD2}=20V, T_a=25°C)

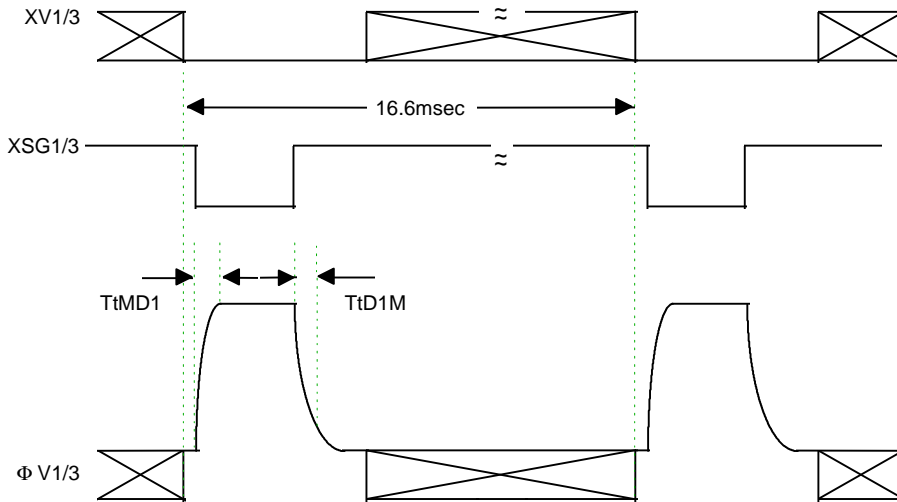
Characteristics	Transient	Symbol	Typ	Max	Unit
Rising Time	V _{EE} → V _{ME} (-0.5V)	T _{tEM}	600	1000	nSEC
Falling Time	V _{ME} → V _{EE} (-9.5V)	T _{tME}	300	500	
Rising Time	V _{EE} → V _{DD1} (-14V)	T _{tMD1}	600	1000	
Falling Time	V _{DD1} → V _{ME} (1.0V)	T _{tD1M}	700	1000	
Rising Time	V _{EE} → V _{DD2} (17.0V)	T _{tED2}	120	200	
Falling Time	V _{DD} → V _{CC} (-7.0V)	T _{tD2E}	120	200	

TIMING DIAGRAM

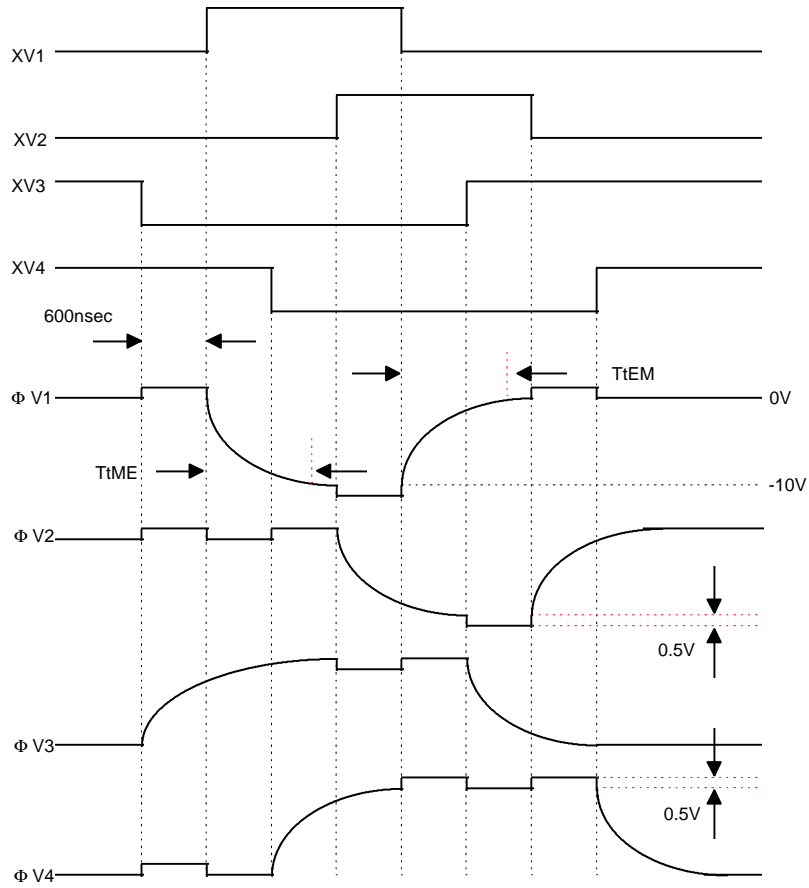
1) TIMING CHART 1 (XSub ----> Φ VSub)



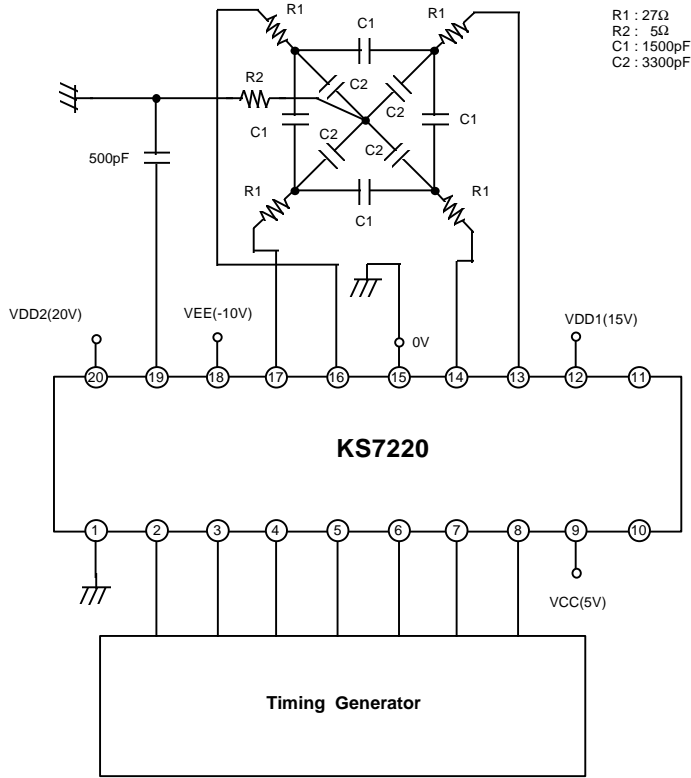
2) TIMING CHART 2 (XV1/3, XSG1/3 ----> Φ V1/3)



3) TIMING CHART 3 (XV1,2,3,4 --> ΦV1,2,3,4)

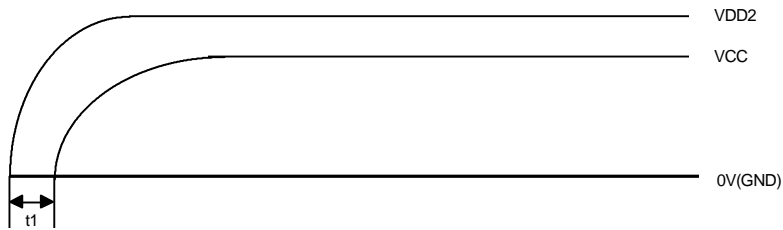


APPLICATION CIRCUIT



VDD1,VDD2,VEE POWER SUPPLIES AT THE APPLICATION CIRCUIT

VCC,VDD2 Supplies at the application under the following condition.



- * $0 < t_1$
- * Care for ; if $t_1 < 0$ then device must be damaged by the Latch-up

PACKAGE DIMENSION

