1 PRODUCT OVERVIEW

SAM87RI PRODUCT FAMILY

Samsung's SAM87RI family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A dual address/data bus architecture and a large number of bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations. Many SAM87RI microcontrollers have an external interface that provides access to external memory and other peripheral devices.

KS86C6004/C6008/P6008 MICROCONTROLLER

The KS86C6004/C6008/P6008 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM87RI CPU core.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The KS86C6004 has 4 K bytes of program memory on-chip and KS86C6008 has 8 K bytes.

Using the SAM87RI design approach, the following peripherals were integrated with the SAM87RI core:

— Five configurable I/O ports (32 pins)

— 12 bit-programmable pins for external interrupts

— 8-bit timer/counter with three operating modes

— Low speed USB function

The KS86C6004/C6008/P6008 is a versatile microcontroller that can be used in a wide range of low speed USB support general purpose applications. It is especially suitable for use as a keyboard controller and is available in a 42-pin SDIP and a 44-pin QFP package.

OTP

The KS86C6004/C6008 microcontroller is also available in OTP (One Time Programmable) version, KS86P6008. KS86P6008 microcontroller has an on-chip 8-Kbyte one-time-programmable EPROM instead of masked ROM. The KS86P6008 is comparable to KS86C6004/C6008, both in function and in pin configuration.

FEATURES

CPU

- SAM87RI CPU core

Memory

- 8-Kbyte internal program memory (ROM)
- 208-byte RAM

Instruction Set

- 41 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 1.0 µs at 6 MHz f_{OSC}

Interrupts

- 25 interrupt sources with one vector, each source has its pending bit
- One level, one vector interrupt structure

Oscillation Circuit

- 6 MHz crystal/ceramic oscillator
- External clock source (6 MHz)

General I/O

- Bit programmable five I/O ports (32 pins total)

Timer/Counter

- One 8-bit basic timer for watchdog function and programmable oscillation stabilization interval generation function
- One 8-bit timer/counter with Compare/Overflow

USB Serial Bus

- Compatible to USB low speed (1.5 Mbps) device 1.0 specification.
- Serial bus interface engine (SIE)
  - — Packet decoding/generation
  - — CRC generation and checking
  - — NRZI encoding/decoding and bit-stuffing
- 8 bytes each receive/transmit USB buffer

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 4.5 V to 5.5 V

Package Types

- 42-pin SDIP
- 44-pin QFP

BLOCK DIAGRAM

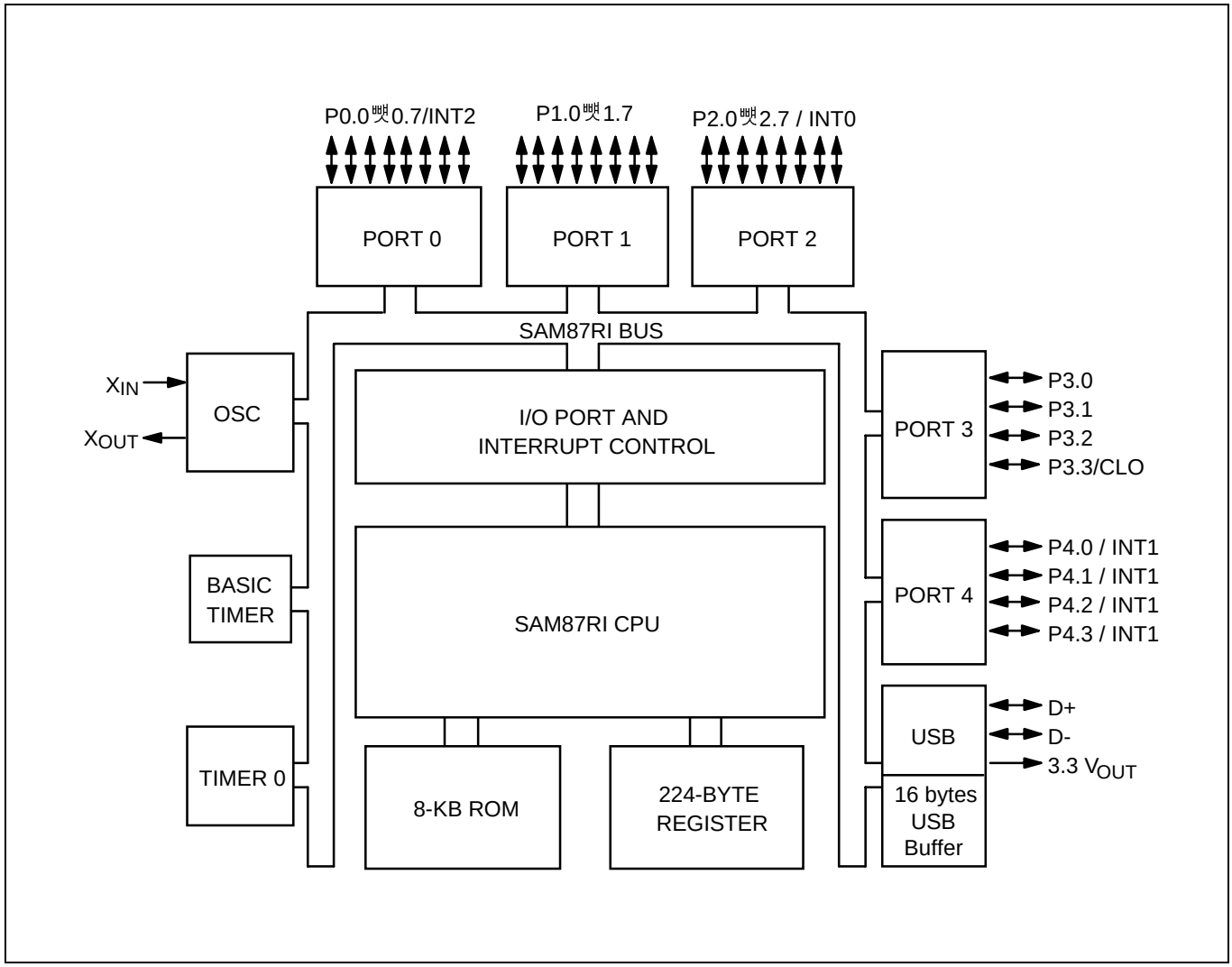

Figure 1-1. Block Diagram

PIN ASSIGNMENTS

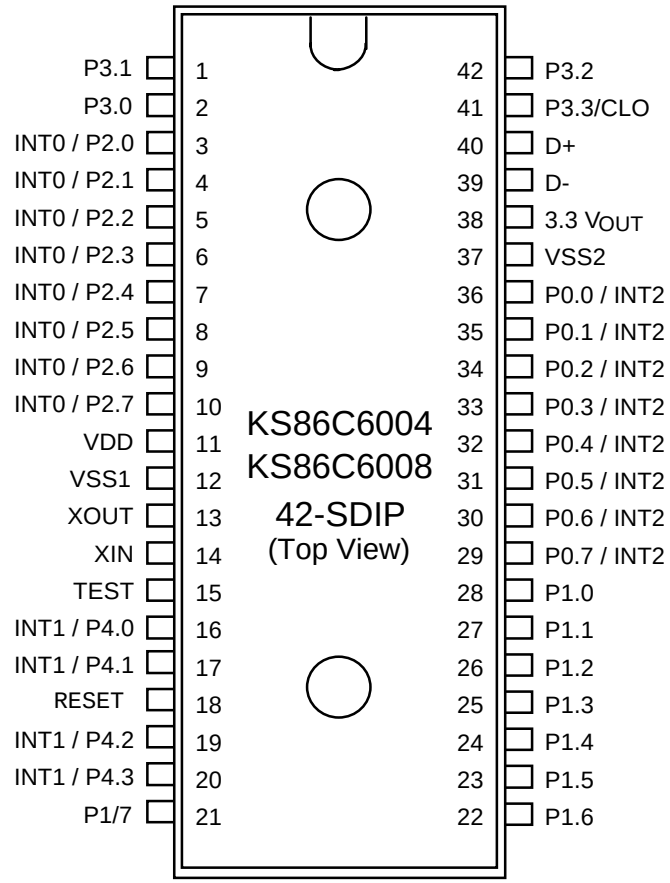

Figure 1-2. Pin Assignment Diagram (42-Pin SDIP Package)

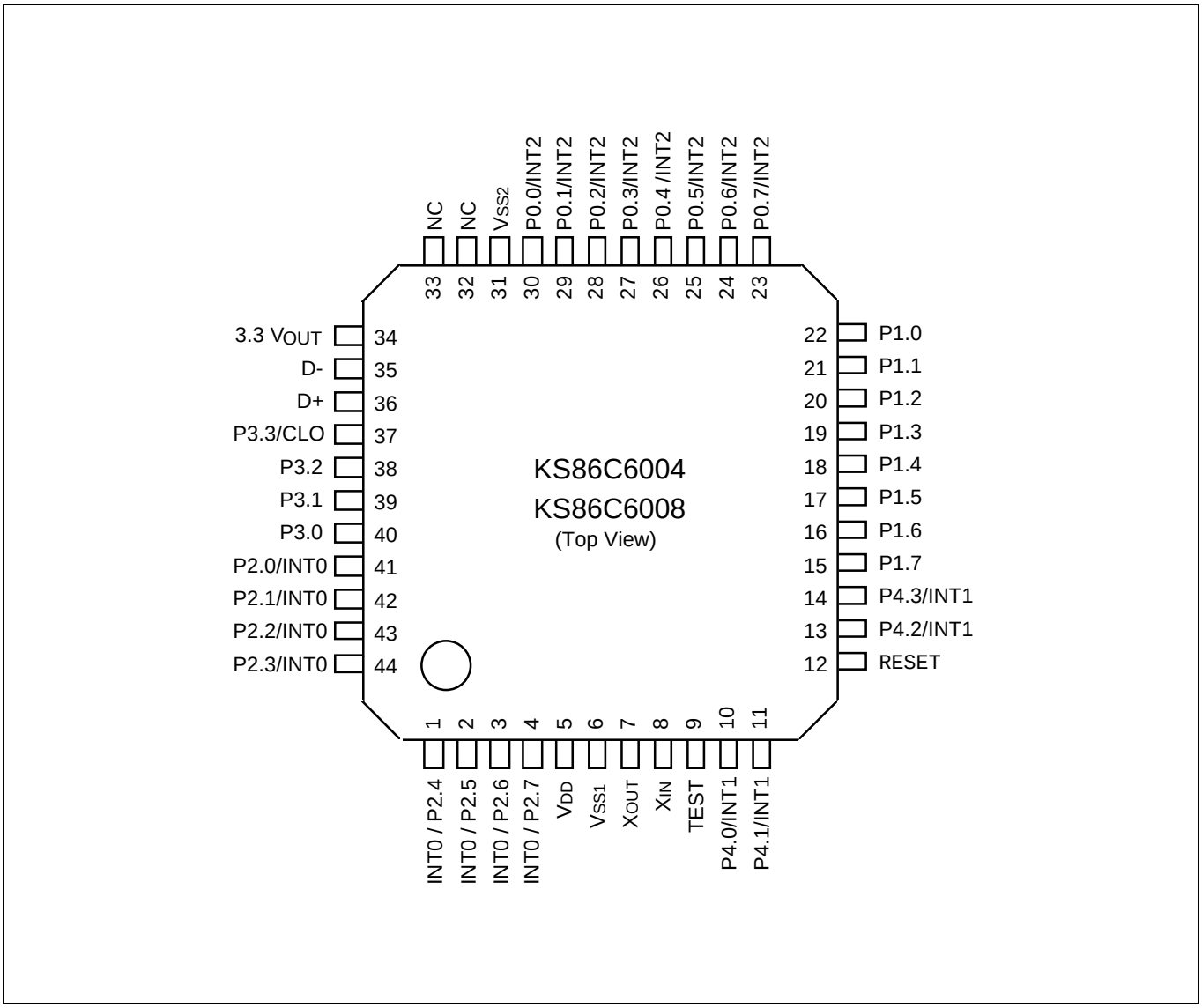

Figure 1-3. Pin Assignment Diagram (44-Pin QFP Package)

PIN DESCRIPTIONS

Table 1-1. KS86C6004/C6008/P6008 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Number	Pin Numbers	Share Pins
P0.0-P0.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Port0 can be individually configured as external interrupt inputs. Pull-up resistors are assignable by software.	B	36–29 (30–23)	INT2
P1.0-P1.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Pull-up resistors are assignable by software.	B	28–21 (22–15)	–
P2.0-P2.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Port2 can be individually configured as external interrupt inputs. Pull-up resistors are assignable by software.	B	3–10 (41–44, 1–4)	INT0
P3.0-P3.3	I/O	Bit-programmable I/O port for Schmitt trigger input, open-drain or push-pull output. P3.3 can be used to system clock output(CLO) pin.	C	2, 1, 42, 41 (40–37)	P3.3/CLO
P4.0-P4.3	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output or push-pull output. Port4 can be individually configured as external interrupt inputs. In output mode, pull-up resistors are assignable by software. But in input mode, pull-up resistors are fixed.	D	16, 17, 19, 20 (10, 11, 13, 14)	INT1
D+/D-	I/O	Only be used USB tranceive/receive port; D+/D-.	–	40–39 (36-35)	–
3.3 V_{OUT}	–	3.3 V output from internal voltage regulator	–	38 (34)	–
X_{IN}, X_{OUT}	–	System clock input and output pin (crystal/ceramic oscillator, or external clock source)	–	14, 13 (8, 7)	–
INT0 INT1 INT2	I	External interrupt for bit-programmable port0, port2 and port4 pins when set to input mode.	–	3–10, 16,17, 19, 20, 29–36 (30–23, 41–44, 1–4, 10, 11, 13, 14)	PORT2/ PORT4/ PORT0
RESET	I	RESET signal input pin. Schmitt trigger input with internal pull-up resistor.	A	18 (12)	–
TEST	I	Test signal input pin (for factory use only; must be connected to V_{SS})	–	15 (9)	–
V_{DD}	–	Power input pin	–	11 (5)	–
V_{SS1},V_{SS2}	–	Vss1 is a ground power for CPU core. Vss2 is a ground power for I/O and OSC block.	–	12, 37 (6, 31)	–
NC	–	No connection	–	– (32, 33)	–

NOTE: Pin numbers shown in parenthesis '( )' are for the 44-QFP package; others are for the 42-SDIP package.

PIN CIRCUITS

Table 1-2. Pin Circuit Assignments for the KS86C6004/C6008/P6008

Circuit Number	Circuit Type	KS86C6004/C6008/P6008 Assignments
A	I	RESET signal input
B	I/O	Ports 0, 1, and 2
C	I/O	Port 3
D	I/O	Port 4

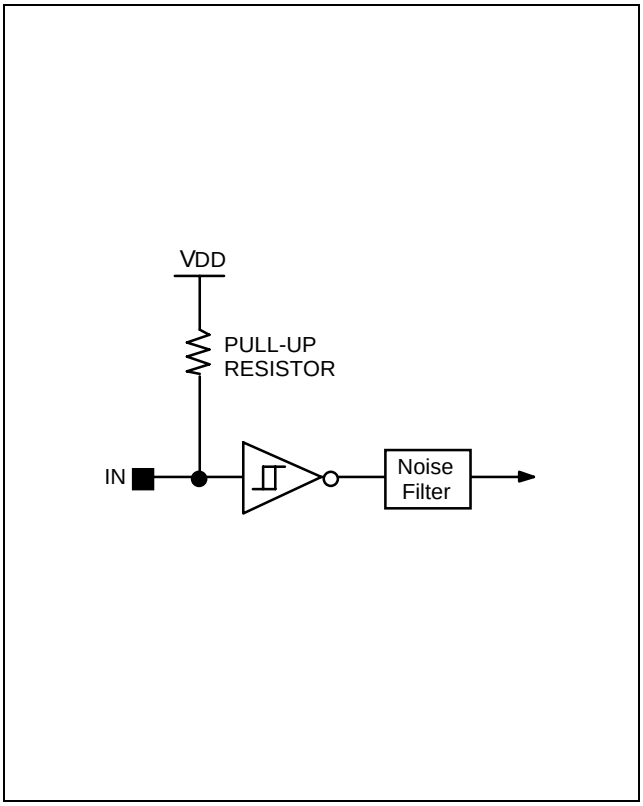

Figure 1-4. Pin Circuit Type A (RESET)

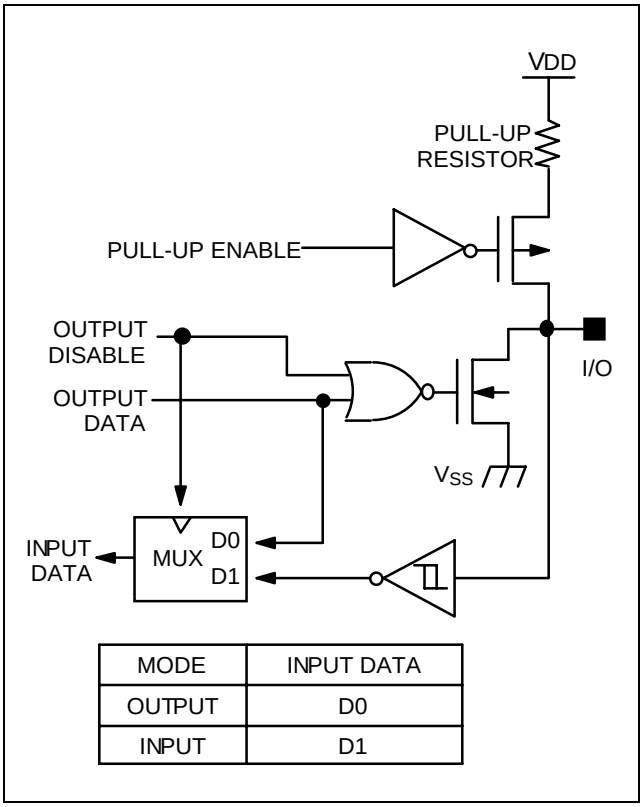

Figure 1-5. Pin Circuit Type B (Ports 0, 1 and 2)