1 PRODUCT OVERVIEW

SAM8 PRODUCT FAMILY

Samsung's SAM87 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture

— Selectable CPU clock sources

— Idle and Stop power-down mode release by interrupt

— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of six CPU clocks) can be assigned to specific interrupt levels.

KS88C0716/P0716 MICROCONTROLLERS

KS88C0716/P0716 single-chip 8-bit microcontrollers are based on the powerful SAM87 CPU architecture. The internal register file is logically expanded to increase the on-chip register space. The KS88C0716 has 16-Kbyte mask-programmable ROM. The KS88P0716 has 16-Kbyte one-time-programmable EPROM.

Following Samsung's modular design approach, the following peripherals are integrated with the SAM87 core:

— Seven programmable I/O ports (total 56 pins)

— One 8-bit basic timer for oscillation stabilization and watchdog functions

— One synchronous operating mode and three full-duplex asynchronous UART modes

— Two 8-bit timers with interval timer and PWM modes

— Two 16-bit general-purpose timer/counters

OTP

The KS88C0716 microcontroller is also available in OTP (One Time Programmable) version, KS88P0716. KS88P0716 microcontroller has an on-chip 16-Kbyte one-time-programmable EPROM instead of masked ROM. The KS88P0716 is comparable to KS88C0716, both in function and in pin configuration.

FEATURES

CPU

- SAM87 CPU core

Memory

- 272-byte general purpose register area
- 16-Kbyte internal program memory
- ROM-less operating mode

External Interface

- 64-Kbyte external data memory area
- 64-Kbyte external program memory area (ROM-less mode)

Instruction Set

- 78instructions
- IDLE and STOP instructions for power-down mode

Instruction Execution Time

- 500 ns at 12 MHz f_{CPU} (Min.)

Interrupts

- 17 interrupt sources
- 17 interrupt vectors
- Eight interrupt levels
- Fast interrupt processing

General I/O

- Four nibble-programmable ports
- One bit-programmable port
- Two bit-programmable ports for external interrupts

Timers

- Two 8-bit timers with interval timer and PWM modes

Timer/Counters

- Two 16-bit general-purpose timer/counters

Basic Timer

- One 8-bit basic timer (BT) for oscillation stabilization control and watch dog timer function.

Serial Port

- One synchronous operating mode and three full-duplex asynchronous UART modes

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 2.7 V to 5.5 V

Package Types

- 64-pin SDIP, 64-pin QFP

Table 1-1. Comparison Table

Feature	KS88C0116	KS88C0716
Core	SAM8	SAM87
ROM	16 K bytes	Same
RAM	272 bytes	Same
I/O	54	56 (add two pins)
Port 6	Open drain (9 V drive)	Normal C-MOS output
I/O option	None	Same
Timer	8-bit back-up timer	None
	Timer A, B — 8-bit — Interval/PWM mode — Timer A match interrupt	Same (some differ in interval mode, see manual)
	Timer C, D — Gate function — Timer/counter	Same
Watchdog timer	None	Watchdog timer (with BT)
SIO	UART — 8-bit/9-bit UART — SIO	Same
Interrupt	External × 12 — P2.4–P2.7, P4.0–P4.7	Same
	Internal × 6 — Timer A, C, D, SI, SO, Back-up	Internal × 5 — Timer A, C, D, SI, SO
Power down	Stop/idle	Same
Oscillator	Crystal, ceramic	Same
CPU clock divider	1/2	1/1, 1/2, 1/8, 1/16
Execution time (Min.)	0.6 µs at 20 MHz (f_{CPU} = 10 MHz)	0.5 µs at 12 MHz (f_{CPU} = 12 MHz)
Operating frequency	Max. 20 MHz (f_{CPU} = 10 MHz)	Max. 12 MHz (at 4.5 V) (2) Max. 4 MHz (at 2.7 V)
Operating voltage	4.5–5.5 V	2.7–5.5 V at 4 MHz 4.5–5.5 V at 12 MHz
OTP/MTP	MTP	OTP
Pin assignment	–	Different
Package	64SDIP/64QFP	Same

NOTES:

1. The KS88C0716 can replace the KS88C0116. Their functions are mostly the same, but there are some differences. Table 1-1 shows the comparison of KS88C0716 and KS88C0116.
2. Operating frequency is maximum CPU clock; the maximum oscillation frequency is 22.1184 MHz.

BLOCK DIAGRAM

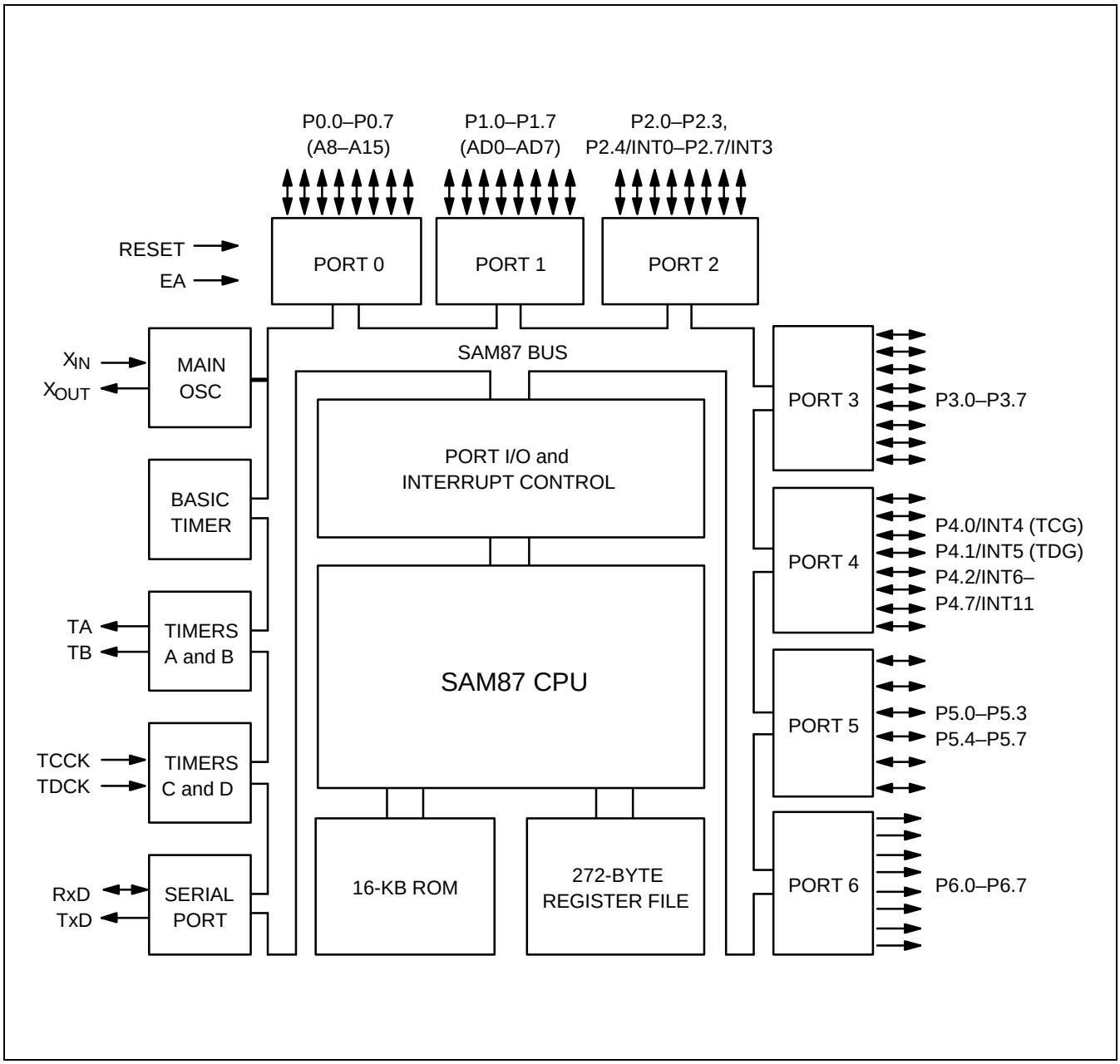

Figure 1-1. KS88C0716 Block Diagram

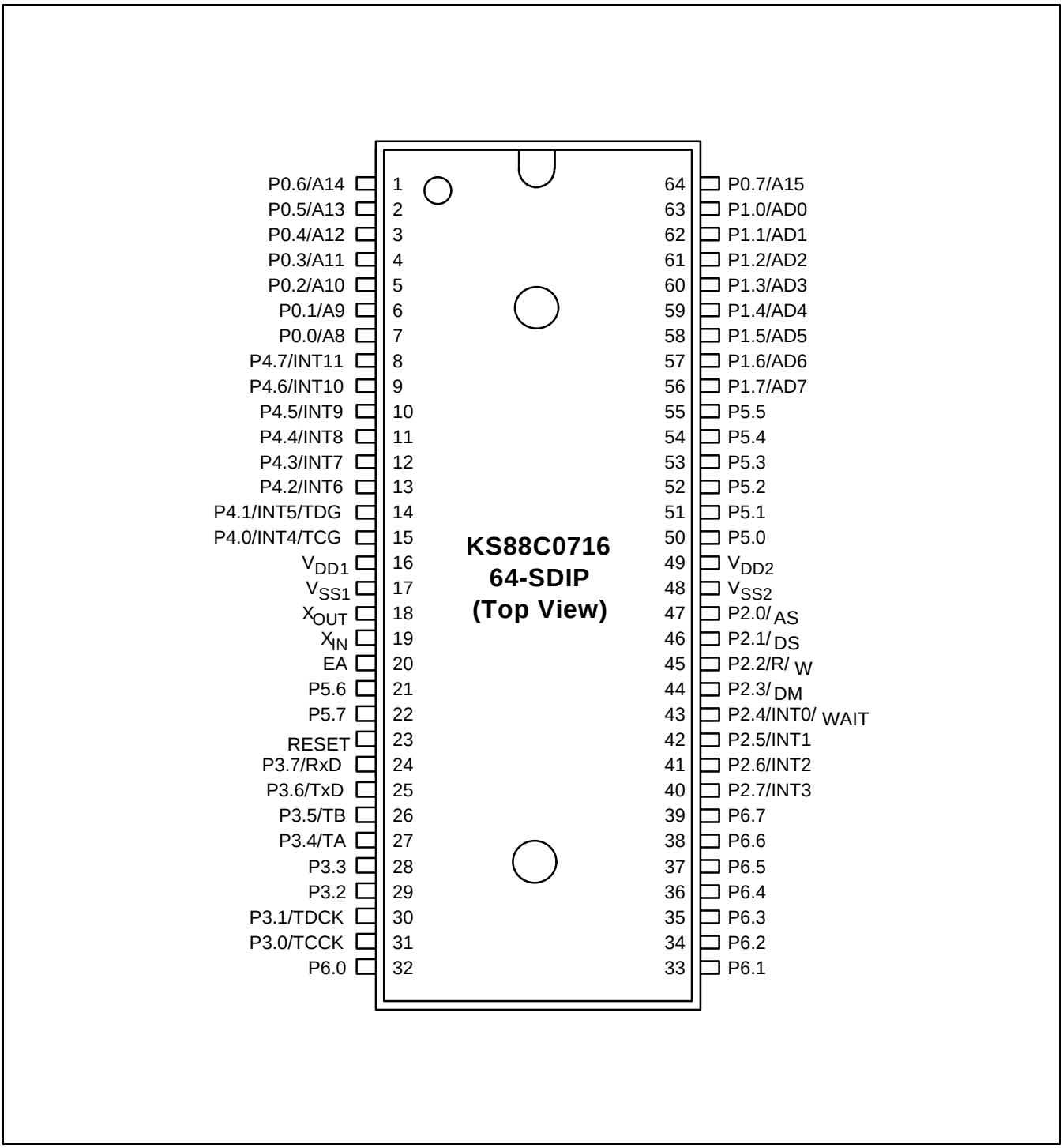

Figure 1-2. KS88C0716 Pin Assignments (64-SDIP)

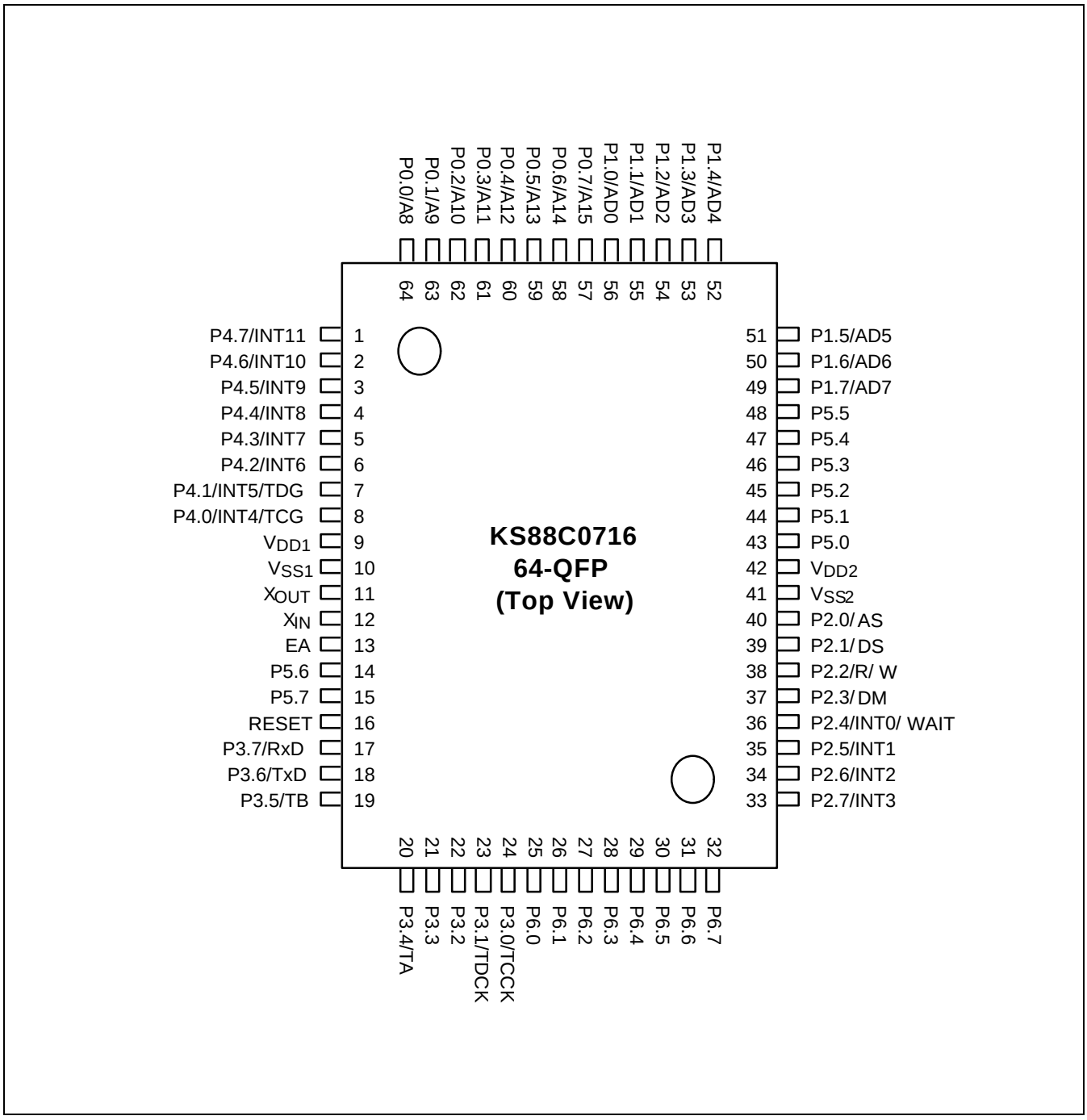

Figure 1-3. KS88C0716 Pin Assignments (64-QFP)

Table 1-2. KS88C0716 Pin Descriptions (64-SDIP)

Pin Name	Pin Type	Pin Description	Circuit Number	SDIP Pin Number	Share Pins
P0.0–P0.7	I/O	I/O port with nibble-programmable pins; Input or push-pull, open-drain output and software assignable pull-ups; also configurable as external interface address lines A8-A15.	E	1–7, 64	A8–A15
P1.0–P1.7	I/O	Same general characteristics as port 0; also configurable as external interface address/data lines AD0–AD7.	E	56–63	AD0–AD7
P2.0–P2.3 P2.4–P2.7	I/O	I/O port with bit-programmable pins; Input or push-pull output. Lower nibble pins 0–3 are configurable for external interface signals; upper nibble pins 4–7 are bit-programmable for external interrupts INT0–INT3. P2.4 can also be used for external WAIT input.	D-1 (lower nibble); D-1 (upper nibble; with noise filter)	40–47	AS, DS, DM, R/W INT0–INT3, WAIT
P3.0–P3.7	I/O	I/O port with bit-programmable pins; Input or push-pull output. Alternate functions include software-selectable UART transmit and receive on pins 3.7 and 3.6, timer B and timer A outputs at pins 3.5 and 3.4, and timer D and C clock inputs at pins 3.1 and 3.0.	D-1	24– 31	TCCK, TDCK, TA, TB, TxD, RxD
P4.0–P4.7	I/O	I/O port with bit-programmable pins; Input or push-pull output; software-assignable pull-ups. Alternate functions include external interrupt inputs INT4-INT11 (with interrupt enable and pending control) and timer C and D gate input at P4.0 and P4.1.	D (with noise filter)	8–15	INT4–INT11, TCG, TDG
P5.0–P5.7	I/O	I/O port with nibble-programmable pins; Input or push-pull, open-drain output; software-assignable pull-ups.	E	21, 22, 50–55	–
P6.0–P6.7	O	Output port with nibble-programmable pins; push-pull, open-drain output; software-assignable pull-ups.	E-8	32–39	–
RxD	I/O	Bi-directional serial data input pin	–	24	P3.7
TxD	I/O	Serial data output pin	–	25	P3.6
TA, TB	I/O	Timer A and B output pins	4	27, 26	P3.4, P3.5
TCCK, TDCK	I/O	Timer C and D external clock input pins	D-1	30, 31	P3.0, P3.1
INT0–INT3	I/O	External interrupts. I/O pin 2.4 (share pin with INT0) is also configurable as a WAIT signal input pin for the external interface.	D-1 (with noise filter)	40–43	P2.4–P2.7

Table 1-2. KS88C0716 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Number	SDIP Pin Number	Share Pins
INT4–INT11	I/O	Bit-programmable external interrupt input pins with interrupt pending and enable /disable control	D (with noise filter)	8–15	P4.0–P4.7
X_{IN}, X_{OUT}	–	System clock input and output pins	–	18, 19	–
RESET	I	System reset pin (internal pull-up: 280 KΩ)	B	23	–
EA	I	External access (EA) pin with three modes: 0 V: Normal operation (internal ROM) 5 V: ROM-less operation (external interface)	–	20	–
V_{DD2}, V_{SS2}	–	Power input pins for port output (external)	–	49, 48	–
V_{DD1}, V_{SS1}	–	Power input pins for CPU (internal)	–	16, 17	–