1 PRODUCT OVERVIEW

KS88-SERIES MICROCONTROLLERS

Samsung's KS88 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Important CPU features include:

— Efficient register-oriented architecture
— Selectable CPU clock sources
— Idle and Stop power-down mode release by interrupt
— Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

KS88C0916/P0916 MICROCONTROLLER

The KS88C0916/P0916 single-chip CMOS microcontroller is fabricated using a highly advanced CMOS process and is based on Samsung's newest CPU architecture.

The KS88C0916 is the microcontroller which has 16-Kbytes mask-programmable ROM.

The KS88P0916 is the microcontroller which has 16-Kbytes one-time-programmable EPROM.

Using a proven modular design approach, Samsung engineers developed the KS88C0916/P0916 by integrating the following peripheral modules with the powerful SAM87 core:

— Four programmable I/O ports, including three 8-bit ports and one 2-bit port, for a total of 26 pins.
— Twelve bit-programmable pins for external interrupts.
— One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).
— One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.
— One 8-bit counter with auto-reload function and one-shot or repeat control.

The KS88C0916 is a versatile general-purpose microcontroller. It is currently available in a 32-pin SOP and SDIP package.

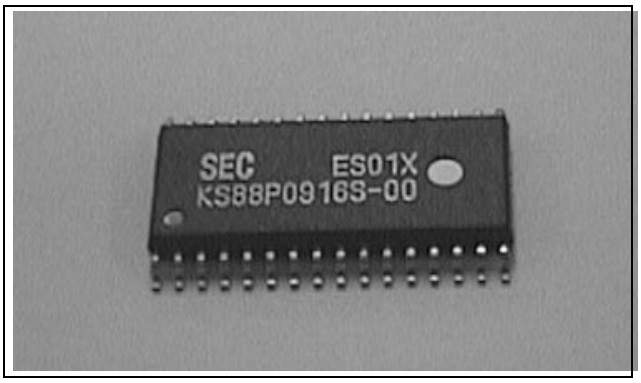

Figure 1-1. KS88C0916 Microcontroller

FEATURES

CPU

- SAM87 CPU core

Memory

- 16-Kbyte internal program memory (ROM)
- 317-byte internal register file

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 750 ns at 8-MHz f_{OSC} (minimum)

Interrupts

- Six interrupt levels and 18 interrupt sources
- 15 vectors (14 sources have a dedicated vector address and four sources share a single vector)
- Fast interrupt processing feature (for one selected interrupt level)

I/O Ports

- Three 8-bit I/O ports (P0–P2) and one 2-bit port (P3) for a total of 26 bit-programmable pins
- Twelve input pins for external interrupts

Timers and Timer/Counters

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function
- One 8-bit timer/counter (Timer 0) with three operating modes; Interval, Capture and PWM
- One 16-bit timer/counter (Timer 1) with two operating modes; Interval and Capture

Carrier Frequency Generator

- One 8-bit counter with auto-reload function and one-shot or repeat control (Counter A)

Operating Temperature Range

- – 20°C to + 85°C

Operating Voltage Range

- 2.0 V to 5.5 V at 4 MHz f_{OSC}
- 2.4 V to 5.5 V at 8 MHz f_{OSC}

Package Type

- 32-pin SOP
- 32-pin SDIP

BLOCK DIAGRAM

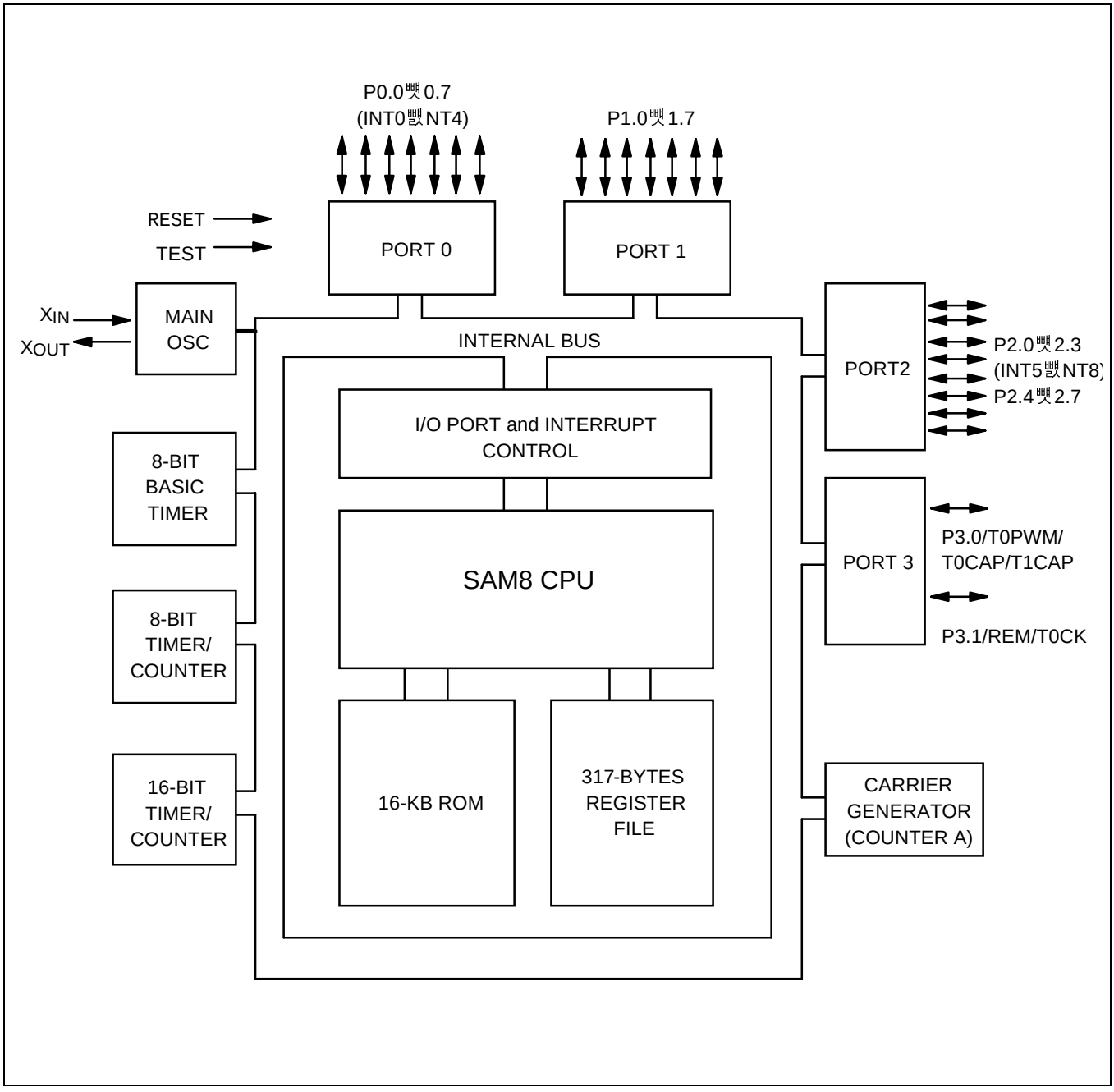

Figure 1-2. Block Diagram

PIN ASSIGNMENTS

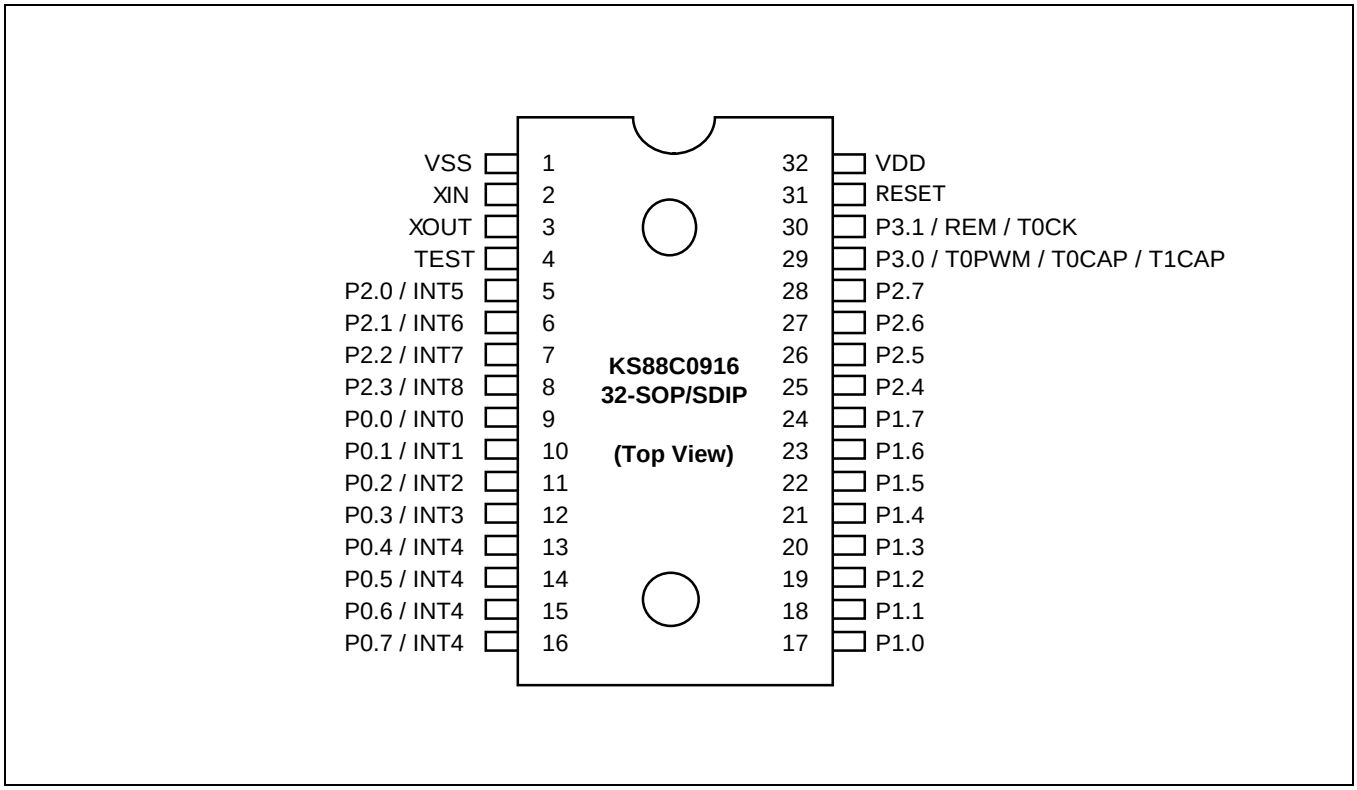

Figure 1-3. Pin Assignment Diagram (32-Pin SOP/SDIP Package)

PIN DESCRIPTIONS

Table 1-1. Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	Pin No.	Shared Functions
P0.0–P0.7	I/O	I/O port with bit-programmable pins. Configurable to input or push-pull output mode. Pull-up resistors are assignable by software. Pins can be assigned individually as external interrupt inputs with noise filters, interrupt enable/ disable, and interrupt pending control.	1	9–16	INT0–INT4
P1.0–P1.7	I/O	I/O port with bit-programmable pins. Configurable to Schmitt trigger input mode or output mode. Pin circuits are either push-pull or n-channel open-drain type. Pull-up resistors are assignable by software.	3	17–24	—
P2.0–P2.3 P2.4–P2.7	I/O	General-purpose I/O port with bit-programmable pins. Configurable to Schmitt trigger input mode, push-pull output mode, or n-channel open-drain output mode. Pull-up resistors are assignable by software. Lower nibble pins, P2.3–P2.0, can be assigned as external interrupt inputs with noise filters, interrupt enable/disable, and interrupt pending control.	2 3	5–8, 25–28	INT5–INT8 —
P3.0 P3.1	I/O	2-bit I/O port with bit-programmable pins. Configurable to Schmitt trigger input mode, push-pull output mode, or n-channel open-drain output mode. Pull-up resistors are assignable by software. The two port 3 pins have high current drive capability.	4	29 30	T0PWM/ T0CAP/ T1CAP/ REM/T0CK
X_{IN}, X_{OUT}	—	System clock input and output pins	—	2, 3	—
RESET	I	System reset signal input pin with schmitt trigger circuit.	5	31	—
TEST	I	Test signal input pin (for factory use only; must be connected to V_{SS}).	—	4	—
V_{DD}	—	Power supply input pin	—	32	—
V_{SS}	—	Ground pin	—	1	—