SAMSUNG ELECTRONICS

Preliminary Data Sheet
Publication Number 10-88-9408
July 1997 (Rev. 0.0)

KS88C9408

CMOS Microcontroller for Smart Card Applications

OVERVIEW

The KS88C9408 single-chip CMOS micro-controller is designed for low voltage smart card applications and is fabricated using an advanced 0.65-micron CSMOS process. Its fast and reliable 8-bit CPU is based on the proven Zilog Super8® architecture.

The KS88C9408 has 8 Kbytes of EEPROM, 528 bytes of SRAM, 16 Kbytes of program ROM, a 16-bit random number generator, an 8-bit basic timer, a power-on reset circuit, asynchronous serial I/O interface and numerous security options.

The time required to complete an EEPROM erase/write operation is a fast 1.5 ms each (typical).

The serial I/O module supports fast data transfer rates of 9.6, 19.2, and 38.4 Kbps.

For added data security and for easier programming, EEPROM erase/write and serial I/O subroutines are integrated in the KS88C9408 ROM.

The KS88C9408 either meets or exceeds all relevant ISO standards.

FEATURES

CPU

- SAM87 8-bit CPU core
- 78 instructions, including multiply and divide
- STOP and IDLE instruction is added to reduce power consumption

Memory Allocation

- 15 Kbytes of ROM for the application program and 1 Kbytes for the built-in subroutine(kernel)
- 8 Kbytes Data Memory (EEPROM)
- 256 bytes Static RAM
- 272 bytes for general-purpose register file

EEPROM Write Operations

- Programmable EEPROM erase/write time
- Byte-wise to Page-wise (32 bytes) EEPROM erase/write operations are supported
- 1.5ms fast erase/write time each (typical)
- More than 100,000 erase/write cycles
- Greater than 10 years data retention

Data Security

- Secure (non-visible) ROM coding
- 32-byte security PROM, hardware protected
- Unique serial number for each chip
- Reset operation are selective if abnormal voltage or frequency is detected.

Serial I/O Interface

- Asynchronous half-duplex character transmission serial Interface (conforms to ISO standards 7816-3)
- Data transfer rates of 9.6, 19.2, or 38.4 Kbps at 3.57-MHz external clock
- Software (kernel) control

Random Number Generator

- One 16-bit random number generator with internal ring oscillator
- Start and Stop control

Basic Timer

- One 8-bit Basic timer for internal reset operation and watchdog timer functions

Reset Function

- Power-on reset and External reset circuits

Operating Characteristics

- Single power supply: 2.7–5.5 V
- Operating frequency range: 1–5 MHz
- Operating temperature range: – 25°C to + 70°C

Package

- 8-pin COB (conforms to ISO standard 7816)

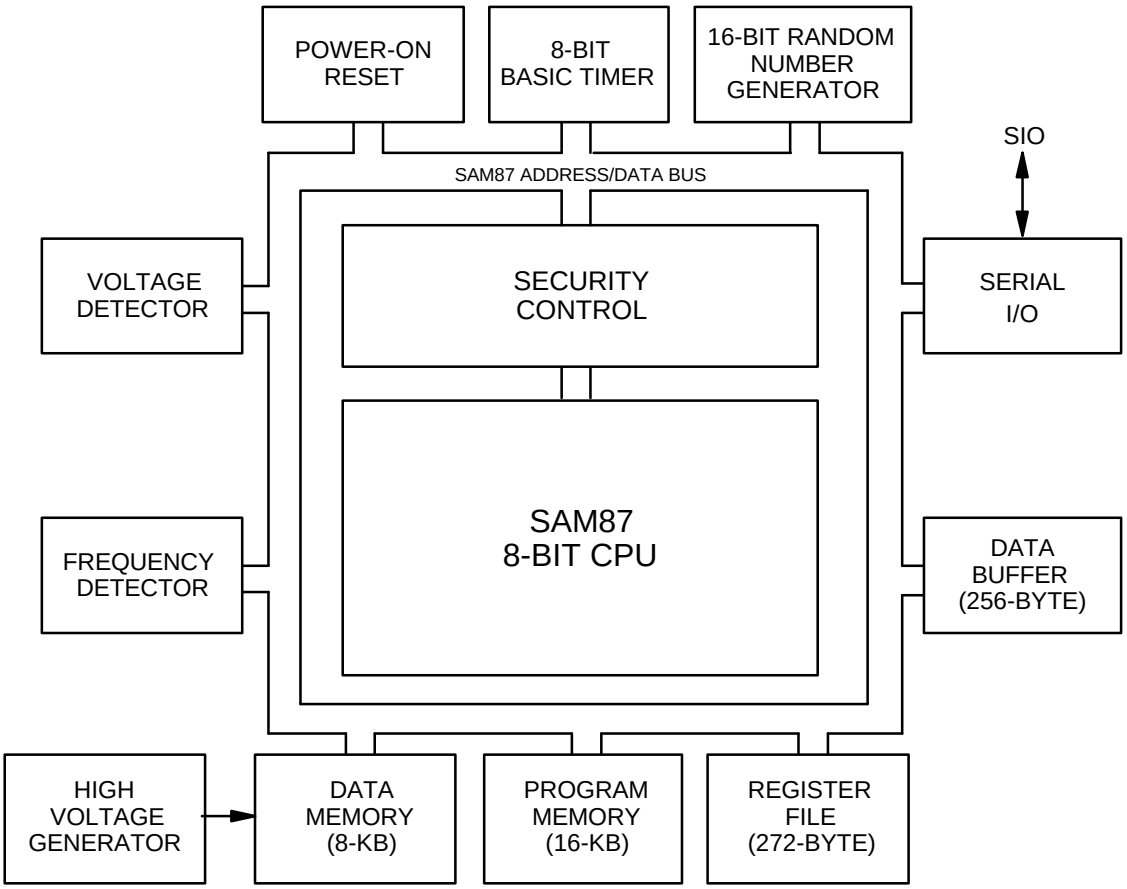


Figure 1. KS88C9408 Block Diagram

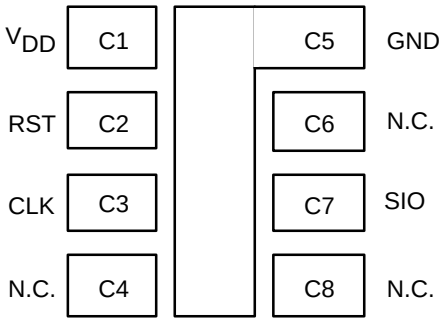


Figure 2. Pin Assignments

Table 1. KS88C9408 Pin Descriptions

Pin Number	Pin Name	Function Description	Pin Type
C1	V_{DD}	Power input	—
C2	RST	System reset input	Input
C3	CLK	External clock input	Input
C4	NC	No connection	—
C5	GND	Ground	—
C6	NC	No connection	—
C7	SIO	Serial data input and output pin: External pull-up resistor should be connected to V_{DD}	Input/output
C8	NC	No connection	—

FUNCTION OVERVIEW

CPU

The KS88C9408 8-bit CPU (SAM87) architecture is based on a 16-bit address bus and an 8-bit data bus. The internal bus supports memory, register, and stack operations, interrupt handling, clock, and power-down control logic.

Instruction Set

The SAM87 instruction set is designed to support a large register file and consists of 78 instructions, including multiply and divide.

The instruction set also supports decimal adjustment of binary-coded decimal (BCD) numbers, 16-bit word increment and decrement, and bit addressing, as well as rotate and shift operations.

Addressing Modes

The KS88C9408 register architecture uses an efficient method of working register addressing to take full advantage of shorter instruction formats and to reduce execution times. An instruction can address a single 8-bit register or a 16-bit register pair. There are seven explicit addressing modes (not all addressing modes are available for each instruction):

— Register (R)
— Indirect Register (IR)
— Indexed (X)
— Direct Address (DA)
— Indirect Address (IA)
— Relative Address (RA)
— Immediate (IM)

Interrupts

The SAM87 interrupt structure has three components: level, source, and vector. The KS88C9408 uses one interrupt source and one vector (one vector for one source).

Interrupt source corresponds to one level. One interrupt level can be selected for the special fast interrupt processing feature.

System Clock Control

Clock frequency input from an external device may range from 1–5 MHz. The typical input clock frequency is 3.57 MHz. To obtain this frequency, you must select a non-divided CPU clock using the appropriate system clock control register settings.

Please note that the data transfer rates which are supported by the KS88C9408 serial I/O interface (9.6, 19.2, and 38.4 Kbps) are based on the typical 3.57-MHz clock frequency value.

Basic Timer

The KS88C9408 8-bit basic timer has two functions:

— To provide an automatic reset mechanism (watchdog timer function) in the event of a system malfunction. If the 8-bit counter overflows, a system reset is initiated.
— To determine the length of the oscillation stabilization interval following a reset. When an external reset or interrupt occurs in Stop mode, or when a power-on reset occurs, the CPU waits for the reset release interval to elapse before resuming normal operation.

Reset Operations

When the power supplied to the KS88C9408 through the V_{DD} pin reaches a minimum level, an internal reset operation is initiated. A reset can also be triggered by the rising edge of the external reset signal through the RST pin.

The minimum Low level width of the external reset signal is 5 µs. An overflow of the basic timer counter signals the CPU that the programmed oscillation stabilization interval has elapsed, and that it can enter normal operating mode.

The KS88C9408 has an integrated power-on reset circuit. When RESET is released and returns to High level, the CPU fetches the instruction stored at program memory location 100H (the reset vector address), and then jumps to the start address of the application program (400H).

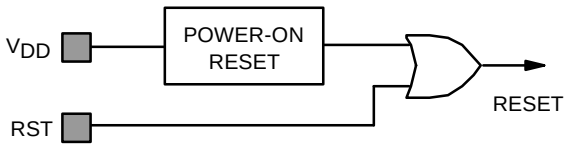


Figure 3. Reset Logic

Power-Down Modes

Idle mode is invoked by the instruction, IDLE. In Idle mode, the CPU "sleeps" while select peripherals remain active. The internal clock signal is gated off to the CPU, but is supplied to the interrupt structure, basic timer, serial I/O block, or the random number generator.

Stop mode is invoked by the instruction, STOP. In Stop mode, the CPU and all peripheral functions "go to sleep", and all on-chip operations come to a halt.

The Idle mode or Stop mode power-down condition may be released in two ways:

— By an interrupt (After the interrupt is serviced, the instruction immediately following the one that initiated Idle mode is executed).

— By a reset operation (When RESET is released and returns to High level, the CPU fetches the instruction stored at memory location 0100H and executes the application program).

Program Memory (ROM)

The KS88C9408 has a 16-Kbyte, read-only program memory (ROM). The upper 15-Kbyte of the ROM is reserved for a user application program. The lower 1-Kbyte is reserved for a built-in subroutine (kernel).

Data Memory (EEPROM)

The KS88C9408 has an 8-Kbyte electrically erasable programmable read-only memory (EEPROM). The EEPROM area is organized as a 32-byte page.

A single EEPROM load operation consists of an erase and a write operation of from 1 to 32 bytes:

— In the erase operation, the selected data bytes within the address range are set to logic one.

— In the write operation, individual bits within the byte range are selectively changed from logic one to logic zero.

A built-in subroutine supports programming in data memory. The lower 32 bytes of the EEPROM (8000H–801FH) is a read-only information area. You can use this area to store manufacturing data about the chip or the smart card.

Data Buffer (SRAM)

The KS88C9408 has a 256-byte area (in SRAM) which serves as a buffer for serial data that is being transmitted or received through the SIO pin.

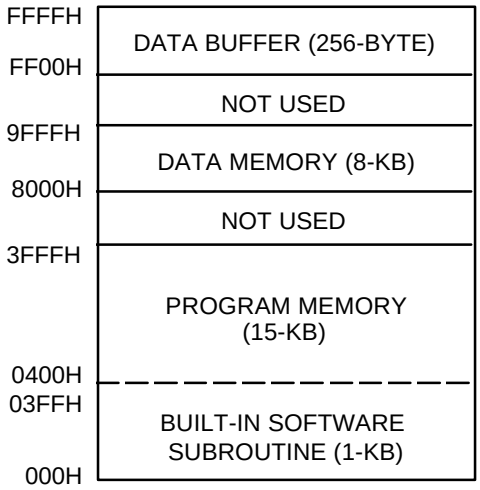


Figure 4. Memory Map

Register File (SRAM)

The KS88C9408 has a 272-byte area in SRAM for general-purpose registers and working registers, and another 25 bytes for mapped system control registers.

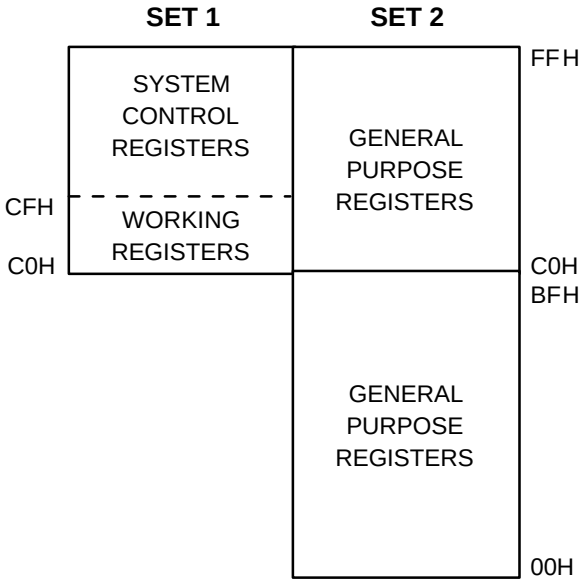


Figure 5. Register File Map

Serial I/O Interface

The KS88C9408 supports asynchronous half-duplex serial I/O in conformance with the ISO 7816-3 standard. A 10-bit frame (one start bit, eight data bits, LSB first and one even parity bit) is used for serial transmit and receive operations. Data transfer rates of 9.6, 19.2, and 36.4 Kbps (at 3.57 MHz) are supported.

Serial data transfer rates are fully compliant with ISO standards:

— Using the built-in software subroutine (kernel)

Security Features

The KS88C9408 voltage and frequency detectors perform the following functions:

— Detect abnormal V_{DD} levels

— Detect abnormal clock frequencies

Using security control register setting, programmers can enable or disable the chip reset function, as required by the application.

Random Number generator

A 16-bit random number generator issues security keys which are used for authentication procedures in smart card applications.

ELECTRICAL DATA

Table 2. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	—	–0.3 to + 7.0	V
Input voltage	V_{IN}	—	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	—	–0.3 to V_{DD} + 0.3	V
Operating temperature	T_A	—	–25 to + 70	°C
Storage temperature	T_{STG}	—	–65 to + 150	°C
Electrostatic discharge	V_{ESD}	—	5000	V

Table 3. D.C. Electrical Characteristics

(T_A = –25°C to + 70°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	2.7	—	5.5	V
Operating current	I_{DD1}	f_{CLK} = 3.57 MHz, 5V	—	3.5	10	mA
		f_{CLK} = 3.57 MHz, 3V	—	1.0	5	
Idle current (with clock)	I_{DD2}	f_{CLK} = 3.57 MHz, 5V	—	1.0	2	
Stop current (without clock)	I_{DD3}	f_{CLK} = GND, 3V	—	—	10	µA
High level input voltage	V_{IH1}	SIO	0.7 V_{DD}	—	V_{DD}	V
	V_{IH2}	RST	0.8 V_{DD}			
	V_{IH3}	CLK	0.7 V_{DD}			
High level input current	I_{IH1}	SIO	–300	—	+ 20	µA
	I_{IH2}	RST	–20	—	+ 150	
	I_{IH3}	CLK	–20	—	+ 100	
Low level input voltage	V_{IL1}	SIO	0	—	0.2 V_{DD}	V
	V_{IL2}	RST			0.15 V_{DD}	
	V_{IL3}	CLK			0.12 V_{DD}	
Low level input current	I_{IL1}	SIO	–1000	—	+ 20	µA
	I_{IL2}	RST	–200	—	+ 20	
	I_{IL3}	CLK	–100	—	+ 20	
High level output voltage	V_{OH}	SIO, I_{OH} = –20 µA	0.7 V_{DD}	—	V_{DD}	V
Low level output voltage	V_{OL}	SIO, I_{OL} = 500 µA	0	—	0.15 V_{DD}	
Low-voltage detection voltage(note)	V_{LVD}	f_{CLK} = 3.57 MHz	—	2.0	—	V
High-voltage detection voltage(note)	V_{HVD}	f_{CLK} = 3.57 MHz	—	7.0	—	V

NOTE: Data for these parameters are for product verification purposes only.

Table 4. A.C. Electrical Characteristics

(T_A = –25°C to + 70°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low-frequency detection frequency (1)	f_{LFD}	V_{DD} = 5 V	200	500	800	kHz
High-frequency detection frequency (1)	f_{HFD}	V_{DD} = 5 V	7	10	12	MHz
External clock frequency	f_{CPU}	CPU clock	1	3.57	5	MHz
External clock duty (1)	t_{CW}	Clock width	45	50	55	%
RST Low level width (1)	t_{RSL}	—	5	—	—	µs
EEPROM erase time	t_E	—	—	1.5	—	ms
EEPROM write time	t_W	—	—	1.5	—	ms
EEPROM data retention time (1)	t_S	—	10	—	—	Years
EEPROM endurance (erase/write cycles) (1)	$n_{E/W}$	—	100,000	—	—	Cycles
Rise time, fall time (1)	t_R, t_F	SIO C_{IN} = 30 pF, C_{OUT} = 30 pF	—	—	1	µs
		RST C_{IN} = 30 pF, C_{OUT} = 30 pF			1	
		CLK (2) C_{IN} = 30 pF, C_{OUT} = 30 pF			0.5 × 9%	

NOTES:
1. Data for these parameters are for product verification purposes only.
2. The rise time, fall time data for CLK assumes 9% of the period with a maximum time of 0.5 µs. This condition is represented by the formula, $0.09 \times 1 / f_{CLK}$.

SIO TIMING DIAGRAM

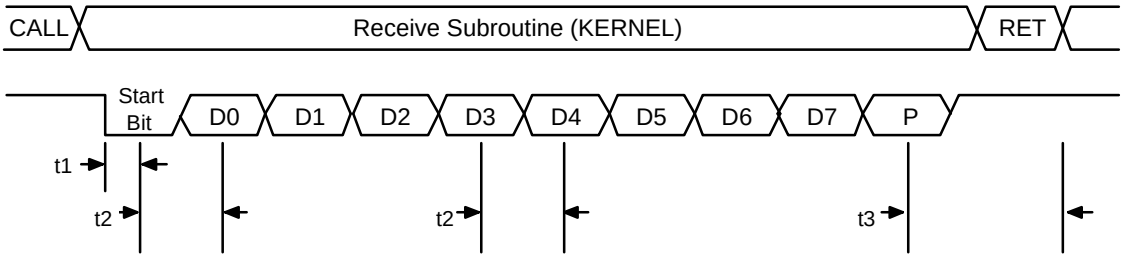


Figure 6. Data Receive

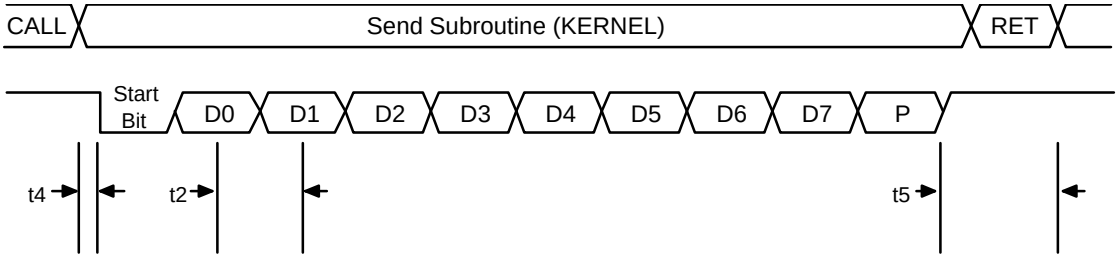


Figure 7. Data Receive

Table 5. Number of Clock for Sampling at 3.57 MHz

bps	t1	t2	t3	t4	t5
9600	178–196	372	305	115	17
19200	86–104	186	161	115	17
38400	38–56	92	127	115	17

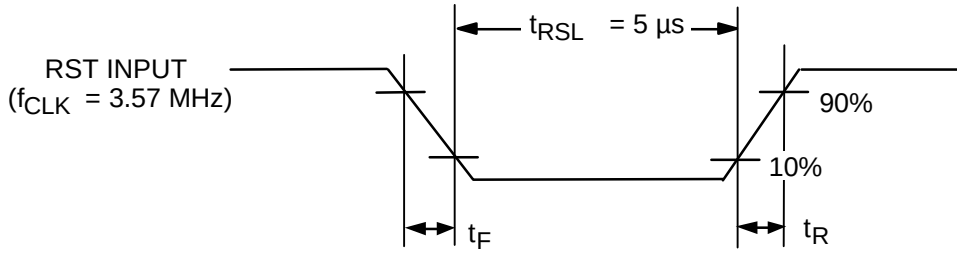


Figure 8. RST Input Wave Form

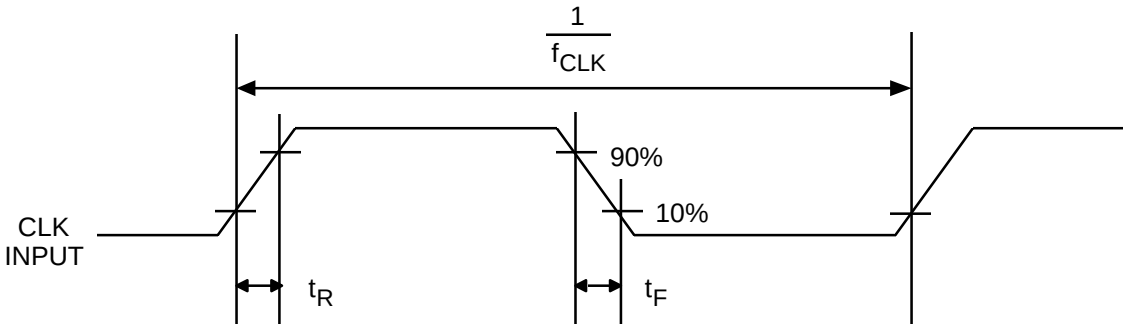


Figure 9. CLK Input Wave Form

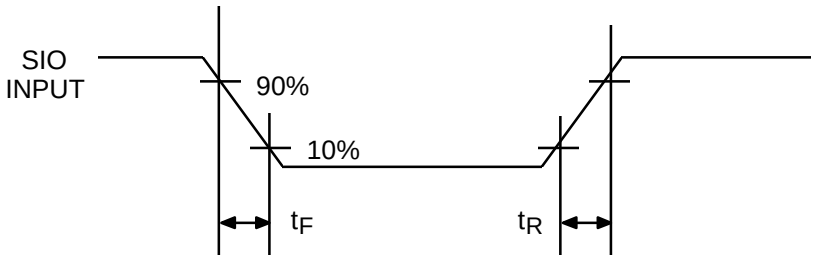
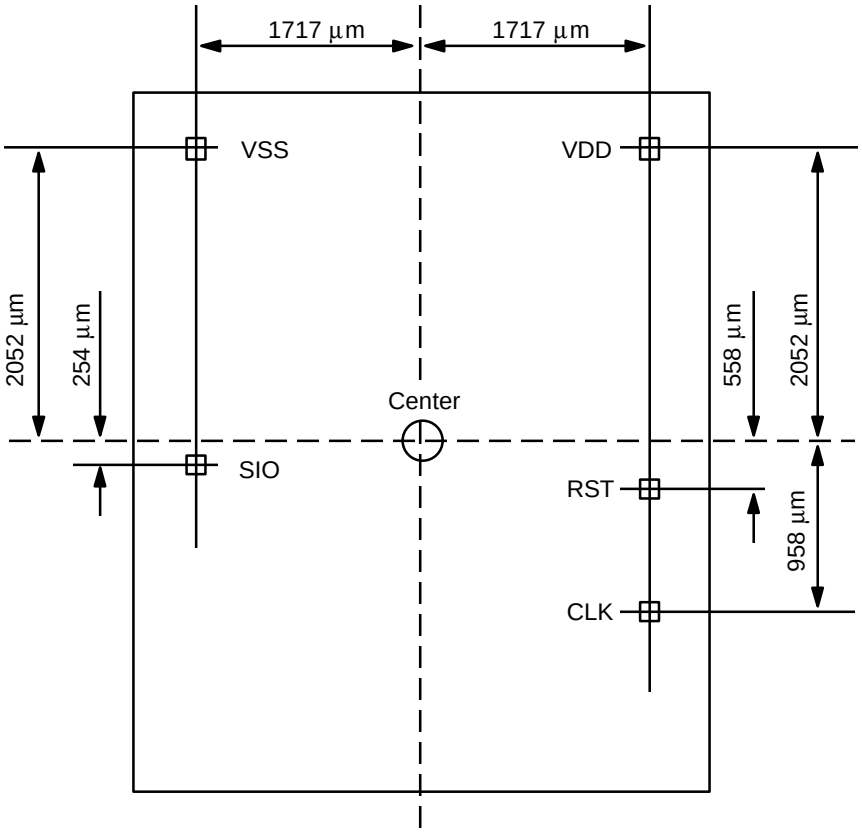


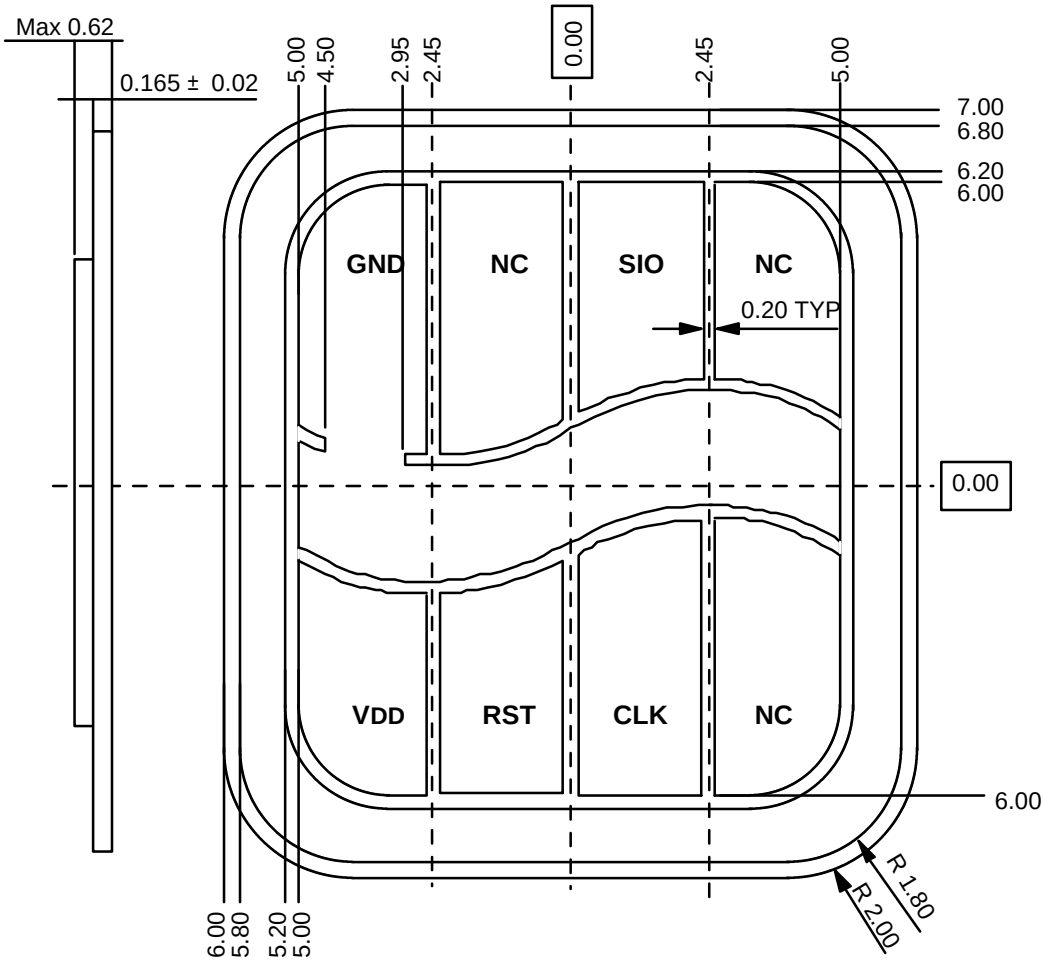
Figure 10. SIO Input Wave Form

MECHANICAL DATA



Wafe Size : 6 inches
Chip Size : 3850 x 4590 µm (not including scribe lane)
Scribe Line : 130 µm
Pad Size : 90 x 90 μm^2

Figure 11. Chip Dimensions



NOTES:

1. Dimensions are in millimeters.
2. The 8-pad COB package dimensions shown above are only approximate. Actual dimensions are adapted to customer specifications.

Figure 12. Package Dimensions