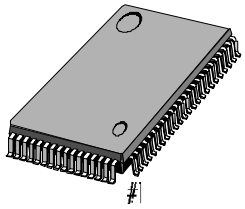
NTRODUCTION

The KS9241B is a CD-ROM Decoder LSl, enabled to perform the real-time Error Correction in CD-ROM Drives or CD-I players. It is suitable for the CD-ROM Drive.

80–QFP–1420C



FEATURES

- Compatible with CD-ROM (Model1) and CD-I (Mode 2)
- Real-time error correction and detection
- Erasure correction by means of C2 pointer
- Connection to external SRAM up to 64K bytes as buffer memory
- Host interface
- CMOS single power supply (+5 V)
- Micom interface

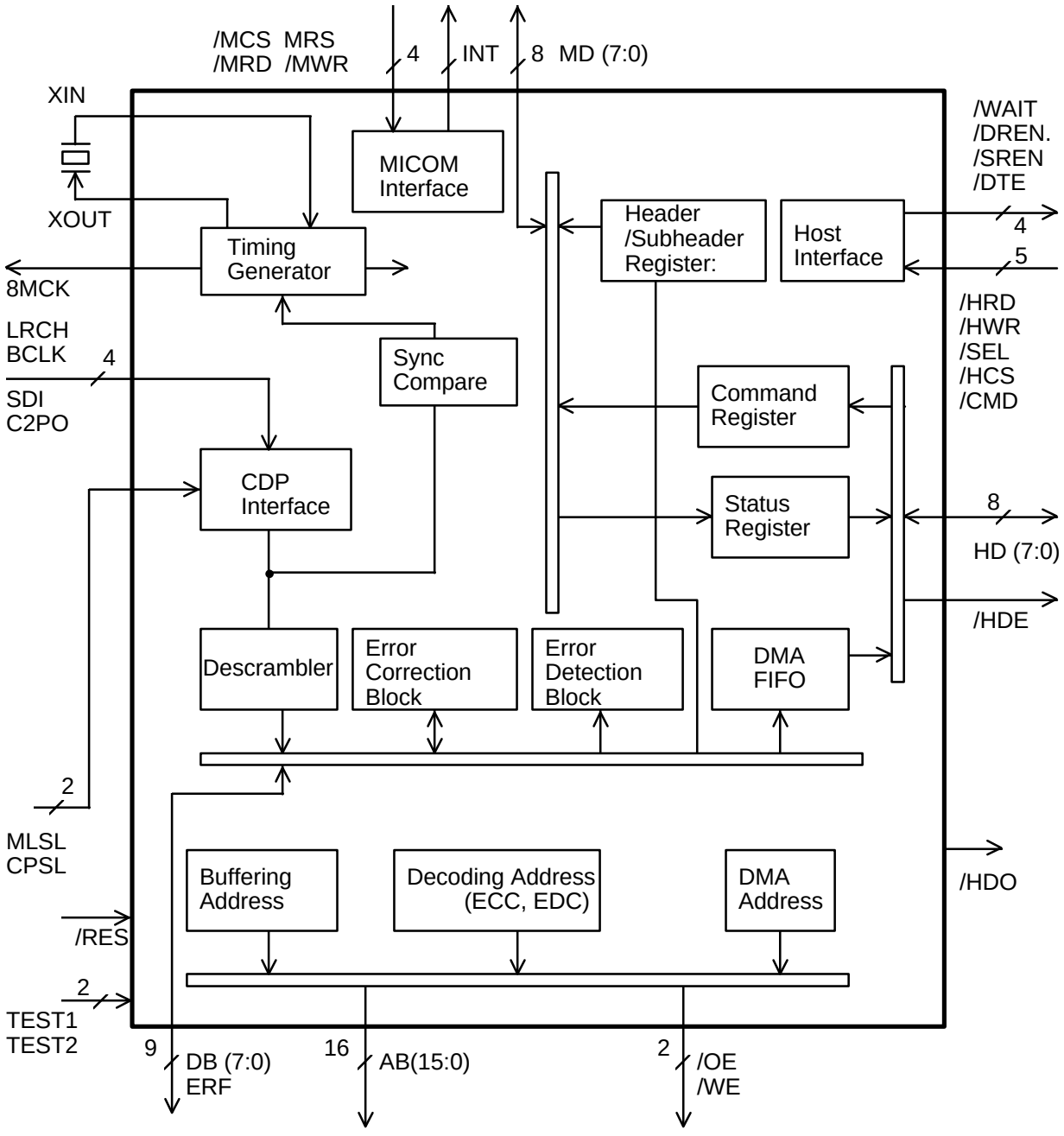
APPLICATIONS

- CD-ROM Drive
- Video-CD
- CD-I
- CD-ROM Game
- Karaoke

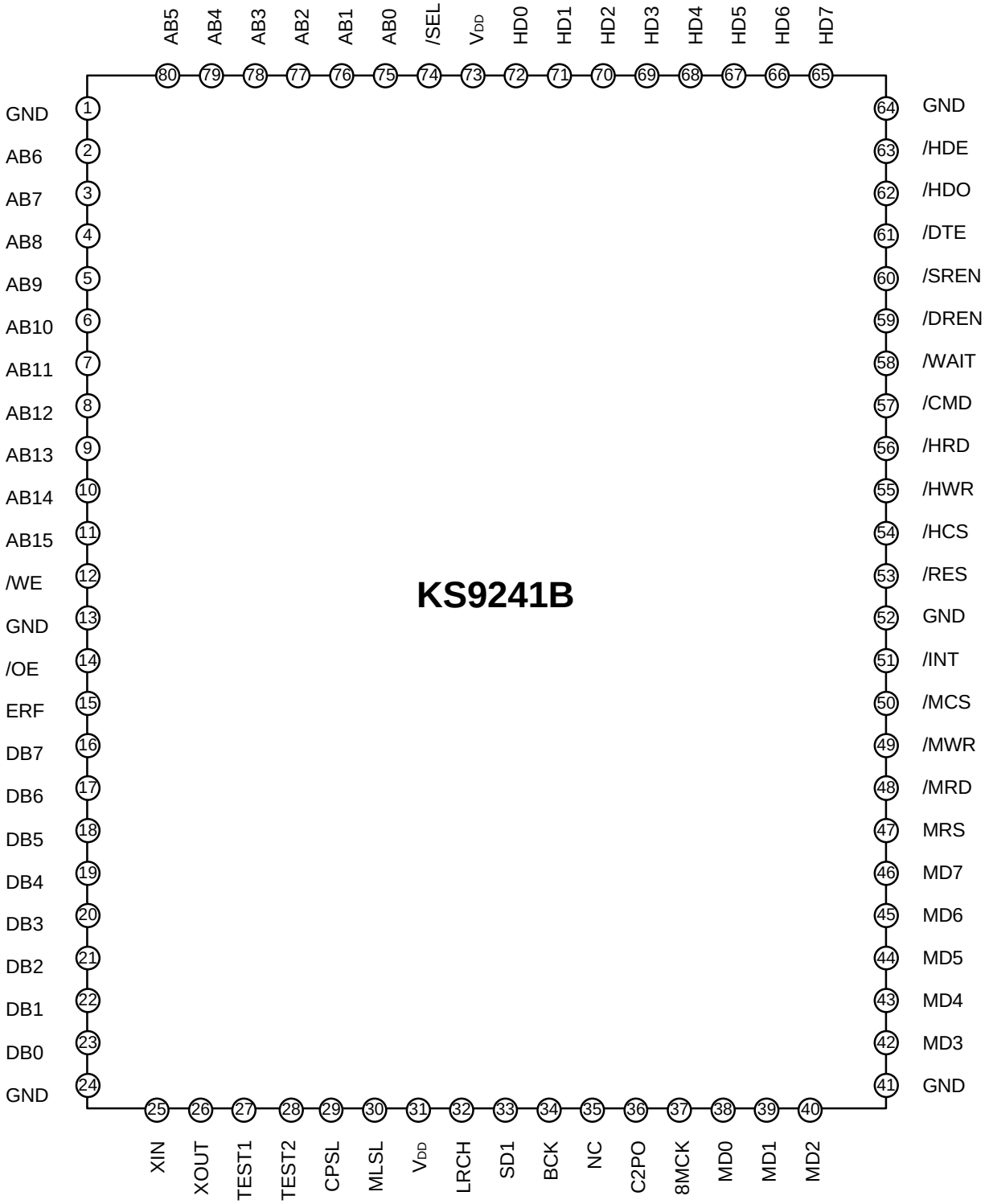
ORDERING INFORMATION

Device	Package	Operating Temperature
KS9241B	80–QFP–1420C	–25°C to +70°C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	GND	–	Ground
2 – 11	AB6-AB15	O	RAM Address output
12	/WE	O	Write Enable output to RAM
13	GND	–	Ground
14	/OE	O	Output Enable output to RAM
15	ERF	I/O	Erasure Flag I/O pin
16–23	DB7–DB0	I/O	Data I/O pin
24	GND	–	Ground
25	XIN	I	Input pin of correction oscillating circuit (f = 16.9344MHz)
26	XOUT	O	Output pin of correction oscillating circuit
27	TEST1	I	Input pin for test. It is “L” during normal operation and “H” during test
28	TEST2	I	Input pin for test. It is “L” during normal operation and “H” during test
29	CPSL	I	Phase selection input pin of serial data input clock
30	MLSL	I	Order selection input pin of serial data input
31	V_{DD}	–	+5 V Supply voltage
32	LRCH	I	Signal input pin of 44kHz to distinguish Left or Right channel of CD audio data
33	SDI	I	Serial data input pin
34	BCLK	I	Clock pin for serial data input
35	NC	–	No Connection
36	C2PO	I	C2 Erasure Flag input pin
37	8MCK	–	Divide 2 output pin of XIN
38-40	MD0-MD2	I/O	Micom data I/O pin
41	GND	–	Ground
42-46	MD3-MD7	I/O	Micom data I/O pin
47	MRS	I	Register selection input pin If “H”, it selects the register and if “L”, it selects the address decoder
48	/MRD	I	Control signal input pin which Micom reading data
49	/MWR	I	Control signal input pin which Micom writing data
50	/MCS	I	Input pin of chip select signal from Micom
51	/INT	O	Ouput pin of interrupt signal to Micom
52	GND	–	Ground

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
53	/RES	I	Chip reset input pin
54	/HCS	I	Input pin of chip select signal from Host
55	/HWR	I	Input pin of control signal which writing data from Host
56	/HRD	I	Input pin of control signal which Host reading data
57	/CMD	I	If Host is set to “L”, it selects command (status) and if “H”, it selects data.
58	/WAIT	O	If /SEL is “H” while Host reading data, it functions as wait signal if /SELis “L” it functions as data requiring signal
59	/DREN	O	Output pin of data read enable signal
60	/SREN	O	Output pin of status read enable signal
61	/DTE	O	Output pin of data transmission completion signal into Host
62	/HDO	O	This pin is “L” while RAM access is performed
63	/HDE	O	Erasure Flag output pin into Host
64	GND	–	Ground
65–72	HD7–HD0	I/O	Host data I/O pin
73	VDD	–	+5V Supply voltage
74	/SEL	I	Transmission mode selection pin into Host
75–80	AB0–AB5	O	RAM Address output

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 ~ + 7.0	V
Input Voltage	V_{IN}	–0.3 ~ + 7.0	V
Output Voltage	V_{OUT}	–0.3 ~ + 7.0	V
Operating Temperature	T_{OPR}	–25 ~ + 75	°C
Storage Temperature	T_{STG}	–55 ~ + 125	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.5	–	5.5	V
Input Voltage	V_{IN}	0	–	V_{DD}	V
Operating Temperature	T_{OPR}	–25	–	70	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 ~ 5.5V, GND = 0V, Ta = 25°C unless otherwise specified)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Low Voltage	$V_{IL(1)}$	–	–	–	$0.2V_{DD}$	V
Input High Voltage	$V_{IH(1)}$	–	$0.7V_{DD}$	–	–	V
Output High Voltage	$V_{OH(2)}$	I_{OH} = –3mA	$0.7V_{DD}$	–	–	V
Output Low Voltage	$V_{OL(2)}$	I_{OL}= 3mA	–	–	$0.2V_{DD}$	V
Input Leak Current	I_{IL}	V_I = GND, V_{DD}	–15	–	25	uA

NOTES:

1. All input pins except for X_{IN} pin (including /RES 4 BUS pin)
2. All output pins except for X_{OUT} pin (including BUS pin)

AC Characteristics

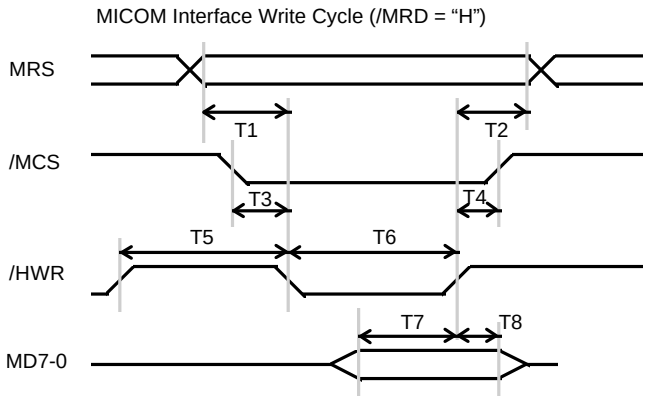


Figure 1.

Name	Description	Min	Typ	Max	Unit
T1	Register select setup to write signal	20	–	–	ns
T2	Register select hold from end of write signal	45	–	–	ns
T3	Chip Select setup to write signal	20	–	–	ns
T4	Chip select hold from end of write signal	35	–	–	ns
T5	Write signal recovery time	60	–	–	ns
T6	Write signal pulse width	60	–	–	ns
T7	Data setup to end of write signal	30	–	–	ns
T8	Data hold from end of write signal	15	–	–	ns

AC Characteristics (Continued)

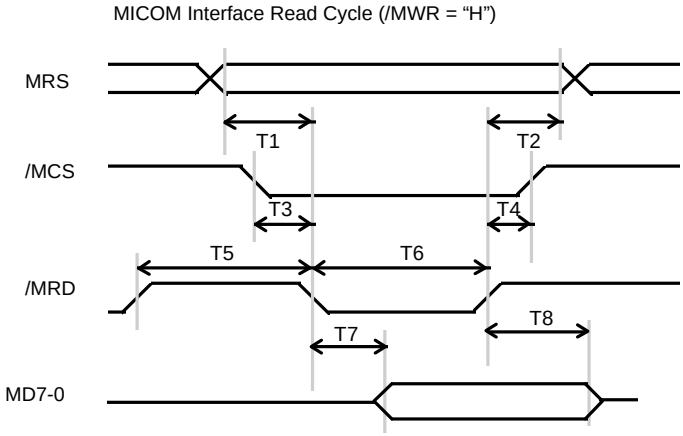


Figure 2.

Name	Description	Min	Typ	Max	Unit
T1	Register select setup to read signal	20	–	–	ns
T2	Register select hold from end of read signal	10	–	–	ns
T3	Chip slect setup to read signal	20	–	–	ns
T4	Chip select hold from end of read signal	10	–	–	ns
T5	Read signal recovery time	60	–	–	ns
T6	read signal pulse width	60	–	–	ns
T7	Data address from read signal	–	–	50	ns
T8	Data hold from end of write signal	5	–	–	ns

AC Characteristics (Continued)

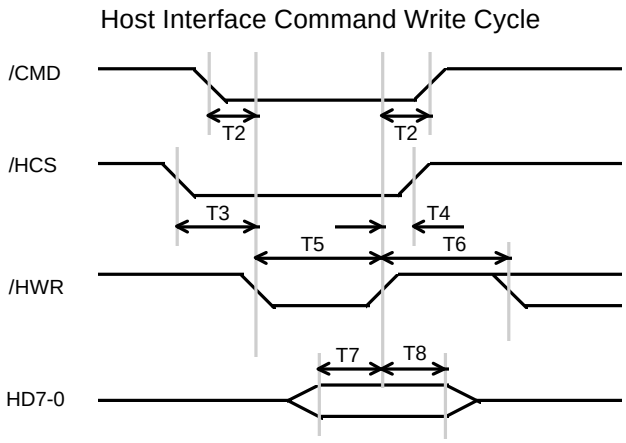


Figure 3.

Name	Description	Min	Typ	Max	Unit
T1	Command select setup to write signal	10	–	–	ns
T2	Command select hold from end of write signal	5	–	–	ns
T3	Chip select setup to write signal	30	–	–	ns
T4	Chip select hold from end write signal	5	–	–	ns
T5	Write signal pulse width	60	–	–	ns
T6	Write signal recovery time	60	–	–	ns
T7	Command data setup to end of write signal	55	–	–	ns
T8	Command data hold from end of write signal	30	–	–	ns

AC Characteristics (Continued)

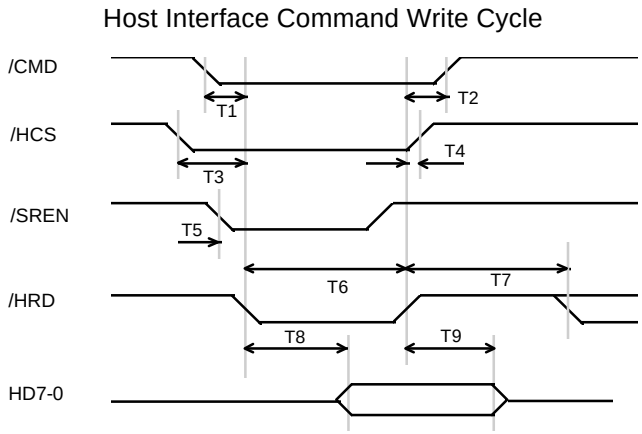


Figure 4.

Name	Deseription	Min	Typ	Max	Unit
T1	Status select setup to read signal	10	–	–	ns
T2	Status select hold from end of read signal	35	–	–	ns
T3	Chip select setup to read signal	30	–	–	ns
T4	Chip select hold from end of read signal	5	–	–	ns
T5	Status read enable to read signal	15	–	–	ns
T6	Read signal pulse width	60	–	–	ns
T7	Read signal recovery time	60	–	–	ns
T8	Status data access from read signal	–	–	60	ns
T9	Status data hold from read signal	0	–	–	ns

AC Characteristics (Continued)

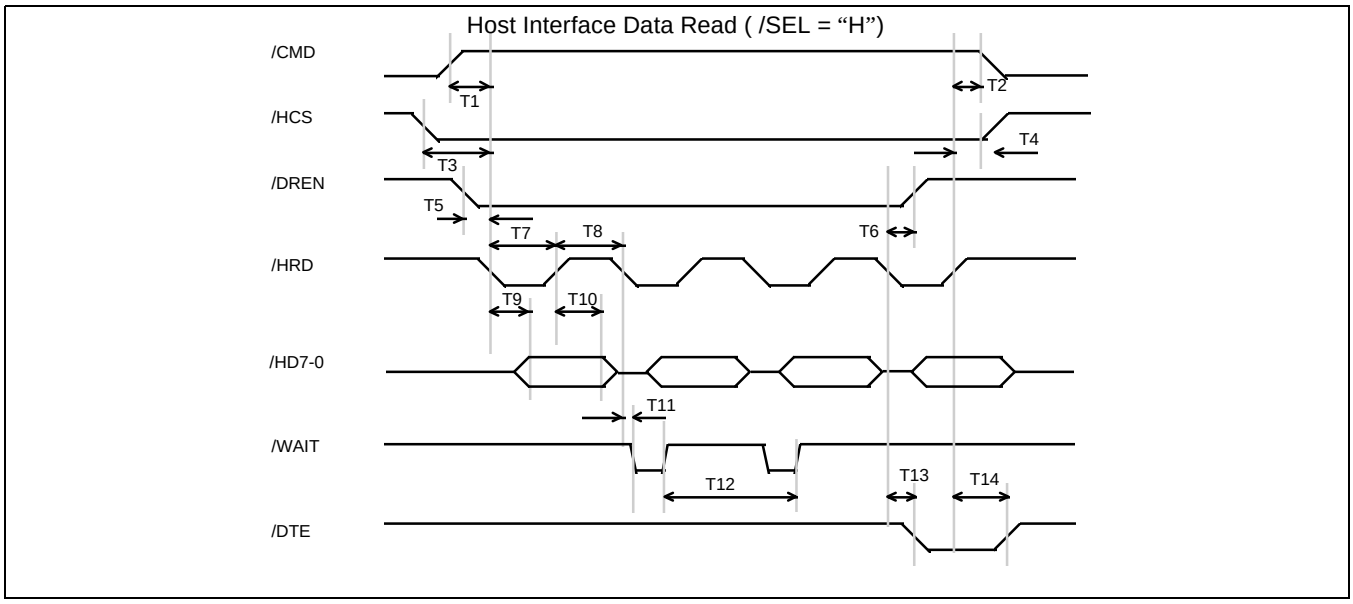


Figure 5.

Name	Description	Min	Typ	Max	Unit
T1	Status select setup to read signal	10	–	–	ns
T2	Status select hold from end of read signal	35	–	–	ns
T3	Chip select setup to read signal	30	–	–	ns
T4	Chip select hold from end of read signal	5	–	–	ns
T5	Data read enable to read signal	15	–	–	ns
T6	Data read enable hold from end of read signal	–	–	70	ns
T7	Read signal pulse width	75	–	–	ns
T8	Read signal recovery time	75	–	–	ns
T9	Data access from read signal	-	–	50	ns
T10	Data hold from end of read signal	0	–	–	ns
T11	Data read wait from read signal	–	–	80	ns
T12	Data read wait recovery time	390	–	–	ns
T13	Data transfer end from read signal	–	–	60	ns
T14	Data transfer end hold from end of read signal	–	–	80	ns

AC Characteristics (Continued)

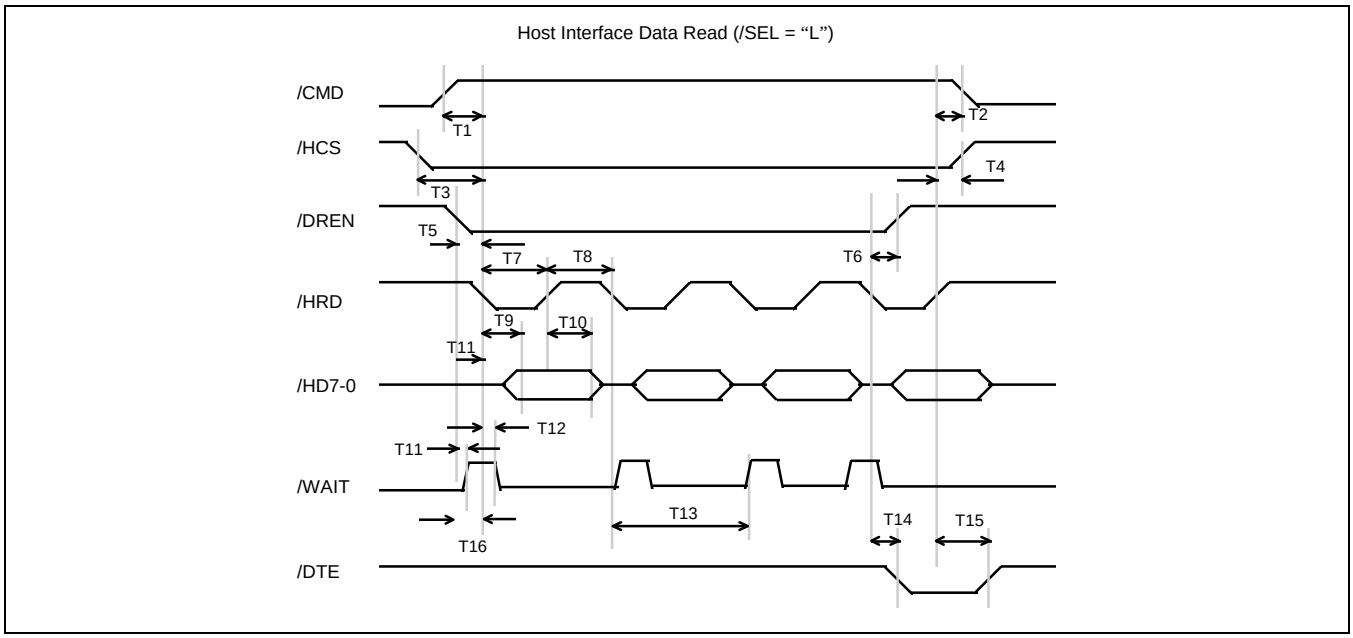


Figure 6.

Name	Description	Min	Typ	Max	Unit
T1	Status select setup to read signal	10	–	–	ns
T2	Status select hold from end of read signal	45	–	–	ns
T3	Chip select setup to read signal	30	–	–	ns
T4	Chip select hold from end of read signal	5	–	–	ns
T5	Data read enable to read signal	15	–	–	ns
T6	Data read enable hold from end of read signal	–	–	70	ns
T7	Read signal pulse width	130	–	–	ns
T8	Data read request from end of read signal	–	–	250	ns
T9	Data access from read signal	–	–	50	ns
T10	Data hold from end of read signal	0	–	–	ns
T11	Data read request from data read enable	–	–	20	ns
T12	Data read request hold from read signal	–	–	70	ns
T13	Data read request recovery time	390	–	–	ns
T14	Data transfer end from read signal	–	–	60	ns
T15	Data transfer end hold from end of read signal	–	–	50	ns
T16	Data read request setup to read signal	15	–	–	ns

AC Characteristics (Continued)

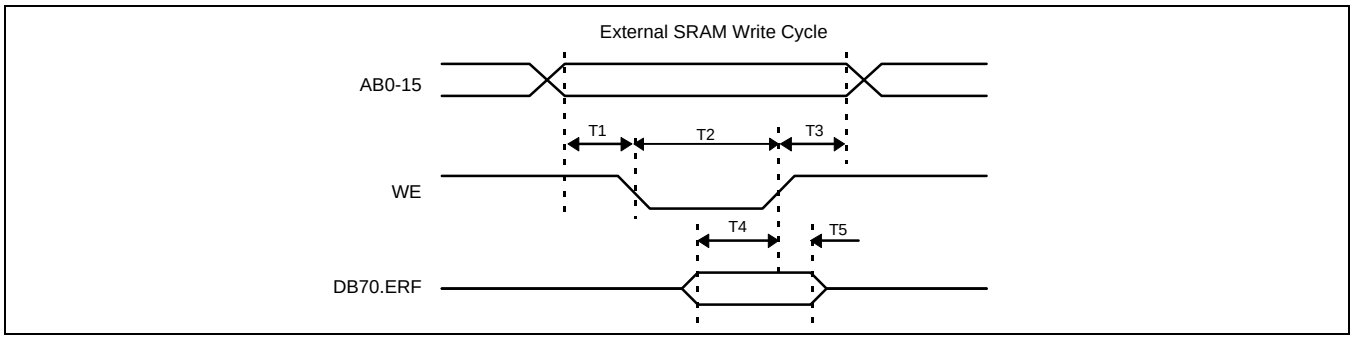


Figure 7.

Name	Description	Min	Typ	Max	Unit
T1	Address setup to Write enable	65	–	–	ns
T2	Write enable width	110	–	–	ns
T3	Address hold from end of write enable	10	–	–	ns
T4	Data address time to end of write enable	75	–	–	ns
T5	Data hold time from end of write enable	5	–	–	ns

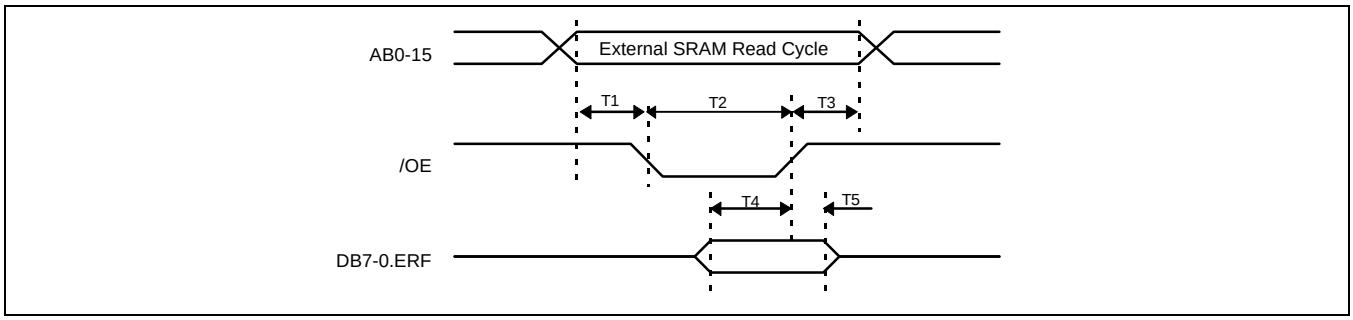


Figure 8.

Name	Description	Min	Typ	Max	Unit
T1	Address setup to read enable	65	–	–	ns
T2	Read enable width	110	–	–	ns
T3	Address hold from end of read enable	10	–	–	ns
T4	Data setup time from read enable	–	–	40	ns
T5	Data hold time from end of read enable	5	–	–	ns

FUNCTION DESCRIPTION

OPERATING MODE

Decoder Mode Selection

Decoder Mode	DECEN	BUFEN	QCOEN + PCOEN
No Decoding	0	"X"	"X"
Monitor Only Mode	1	0	0
Buffering Only Mode	1	1	0
Real-time Correction Mode	1	1	1
Repeat Correction Mode	1	0	1

NOTE: "X" = Don't Care

Monitor Only Mode:

Without buffering, the decoder writes the Error Flags which are compatible to Header and Subheader from the input data, into the Header 1-4 register and the Header register. There is no delay in data input.

Buffering Only Mode:

Decoder performes buffering of input data without error detection and correction. To perform error detection, after power is on, the data over 1 block is required the RAM so this mode is available then.

Real Time Error Correction:

Data buffering, decoding and transferring to Host are performed in parallel by pipeline control. This decoding indicates ECC and CRC (EDC) corrections.

Repeat Error Correction Mode:

If BUFEN is set to 0, the error correction is performed repeatedly for one block without buffering. So high reliability of the data is obtainable.

DATA BUFFERING BLOCK

(a) CDP Interface

For the purpose of the matching with DSP ICs for the conventional CDPs, it is designed to be compatible to 3 types data format in accordance with the assignments of MLSL pin and CPSL pin.
(i) The input signal format when MLSL = “L”, CPSL = “L”.

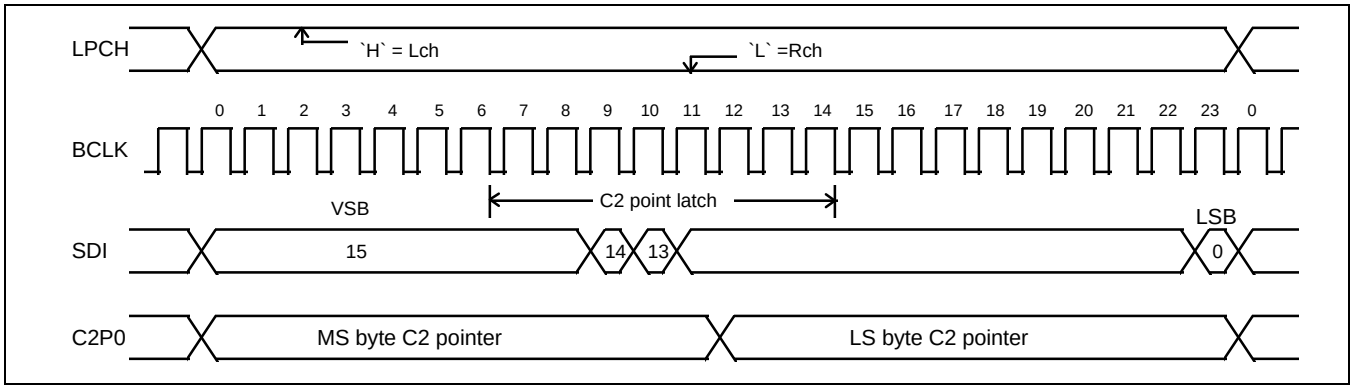


Figure 9.

This mode is available to interface with the DSP ICs or CDPs such as KS5990 from SAMSUNG or CXD2500 from SONY.
(ii) Input signal format in case MLSL = “H”, CPSL = “L”.

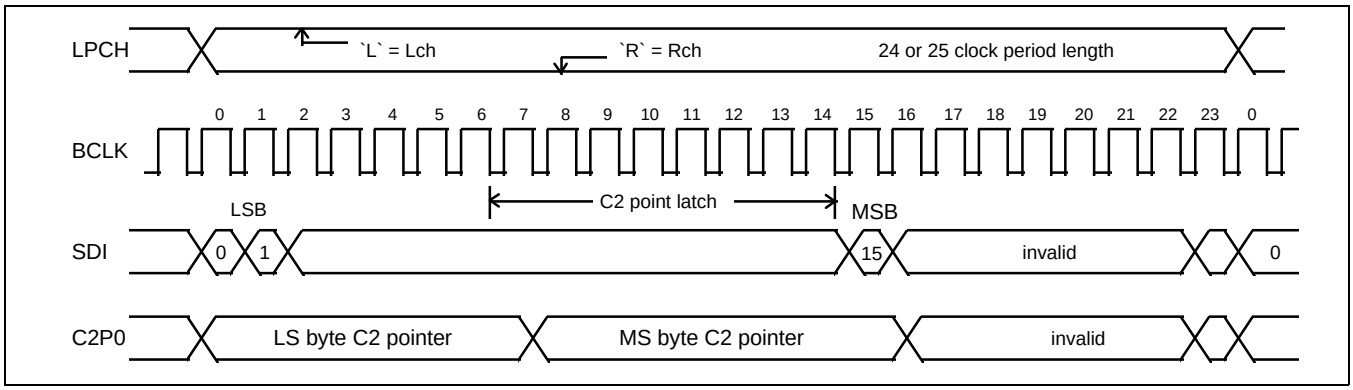


Figure 10.

This mode is available to interface with DSP Ics for CDP such as YM 8315 from YAMAHA or LC7860 SANYO.

(iii) Input signal format in case MLSL = “L”,CPSL = “H”.
This mode is available to interface with DSP ICs for CDP such as TC 9200F from TOSHIBA.

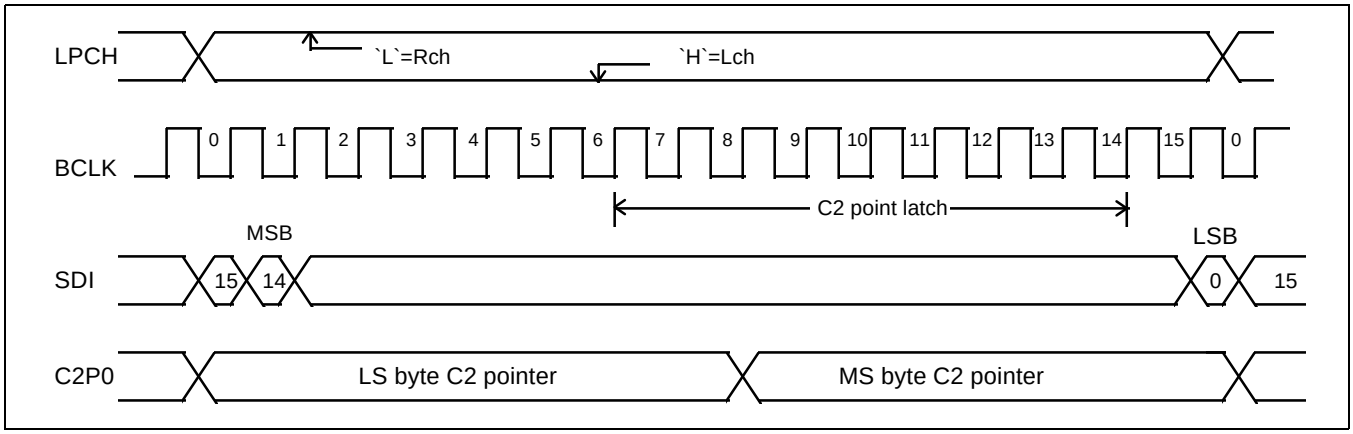


Figure 11.

(iv) This mode is prohibited from use in case MLSL = “H”,CPSL = “H”.

(b) Block Sync

The Sync of KS9241B is controlled by the sync detected from the external input data through sync pattern and the internal sync through built-in circuits. DSYEN bit of CONT2 register makes the sync from the external input enabled and GSYEN bit of CONT2 register makes internal sync enabled. DSYEN and GSYEN are both set to “1” so as to recover the loss of Track Jump and sync pattern quickly which may occur.
But, in repeat correction mode, DSYEN should be set at “0” and GSYEN at “1” because then there is no need for the sync from input data. Both DSYEN and GSYEN are prohibited to be set at “0” at once. Regarding sync state, it can be displayed by NOGSY, NODSY, LNGBLK, STRBLK flag of STATE 1 register.

(I) In case DSYEN = “1”, GSYEN = “1”

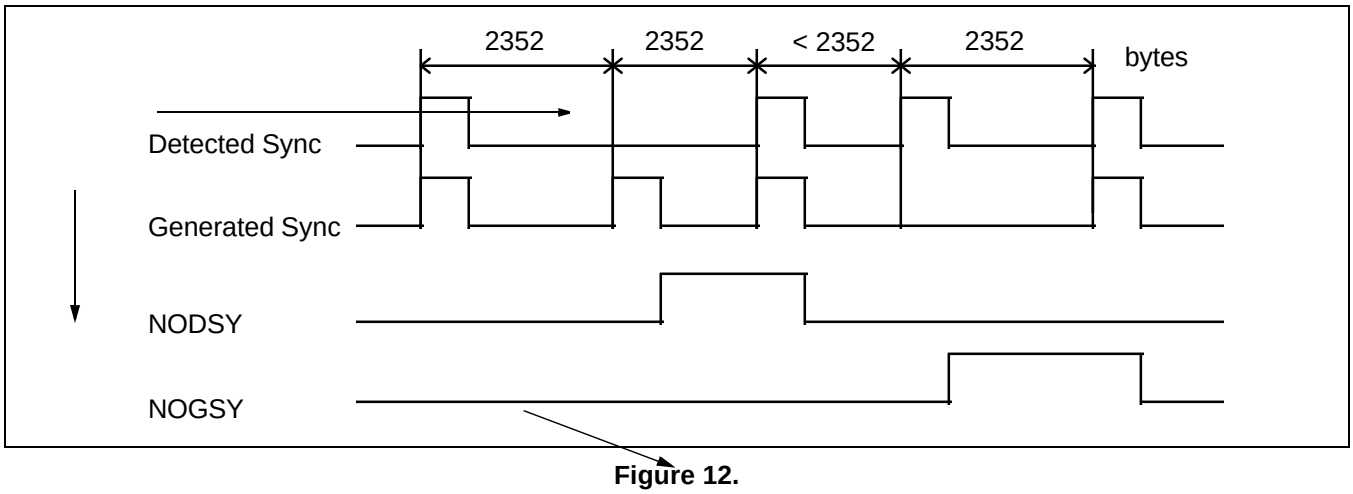


Figure 12.

(ii) In case DSYEN = “1”, GSYEN = “0”

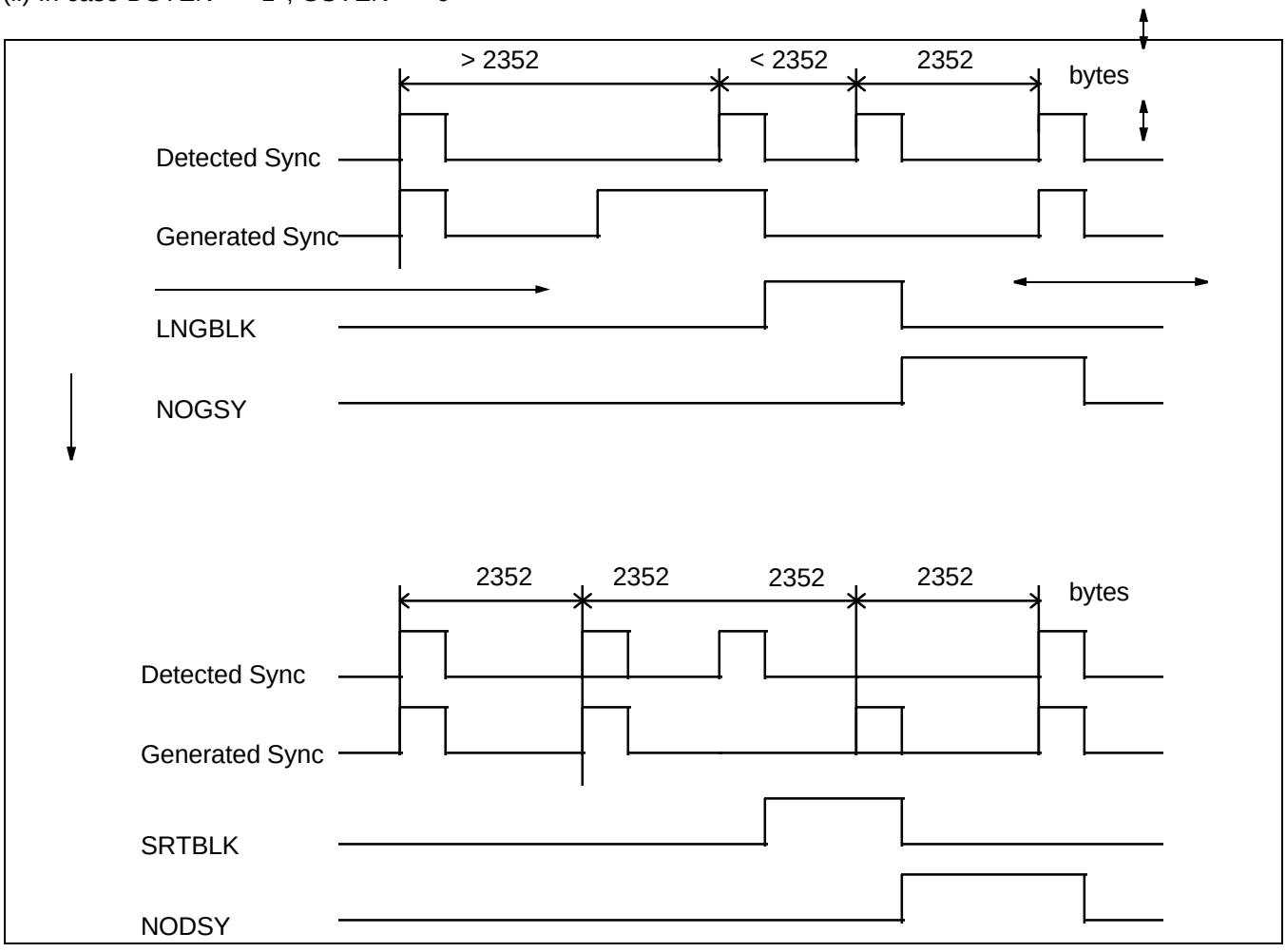


Figure 13.

(c) Descrambling

Since CD ROM Disc is scrambled according to Polynomial $X^{15} + X+1$, it is required to descramble the CD ROM Disc to restore the original data before storing the data. The data is stored by the 9-bit (Data 8-bit and Error Flag 1-bit) at RAM. Scrambling is aimed to reduce the possibility of the same pattern as sync signal, and is performed for 2340 byte of 2352 byte, excluding sync data 12 byte. Besides, both circuits of scrambler and descrambler are same and the configuration is as follows.

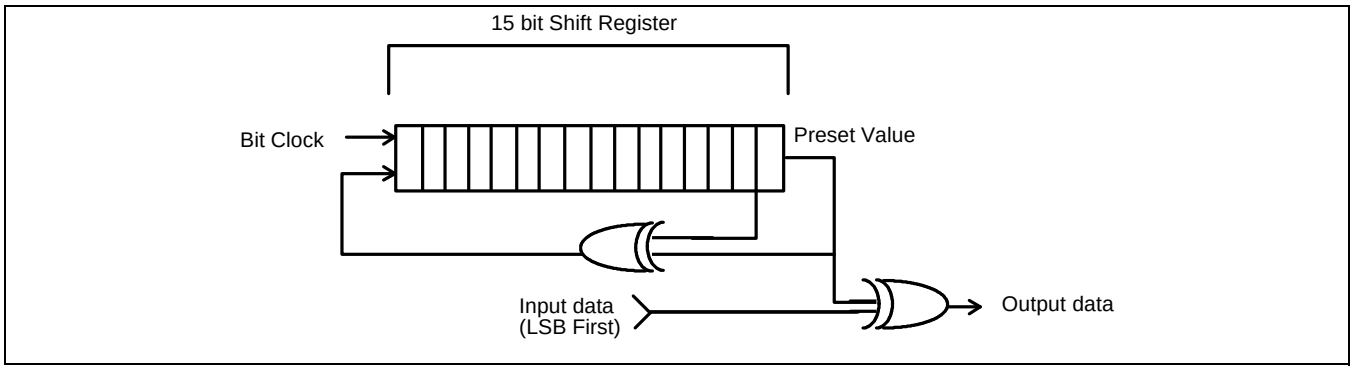


Figure 14.

DECODING BLOCK

The data written in CD-ROM Disc will have the format as follows depending on the mode and form.

	12	4	2048		4	8	276	byte
Mode 1	Sync	Header	User Data		EDC	Space	ECC	
	12	4	8	2048		4	276	byte
Mode 2 Form 1	Sync	Header	Subheader	User Data		EDC	ECC	
	12	4	8	2048		4		byte
Mode 2 Form 1	Sync	Header	Subheader	User Data		EDC or Space		

Error correction is available in case of Form 1 of mode 1 or mode 2, and it is not available in case of form 2 of mode 2. Real time error correction can be started on condition that the data of over 1 block (2352 byte) is buffered at RAM. If the command of correction is given by micom, KS9241B will read data from RAM and generate syndrome after that the value of error location is measured. As a result, error correction will start.
In CD-ROM, RS [26, 24] [45, 43] are used as code and called P code and Q code respectively. The error correction of CD-ROM are performed in terms of 2340 byte excluding sync data. Both the lower byte of 16-bit 1 word data written at even-numbered RAM address and the higher byte written in odd-numbered RAM address, are, LSB plane and MSB plane, decoded by the 1176 byte.

The symbol position of P code and Q code in one plane are as follows

(i) In case of P code

	N_P									
		0	1	2				41	42	
M_P	0	0000	0001	0002	....	....	....	0041	0042	
	1	0043	0044	0045	....	....	....	0084	0085	
	2	0086	0087	0088	....	....		0127	0128	
	3	0129	0130	0131	....	....			0171	
	4	0172	0173	....					0214	
		↓P			Q					
	22	0946	0947	0948			....	0987	0988	
	23	0989	0990	0991		....	....	1030	1031	
					....	....	....			
	24	1032	1033	1034			1072	1073	1074	PARITY-P
	25	1075	1076	1077			1115	1116	1117	
	26	1118	1119	1120	....	1143				PARITY-Q
	27	1144	1145	1146	....	1169				
		0	1	2	.	25				

(ii) In case of Q code

	M_Q										
		0	1	2			40	41	42	PARITY-Q	
N_Q	0	0000	0044	0088	....	....	0642	0686	0730	1118	1144
	1	0043	0087	0131	....	....	0685	0729	0773	1119	1145
	2	0086	0130	0174	....	....	0728	0772	0816	1120	1146
	3	0129	0173	0217	....	....	0771	0815	0859	1121	1147
	4	0172	0216	0260	....	....	0814	0858	0902	1122	1148
		:					:				:
	22	0946	0990	1034	....	....	0470	0514	0558	1140	1166
	23	0989	1033	1077	....	....	0513	0557	0601	1141	1167
	24	1032	1076	0002	....	....	0556	0600	0644	1142	1168
	25	1075	0001	0045	....	....	0599	0643	0687	1143	1169

In terms of P code, the real position of the (MP + 1) th symbol of the (NP + 1)th code at RAM can be measure as follows:

$$(NP + 43 \times MP) \times 2 + a,\ 0 \le N_P \le 42,\quad 0 \le M_P \le 25$$

In terms of Q code, the real position of $(M_Q + 1)$ th symbol of $(N_Q + 1)$ th code at RAM is measured as follows

$$\{(43 \times N_Q + 44 \times M_Q)\bmod 1\,1\,1\,8\} \times 2 + a,\ 0 \le N_Q \le 25,\quad 0 \le M_Q \le 42$$

$$(N_Q + 26 \times M_Q) \times 2 + a,\ 0 \le N_Q \le 25,\quad 43 \le M_Q \le 44$$

Only, a is “0” in case of LSB plane and “1” in case of MSB plane. The detecting correction of KS9241B is completed by the follwing process. Low order byte of Q code → High order byte of Q code → Low order byte of P code → High order byte of P code. The erasure correction order is the same as the above. EDC can be performed after error correction is finished during 1 block correction period.
EDC uses 32-bit CRC in mode 1 from sync to user data and in mode 2 from subheader to user data. EDC code word should be divided by check Polynomial which is as follows.

$$P(X) = (X^{16} + X^{15} + X^2 + 1)(X^{16} + X^2 + X + 1)$$

During EDC period, the header and subheader are stored at the internal register. After EDC, KS9241B are designed to generate decode interrupt to micom. The micom reads the header, subheader, DBSPH, DBSPL registers of the decoded block and various flags which indicates the decoding result.

INTERFACE BLOCK (HOST AND MICOM)

(a) Control signal

– Control signal of host interface: /CMD, /HRD, /HWR
But, available only when /HCS pin is “L”

(i) When / CMD = “L” / HRD = “L” / HWR = “H” (Status read):
The data applied from micom and written in status register is outputted as host data.

(ii) When / CMD = “L” / HRD = “H” / HWR = “L” (Command write):
The data from host is written into command FIFO register.

(iii) When / CMD = “H”, / HRD = “L”, / HWR = “H” (Data read):
Of those read from RAM, the data is sent out through HD0-7 and the erasure frag is out through /HDE

(iv) It is prohibited when / CMD = “H”, / HRD = “H”, / HWR = “L”

– Control signal of micom interface : MRS, / MRD, /MWR.
But, available only when /MCS pin is “L”

(i) MRS = “L”, /MR = “L”, /MWR = “H” (Reads register’s address):
The address values determining internal register are output as micom data. At this time, address is output as the lower 4-bit of micom data and the higher 4-bit is output as “0”.

(ii) MRS = “L”, /MRD = “H”:, /HWR = “L” (Writes register’s address):
The lower 4-bit of micom data is written to address decoder.

(iii) MRS = “H”, / MRD = “L”, /MWR=“H” (Register read):
The contents of register selected by address decoder is outputted into micom data.

(iv) MRS = “H”, /MRD = “H”, /HWR = “L”, (Register write):
The micom data is written into the register selected by address decoder.

(b) Command Transferring

Host is enabled to set /HCS and /CMD at “L” and writes command byte into COMD register. Micom is available to read command byte by setting /MCS at “L” and MRS at “H”. If no command byte is written into COMD register, FF (16 binary number) will be out through micom data bus in case micom starts to read COMD register. Also, on condition that although all data are written at command FIFO of 8 byte, host may write another comman byte, and the later written data can be neglected.
If the command byte is existed at COMD register, command interrupt is generated and /CDINT bit of ISTATE register is set to “0”.
Then, if the CDIEN bit of ICONT register is “1”, /INT pin will be “L”.

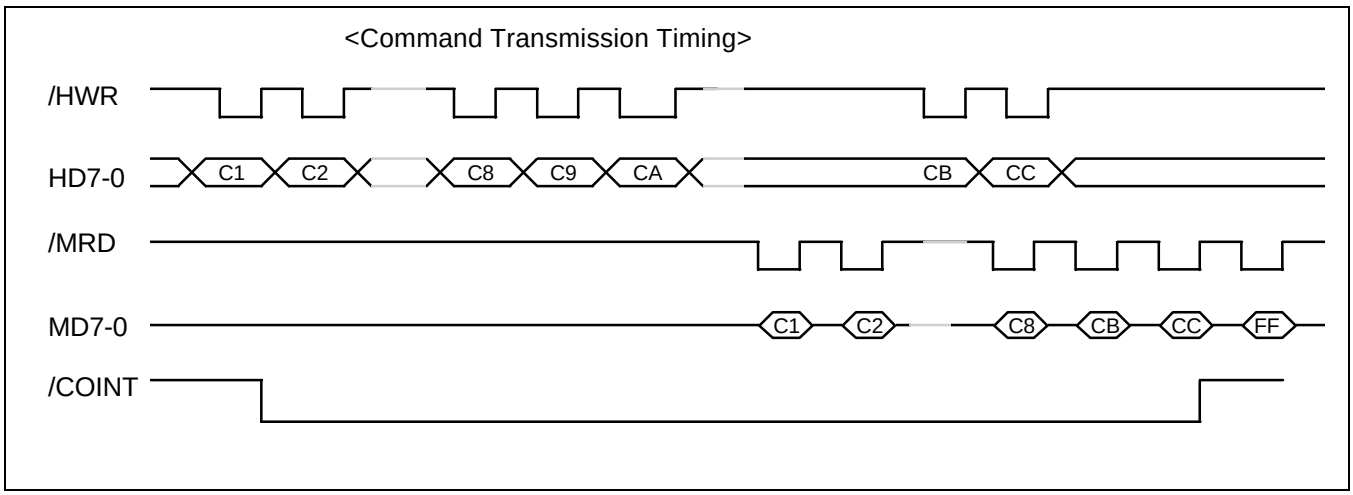


Figure 15.

NOTE: Condition: /HCS = “L”, /CMD = “L”, /HRD = “H”.
/MCS = “L”, MRS = “H”, /MWR = “H”, Address Decoder = “0”

(C) Status Transferring

(i) Normal Operation

On condition that STUEN bit of ICONT register is “1”, micom is enabled to transmit the status byte to the host. Writing the micom data into STATUS register for the status byte transmission is available only when /STUOP bit of ISTATE register is “1”. Meanwhile, if the bit is “0”, the status byte written already will disappear. Normal operation occurs when /STWT bit of ICONT register is “1”. After the writing into STATUS register, /STUOP and /STOPR bits of ISTATE register will be “0” and /SREN pin is “L”. Host is enabled to set /HCS pin at “L” and /CMD pin at “L” and read status byte on condition that /SREN pin is “L”. When host starts to read status byte from STATUS register, /STUOP bit of ISTATE register will be set to “1” and /SREN pin to “H”. After reading is over, /STOPR bit of ISTATE register will be set to “1”. If host reads the data while micom is writing the data into STATUS register, invalid data will be out through host. At this moment, /STUOP bit of ISTATE register will be “0” after writing of micom data. However, /STOPR bit will be “0” and /SREN pin will be “L” only after reading is finished.

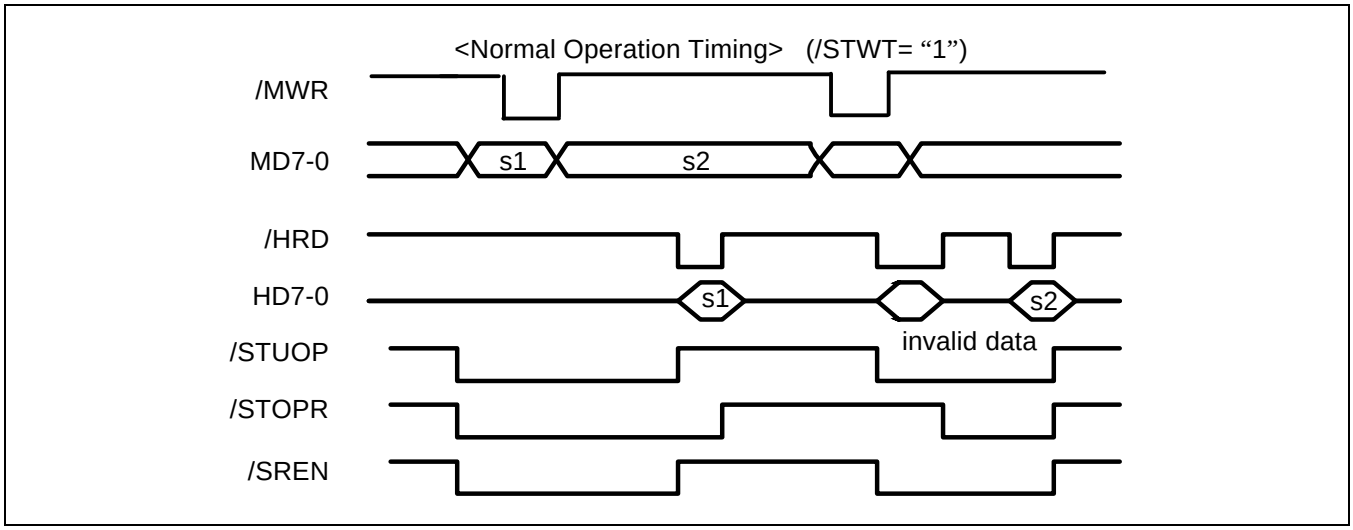


Figure 16.

NOTE: Condition : /HCS = “L”, / CMD = “L”, /HWR = “L”, /MCS = “L”,
MRS = “H”, /MRD = “H”, Address Decoder = “0”

(ii) Wait Operation

The wait operation occurs if /STWT bit of ICONT register is “0”, status byte transmission is performed and RAM data transmission is operational. Then, when the data writing of micom into STATUS register is finished, /STUOP bit of ISTATE register gets to “0”, but /STOPR bit will be “0” and /SREN pin will be “L”, even after RAM data transmission is finished. The rest of this operation is the same as normal operation.

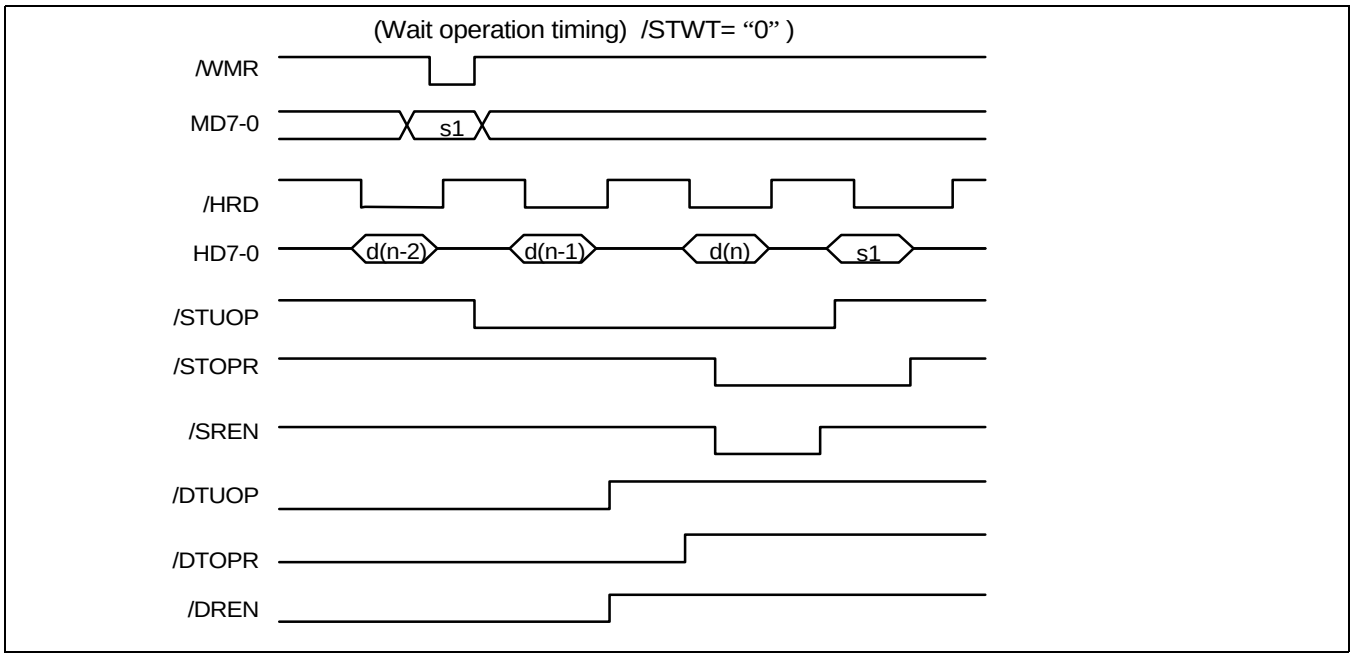
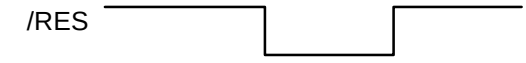


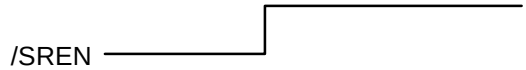
Figure 17.

NOTE: Condition: /HCS = “L”,/ CMD = “L”, /HWR = “L”
/MCS = “L”, MRS = “H”, /MRD = “H”, Address Decoder = “0”

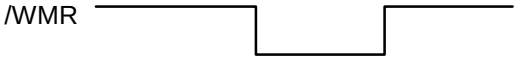
(iii) Status Transmission Stop

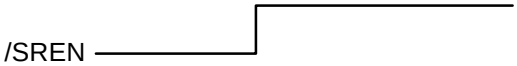
–Stop by /RES pin





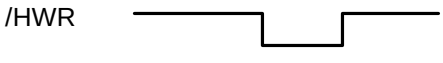
–Stop RESET rigister

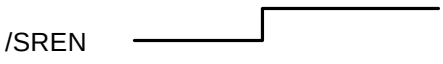




NOTE: Condition : /MCS = “L”, MRS = “H”, /MRD = “H”, Address Decoder = “15”

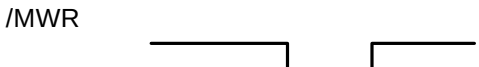
– Stop by command break

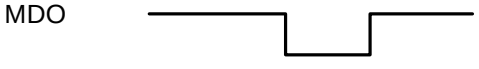




NOTE: Condition: /HCS = “L”, /CMD = “L”, /HRD = “H” /CMDBK bit of ICONT register = “0”

– Stop by STUEN bit of ICONT register





NOTE: Condition: /MCS = “L”, MRS = “H”, /MRD = “H”, Address Decoder = “1”

(d) Data Transmission

(i) Normal Operation

Normal operation occurs only when /DTWT bit of ICONT register is “0” and data transmission is available only when DTUEN bit of ICONT register is “1”. For data transmission, first, DTUEN bit should be set at “1” by writing of micom data, and then the byte number should be registered next into DTBCL. DTBCH registers are transmitted. Here the data to be registered is the value of the byte number to be registered, minus 1. The maximum amount to be transmitted is 4096 bytes. After that, the 2 X 9-bit FIFO register for data transmission is cleared by writing into DTSTR register and / DTOPR bit of ISTATE register becomes “0”. Then the /DREN pin becomes “L”, which indicates that the data transmission into host is ready. Host is enabled to read data from FIFO only when /DREN pin is “L”.

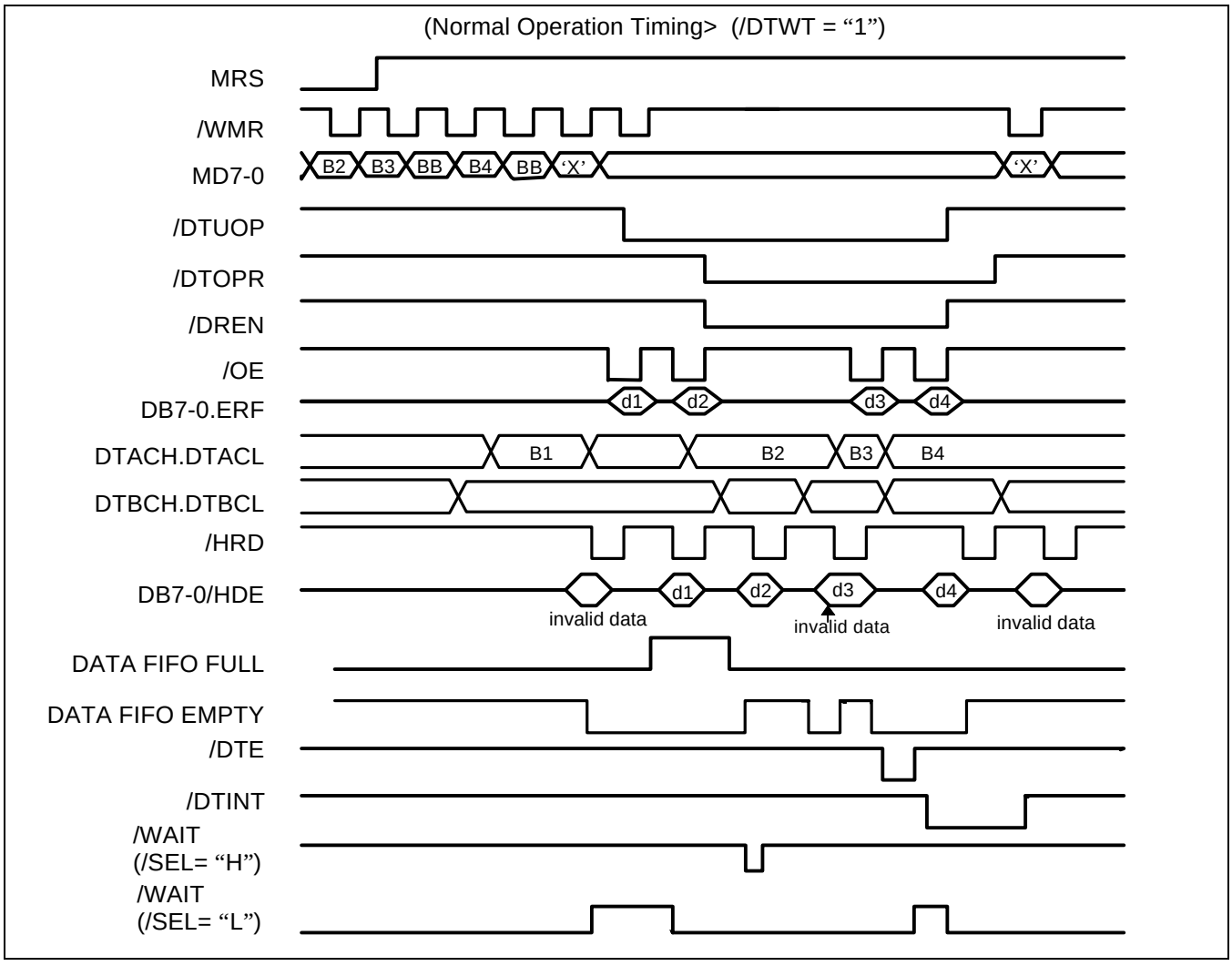


Figure 18.

NOTE: Condition: /HCS = “L”, /CMD = “L”, /HWR = “H”
/MCS = “L”, /MRD = “H”

If host reads data from FIFO when the first data is registered into FIFO, the output data will be invalid and in this case, /DTOPR bit of ISTATE register will be “0” and /DREN pin will “L” only after reading is finished at host. Data transmission is finished when host reads data so much as the byte number established by micom. The moment host starts to read the last byte, /DTUOP bit of ISTATE register becomes “1”, and /DREN bit becomes “H”. While host is reading the last byte, /DTE bit becomes “L”. During the period of finishing the reading to writing into DTEACK register, /DTINT bit of ISTATE register becomes “0”. At this moment, if the DTIEN bit of ICONT is “1” the /INT pin becomes “L”. /WAIT signal output occurs at /WAIT pin when /SEL pin is “H”. Besides, host starts to read data from FIFO for data transmission then, and if no data is written in FIFO, the /WAIT pin becomes “L”. On condition that /SEL pin is “L”, data demanding signal is generated at /WAIT pin. The /WAIT pin is valid only which host is reading data. The signal waveform of the following picture explains the case of transmission of 4 byte from 1*st address.

(ii) Wait Operation

(Wait Operation Timing)

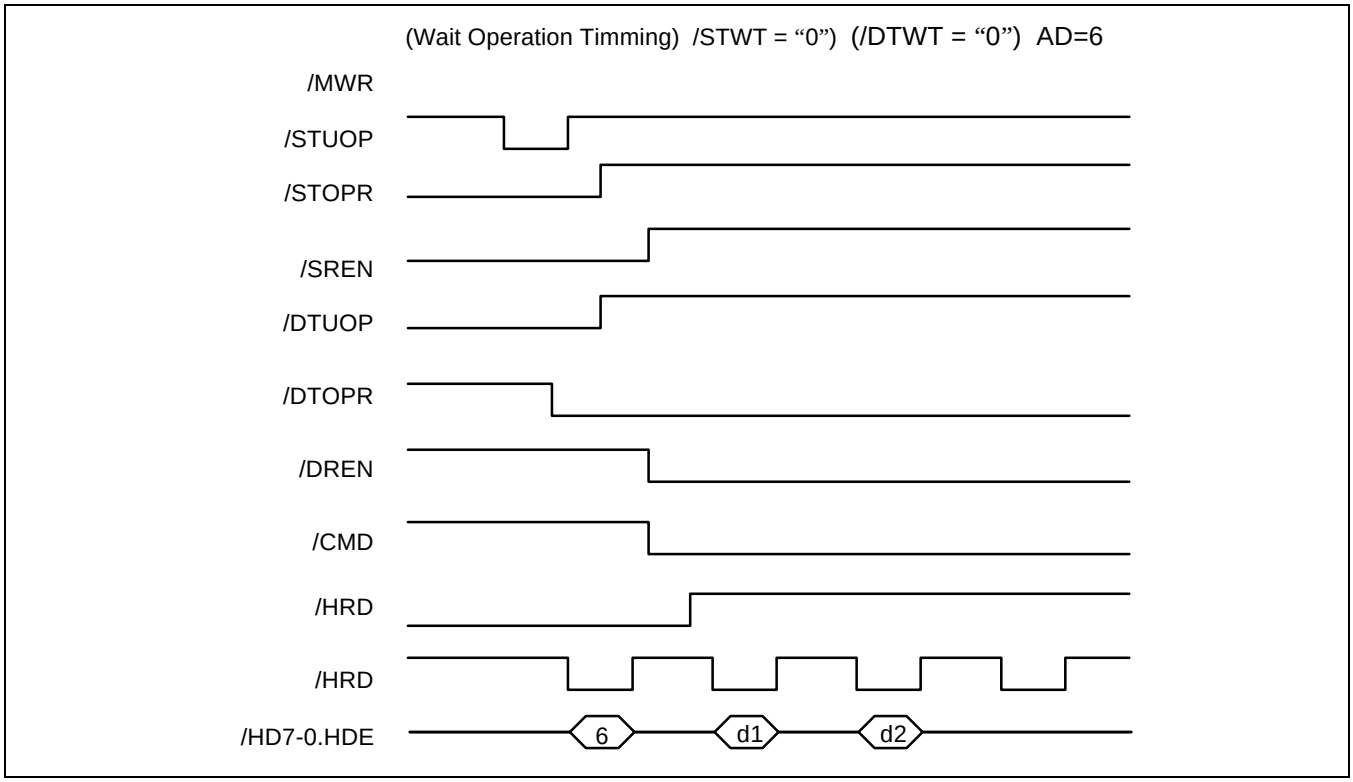


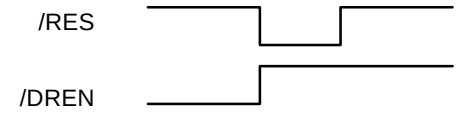
Figure 19.

NOTE: Condition : /HCS = “L”,/ CMD = “L”, /HWR = “L”
/MCS = “L”, MRS = “H”, /MRD = “H”, Address Decoder = “0”

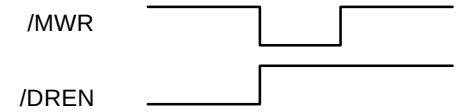
If /DTWT bit of ICONT register is “0”, wait operation is started during status byte transmission. On condition that the writing into DTSTR register is performed and finished by host, the /DTUOP bit of ISTATE register becomes “0”. However, if status was then being transmitted, /DTOPR bit of ISTATE register becomes “0” and /DREN bit becomes “L”, only when /STOPR bit of ISTATE register is “1” after status transmission is finished. After that, the operation is as follows:

(iii) Data Transmission Stop

– Stop by /RES pin

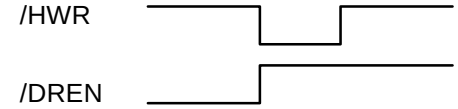


– Stop by RESET register



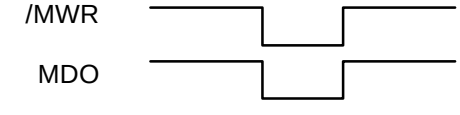
NOTE: Condition: /MCS = “L”, MRS = “H”, /MRD = “H”, Address Decoder = “15”

– Stop by Command Break



NOTE: Condition : /HCS = “L”, /CMD = “L”, /HRD = “H”, /CMDBK bit of ICONT register = “0”

– Stop by DTUEN bit of ICONT register



NOTE: Condition: /MCS = “L”, MRS = “H”, /MRD = “H”, Address Decoder = “1”

DESCRIPTION OF INTERNAL REGISTER

Read Address	Register	Data								Write Address
		D7	D6	D5	D4	D3	D2	D1	D0	
0000	COMD	MSB	–	–	–	–	–	–	LSB	–
0001	ISTATE	/CDINT	DTINT	/DTINT	1	/DTUOP	/STUOP	/DTOPR	/STOPR	–
0010	DTBCL	D7	D6	D5	D4	D3	D2	D1	D0	0010
0011	DTBCH	DTINT	DTINT	DTINT	DTINT	D11	D10	D9	D8	0011
0100	HEADER1	MSB	–	–	–	–	–	–	LSB	–
0101	HEADER2	MSB	–	–	–	–	–	–	LSB	–
0110	HEADER3	MSB	–	–	–	–	–	–	LSB	–
0111	HEADER4	MSB	–	–	–	–	–	–	LSB	–
1000	DBSPL	A7	A6	A5	A4	A3	A2	A1	A0	1100
1001	DBSPH	A15	A14	A13	A12	A11	A10	A9	A8	1101
1010	BPTRL	A7	A6	A5	A4	A3	A2	A1	A0	1000
1011	BPTRH	A15	A14	A13	A12	A11	A10	A9	A8	1001
1100	STATE1	NOERR	NOGSY	NODSY	LNGBLK	SRTWRD	SRTBLK	EFIBLK	UEIBLK	–
1101	HEADERR	H1ERR	H2ERR	H3ERR	H4ERR	SH1ERR	SH2ERR	SH3ERR	SH4ERR	–
1110	FORMAT	NDBM1	NDBM2	NDBM3	NDBM4	MODE	NOEC	NDBFM	NDBSEF	–
1111	STATE2	/DIREN	LNGWRD	ECPRC	–	–	–	–	–	–
–	STATUS	MSB	–	–	–	–	–	–	LSB	0000
–	ICONT	CDIEN	DTIEN	DCIEN	/CMDBK	/DTWT	/STWT	DTUEN	STUEN	0001
–	DTACL	A7	A6	A5	A4	A3	A2	A1	A0	0100
–	DTACH	A15	A14	A13	A12	A11	A10	A9	A8	0101
–	DTSTR	–	–	–	–	–	–	–	–	0110
–	DTEACK	–	–	–	–	–	–	–	–	0111
–	CONT1	DECEN	–	ERRCEN	AUTCEN	ERACEN	BUFEN	QCOEN	PCOEN	1010
–	CONT2	GSYEN	DSYEN	DESCEN	CDWEN	MODSEL	FRMSEL	MODCHK	SHREN	1011
–	RESET	–	–	–	–	–	–	–	–	1111

ADDRESS DECODER:

It consists of 4 bits and enables the internal register according to address output. When MRS and /MCS are “L”, the address input to select register should be applied by micom before access to address. In case of address (1-14), access automatically adds one.
In case of address 15, it is “0”. If the address is “0”, the address remains “1” regardless of accessing register. But, MRS is then “H”, and when MRS is “L”, only the reading register makes micom read the address for the selecting register.

INFORMATION ABOUT THE REGISTER ACCESSED BY MICOM

COMD (Command) Register:

This register is designed to read commands written by the host and consists of an 8 byte FIFO.

ISTATE (Interface State) Register

- /CDINT (Command Interrupt):
  If 0, it indicates that there is command byte on CDMD register.
  If 1, it indicates that COMD register is empty.

- /DTINT (Data Transfer Interrupt):
  If 0, transmission stop register Interrupt is generated.
  The Interrupt is dissolved by writing into DTEACK register.

- /DCINT (Decoder Interrupt):
  Decoder Interrupt is generated if “0”.
  The Interrupt is dissolved by reading of STATE 2.

- /DTUOP (Data Transfer Unit Operation):
  If “0”, the data transmission circuit is operative.

- /STUOP (Status Transfer Unit Operation):
  If “0” , the data transmission circuit is operative.

- /DTOPR (Data Transfer Unit Operation):
  If “0”, Data transmission is performed.

- /STOPR (Status Transfer Operation):
  If “0”, status is being transmitted.

DTBCL (Data Transfer Byte Counter Low) Register

DTBCH (Data Transfer Byte Counter High) register:
It is a counter to count the transmitted byte number during data transmission to host. DTBCL is LSB 8 bits and DTBCH is MSB 4 bits. Both are 12-bit Down-Counter. The information (the byte number to be transmitted, minus one) about data volume, is to be transmitted to host and is supposed to be applied from host.

HEADER 1-4 Register

This register is able to read header and subheader according to SHREN bit of CONT 2 register. When SHREN = 0, the HEADER 4 register in HEADER 1 indicates minutes, seconds, blocks, mode in header. If SHREN = 1, HEADER 4 register in HEADER 1 indicates file number, channel number, subcode number, coding information of each subheader.

In terms of reading subheader, from 16th to 19th byte are read on condition that the first sync byte is 0th byte. However, on condition that error flag is set, the data is replaced from 20th to 23th byte. In case of corresponding 2 bytes with error flag which is set, 20th to 23th byte are read.

DBSPL (Decoding Block Start Pointer Low) Register

DBSPH (Decoding Block Start Pointer High) Register:
They indicate the forwarding address of the block which is under decoding, and DBSPL register indicates LSB 8 bits and DBSPH register indicates MSB 8 bits. Further more, the forwarding address means the address of header's first byte. Since this register is in control of micom , the block can be changed by micom.

BPTRL (Buffering Pointer Low) Register/ BPTRL (Buffering Pointer High) Register

It is a counter about the address which are applied from DSP for CDP system and buffered at RAM.

STATE 1 register

- NOERR (No Error):
  If "1", the result of 32 bit CRC indicates no error in the block.

- NOGSY (No Generated Sync):
  If "1", the sync detected by input data is different from the internal sync by word counter.
  Then, the decoder is synchronized by the detected sync.

- NODSY (No Detected Sync):
  If "1", the sync by input data is not detected at the position of the internal sync by word counter.
  Then, the decoder is synchronized by generated sync.

- LNGBLK (Long Block):
  If "1", the sync from input data at the position of internal sync is not detected on condition that GSYEN of CONT 2 register and DSYEN is "1" .
  This result indicates that the 1 indicates that the 1 block duration time gets longer

- SRTWD (Short Word):
  If "1", it indicates that one word period is shorter than 192 clock of XIN bit signal, and then the decoder operation is stopped.

- SRTBLK (Short Block):
  If "1", the detected sync from input data is different from the internal sync, on condition that GSYEN is "1" and DSYEN is "0" in CONT 2 register.

- EFIBLK (Erasure Flag In Block):
  If "1", it indicates that there is more than one error flag which is set in block. Here, the block is from header to EDC parity.

- UEIBLK(Uncorrectable Errors In Block):
  If "1" , it indicates that more than one codeword of uncorrectable error is found. Here, the block is from header to ECC parity.

HEADERR (Head / Subheader Error) Register

- H1ERR - H4ERR:
  Error flag about each minutes, seconds, blocks, and mode byte.

- SH1ERR - SH2ERR:
  Error flag about the byte of file number, channel number, submode number, coding information. In this case, if only one of 2 bytes is error, the error flag becomes “0”,and if both of 2 bytes are errors, the error flag becomes “1”.

FORMAT Register

- NDBM1 - NDBM4 (Next Decoding Block Mode):
  It indicates the mode byte conditions of the block to be decoded at the next stage.
  NDBM1 = Mode byte bit 7 + bit 6 + bit 5 + bit 4 + bit 3 + error flag of mode byte
  NDBM2 = Mode byte bit 2 + error flag of mode byte
  NDBM3 = Mode byte bit 1 + error flag of mode byte
  NDBM4 = Mode byte bit 0 + error flag of mode byte

- MODE:
  It indicates the mode when the block is decoded, For example, if “0”, it indicates mode 1 and If “1”, mode 2.

- NOEC (No Error Correction):
  If “1”, the error correction is prohibited.

- NDBFM (Next Decoding Block Form):
  It indicates the subheader’s form bit before the error correction of the block which should be decoded.
  And it is valid only when NDBSEF is “1”.

- e. NDBSEF(Next Decoding Block Submode byte Error Flag):
  Error flag of submode byte of the subheaders in the block which should be decoded.

STATE 2 Register

- DIREN (Decoder Interrupt Register Enable):
  If “0”, the register about Decoder Interrupt is valid.

- /LNGWRD (Long word):
  If “1”, it indicates when the one word period is longer than 192 clock of XIN pin signal, and then the Decoder operation is not affected by the process.

- ECPRC (Error Correction Processing):
  If “1”, it indicates that error correction is being performed.

STATUS Register

It is a register designed to transmit the status data into the the host.

ICONT (Interface Control) Register

- CDIEN (Command Interrupt Enable)/
  DTIEN (Data Transfer Interrupt Enable)/ DCIEN (Decoder Interrupt Enable): On condition that the corresponding bit or ISTATE register is “0”, if the Interrupt Enable bit is “1”, the /INT pin is “L”.

- /CMDBK (Command Break):
  If “0”, and the host writes commands, during the status transmission into host, the transmission of data or status will be stopped.

- /DTWT (Data Wait):
  If “1”, the data transmission into host is performed irrelative to the status transmission.
  If “0”, on condition that /SREN bit is “L”, the status transmission operation is delayed.

- /STWT (Status Wait):
  If “1”, the status transmission to host is performed irrelative to the data transmission.
  If “0”, on condition that /DREN bit is “L” the status transmission operation is delayed.

- DTUEN (Data Transfer Unit Enable):
  If the data bit is set to “1”, the data transmission circuit is enabled to operate.
  During data transmission, the transmission is stopped if the data bit is “0”.

- STUEN (Status Unit Enable):
  If the data bit is set to “1”, the data transmission circuit is enabled to operate.
  When the data bit is “0”, during status transmission, the transmitting operation is stopped.

DTACL(Data Transfer Address Counter Low) /DTACH (Data Transfer Address Counter High) Register

It is a counter to indicate the transmission data address while data transmitting into the host. When the start address of data to be transmitted from micom is applied into this register, the counter value will be increased automatically by one as one byte is transmitted.

DTSTR (Data Transfer Start) Register

The writing into this register starts the data transmission into the host.
The data to be written is “Don’t care”.

DTEACK (Data Transfer End Acknowledge) register

/DTINT is set to “1” with the writing operation in this register. While writing data, the data is “Don’t care”.

CONT1 (Control1) Register

- DECEN (Decoder Enable):
  If the data bit is “1”, buffering, ECC and EDC are performed and the established bit of BUFEN, QCOEN, PCOEN of CONT1 register are valid.
  If the data bit is “0”, the Decoder is not operational. However, the establishment of the above flag is available and the flag will be valid when DECOPR becomes “1”.

- ERRCEN (Error Correction Enable):
  If the data bit is “1”, the error correction is enabled to operate.

- AUTCEN (Auto Correction Enable):
  When the data is “1”, the error correction is performed on condition that form 1 is available by form of bit within the subheader.
  On the contrary, the error correction is not operational in case of form 2. This flag is valid only if MODSEL bit of CONT2 register is “1”.

- ERACEN (Erasure Correction Enable):
  When data bit is “1”, the Erasure correction is enabled after the Erasure flag data read from RAM is enabled.
  When this data bit is “0”, the Erasure flag is always considered as “1”.

- BUFEN (Buffering Enable):
  When the data bit is “1”, the buffering is enabled and the decoding block start pointer of DBSPL /DBSPH is renewed.

- QCOEN (Q Code Correction Enable):
  When the data is “1”, the error correction for Q code is enabled.

- PCOEN (P Code Correction Enable):
  When the data is “1”, the error correction for P code is enabled.

CONT2 (Control2) register

- GSYEN (Generated Sync Enable):
  When the data bit is “1”, the internal sync which is generated by word counter is valid.
  1 word is 2 bytes and 1 block is 2352 bytes. Therefore the word counter is enabled to make 1 block period to gather 1176th syncs.

- DSYEN (Detected Sync Enable):
  When the data bit is “1”, it makes the sync, which is detected from the applied input serial data vaild.

- DESCEN (Descrambling Enable):
  When the data bit is “1”, Descrambling is available.

- CDWEN (Corrected Data Write Enable):
  When the data bit is “1”, it makes available writing of the data, which is through error correction into RAM.

- MODSEL (Form Select):
  When the data bit is “0” , the Decoder Mode is established through mode 1, and it is established through mode 2, when the bit is “1” .

- FRMSEL (Form Select):
  This flag is valid only when AUTCEN of CONT1 register is “0” and MODSEL of CONT2 register is “1”. Besides it indicates Form 1 when the bit is “0” and Form 2 when the bit is “1”.

- MODCHK (Mode Check):
  When the bit is “1”, the error correction can be performed only when the mode of MODSEL and mode byte of the header before error correction coincide.
  When the bit is “0”, the error correction performance is affected by the mode of MODSEL only.

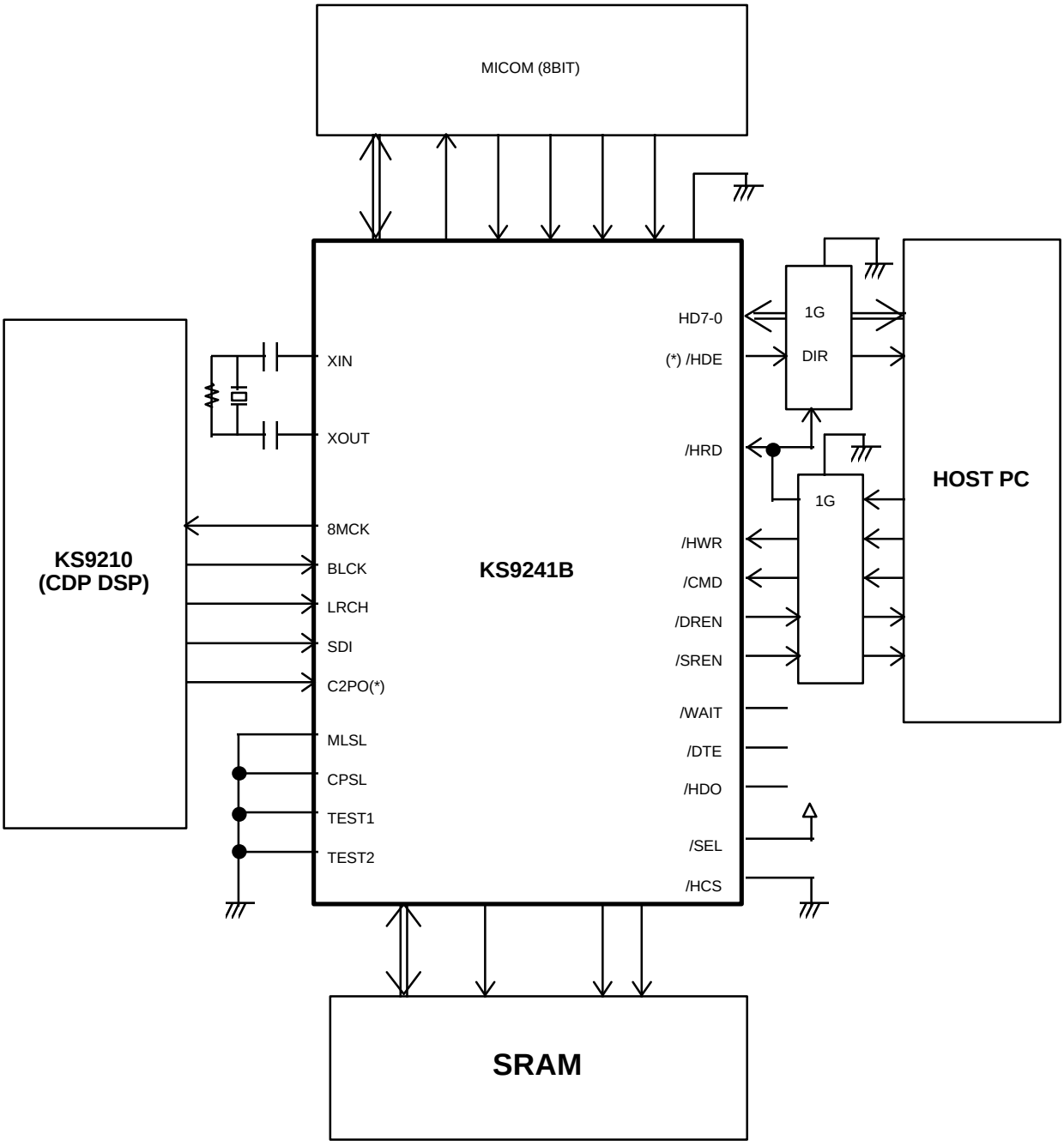
- SHREN (Subheader Read Enable):
  When the data bit is “0”, it enables to read the header, and when the bit is “0”, reading the subheader is enabled.

RESET Register

The chip reset is performed after writing into this register.

CD-ROM DRIVE SYSTEM

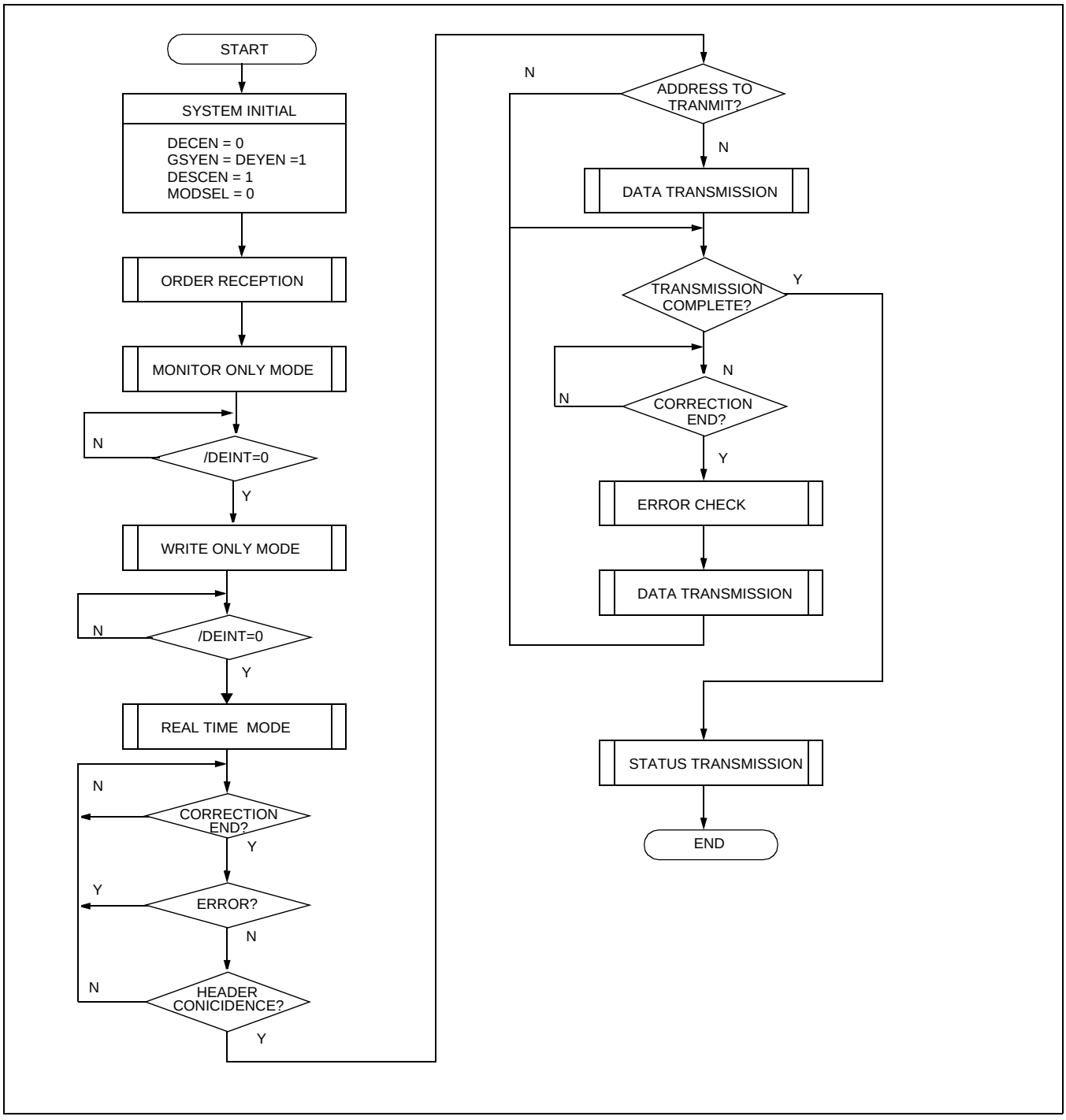
EXAMPLE OF MICOM PROGRAM)



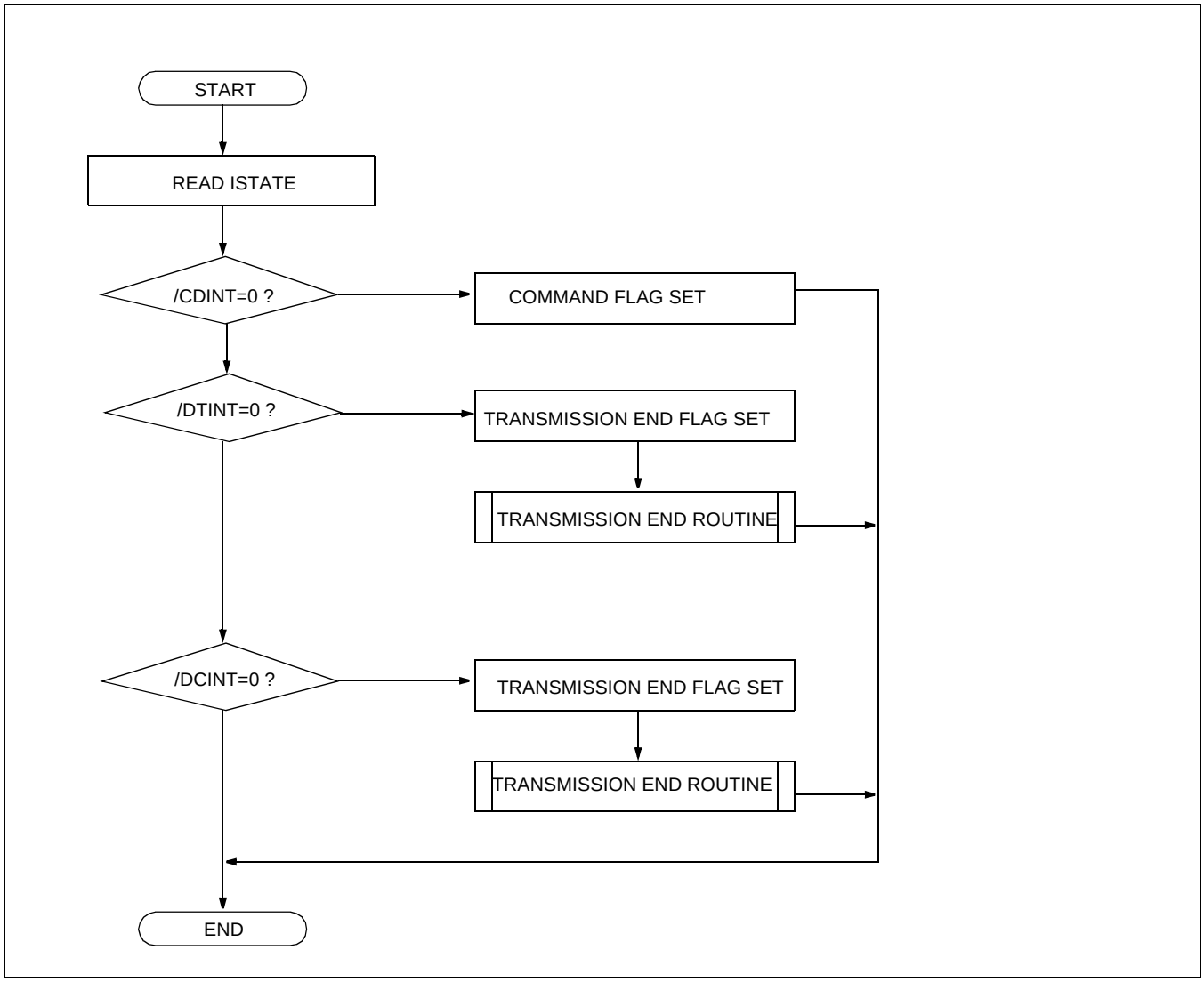
(NOTE) In case of Erasure correction

EXAMPLE OF MICOM PROGRAM

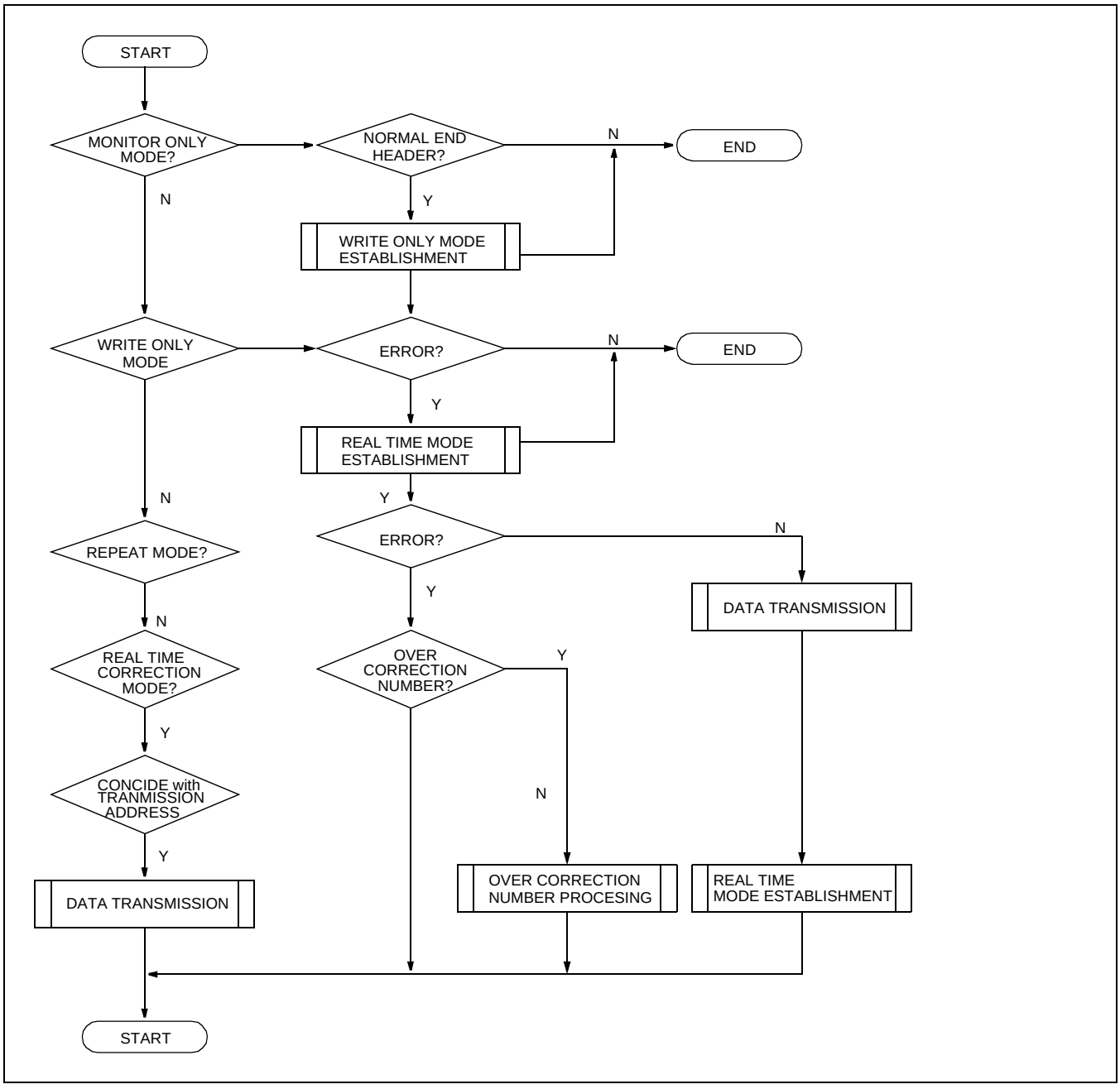
(Example 1 : Normal Operation Routine)



(Example 2 : Interrupt Processing Routine)

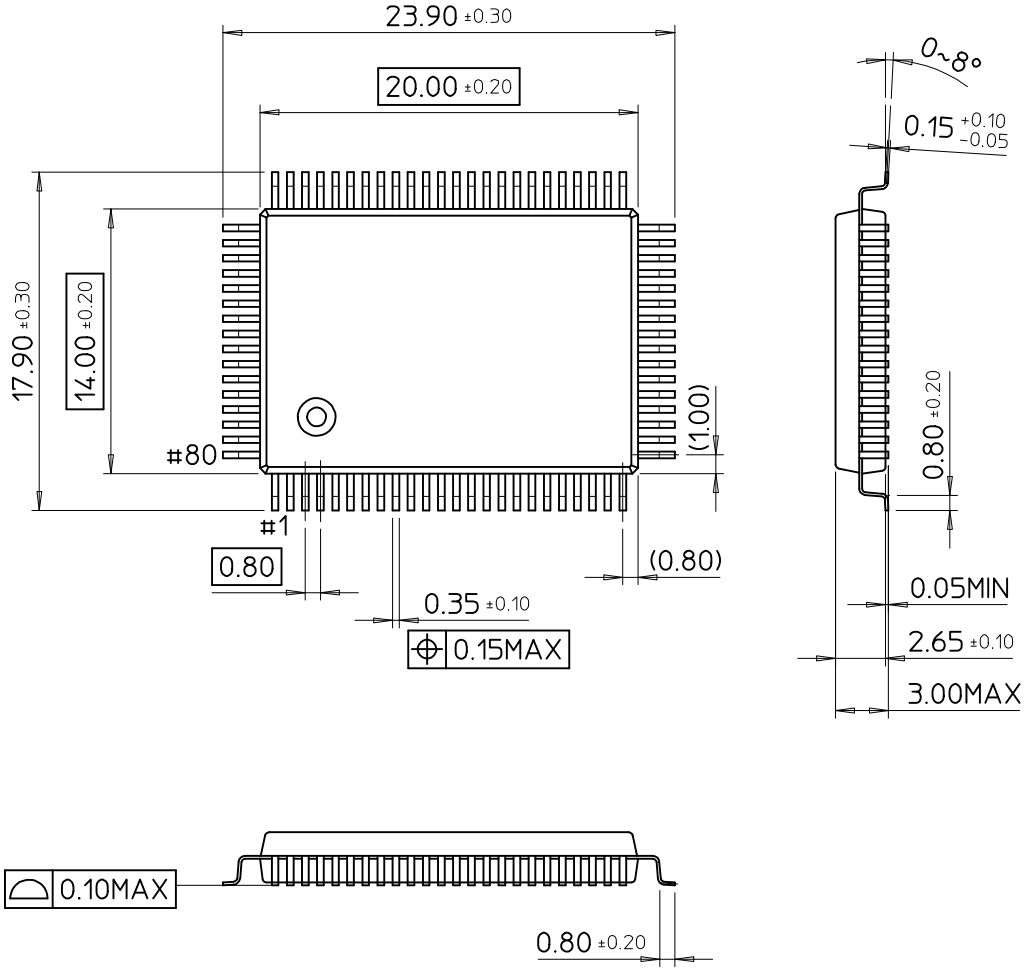


(Example 3 : Correction End Routine)



80-QFP-1420C

Dimensions in Milimeters



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