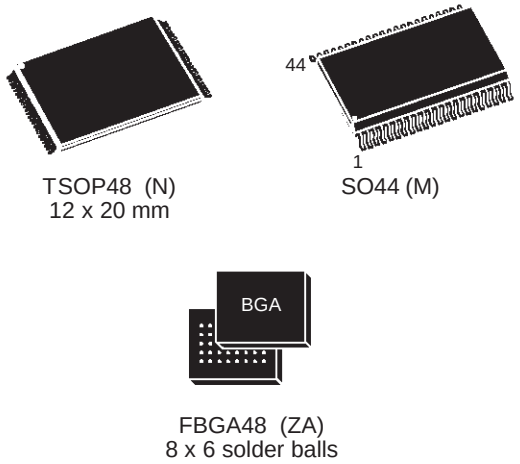
# M29W400T
# M29W400B

## 4 Mbit (512Kb x8 or 256Kb x16, Boot Block) Low Voltage Single Supply Flash Memory

**DATA BRIEFING**

- 2.7V to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- FAST ACCESS TIME: 90ns
- FAST PROGRAMMING TIME
  - 10µs by Byte / 16µs by Word typical
- PROGRAM/ERASE CONTROLLER (P/E.C.)
  - Program Byte-by-Byte or Word-by-Word
  - Status Register bits and Ready/Busy Output
- MEMORY BLOCKS
  - Boot Block (Top or Bottom location)
  - Parameter and Main blocks
- BLOCK, MULTI-BLOCK and CHIP ERASE
- MULTI BLOCK PROTECTION/TEMPORARY UNPROTECTION MODES
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- LOW POWER CONSUMPTION
  - Stand-by and Automatic Stand-by
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS DATA RETENTION
  - Defectivity below 1ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code, M29W400T: 00EEh
  - Device Code, M29W400B: 00EFh

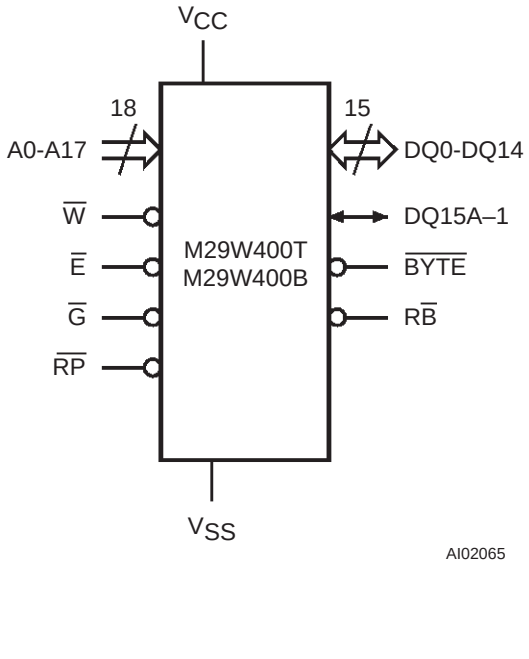



TSOP48 (N)
12 x 20 mm

SO44 (M)

FBGA48 (ZA)
8 x 6 solder balls

### Logic Diagram

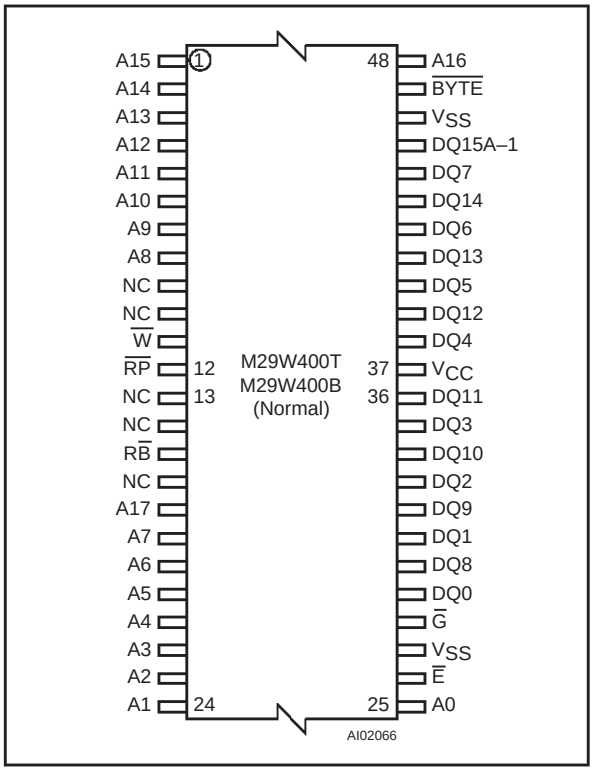



### DESCRIPTION

The M29W400 is a non-volatile memory that may be erased electrically at the block or chip level and programmed in-system on a Byte-by-Byte or Word-by-Word basis using only a single 2.7V to 3.6V $V_{CC}$ supply. For Program and Erase operations the necessary high voltages are generated internally. The device can also be programmed in standard programmers.

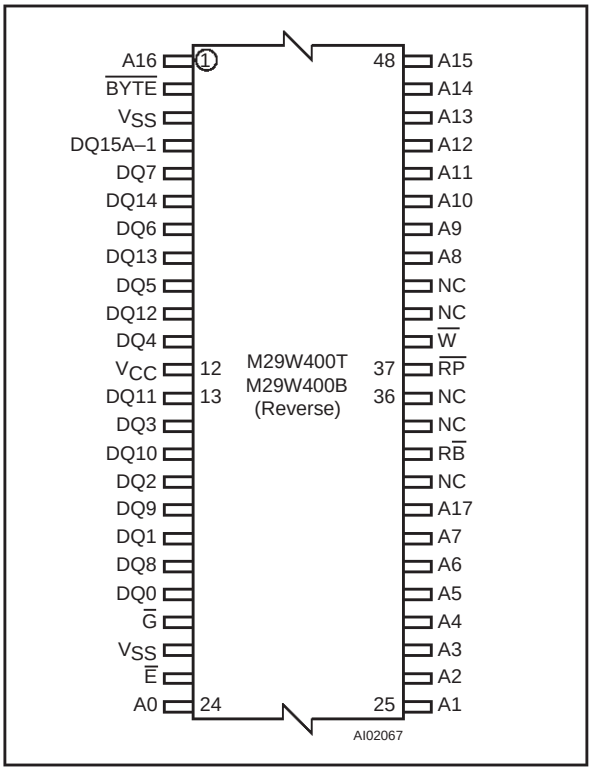
The array matrix organisation allows each block to be erased and reprogrammed without affecting other blocks. Blocks can be protected against programing and erase on programming equipment, and temporarily unprotected to make changes in the application. Each block can be programmed and erased over 100,000 cycles.

### TSOP Pin Connections



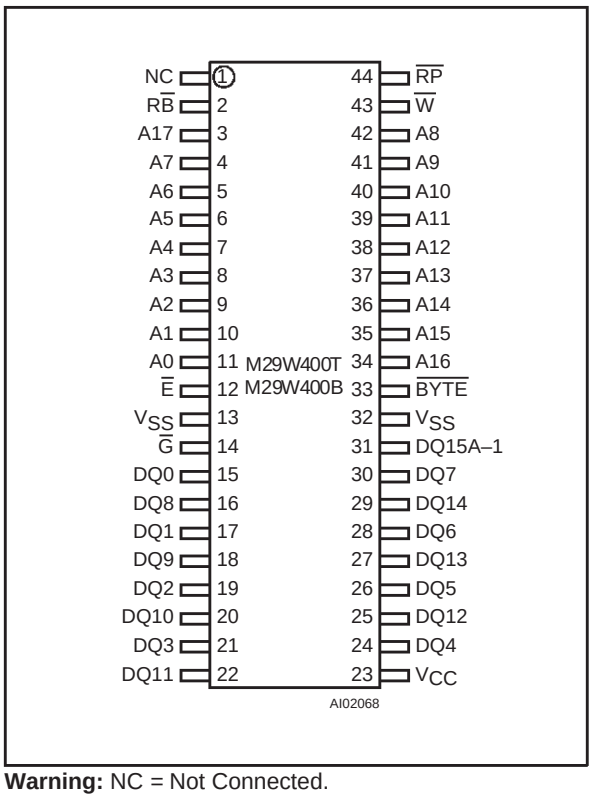

**Warning:** NC = Not Connected.

### TSOP Reverse Pin Connections




**Warning:** NC = Not Connected.

### SO Pin Connections

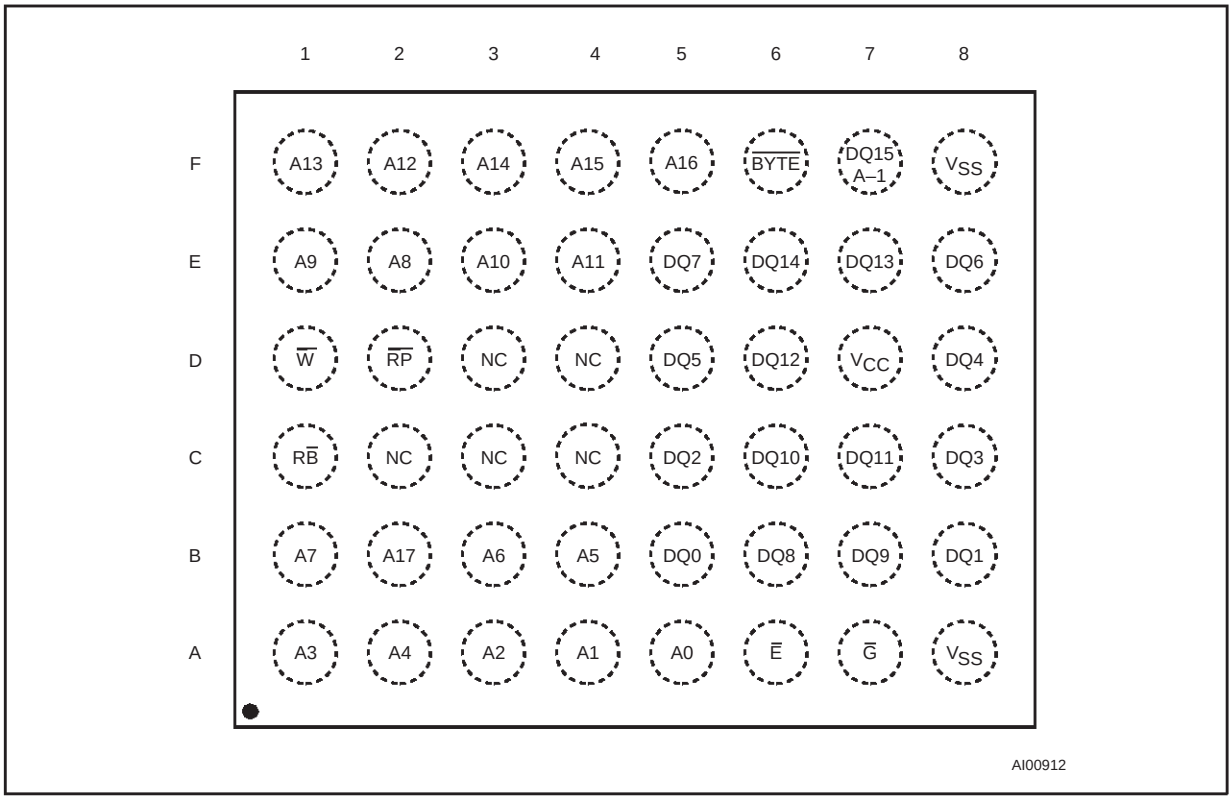



**Warning:** NC = Not Connected.

### Signal Names

| | |
|---|---|
| A0-A17 | Address Inputs |
| DQ0-DQ7 | Data Input/Outputs, Command Inputs |
| DQ8-DQ14 | Data Input/Outputs |
| DQ15A–1 | Data Input/Output or Address Input |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $\overline{RP}$ | Reset / Block Temporary Unprotect |
| $R\overline{B}$ | Ready/Busy Output |
| $\overline{BYTE}$ | Byte/Word Organisation |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

### FBGA Package Ball Out (Top View)

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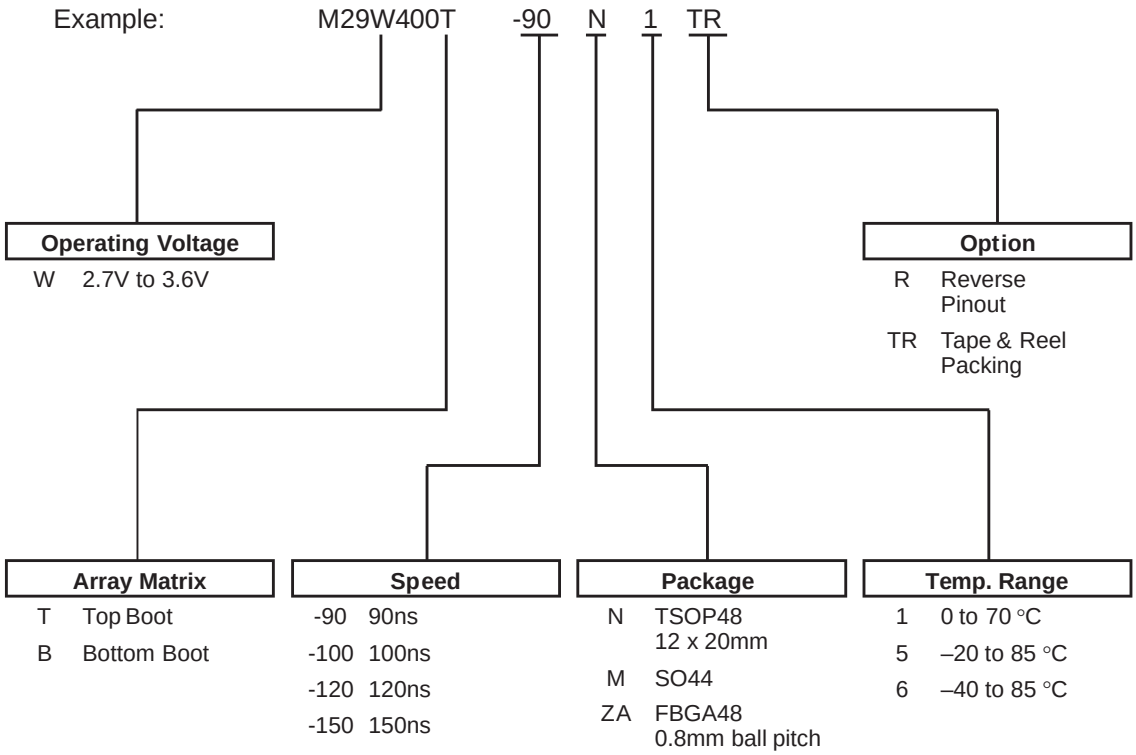
## ORDERING INFORMATION SCHEME




Devices are shipped from the factory with the memory content erased (to FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.