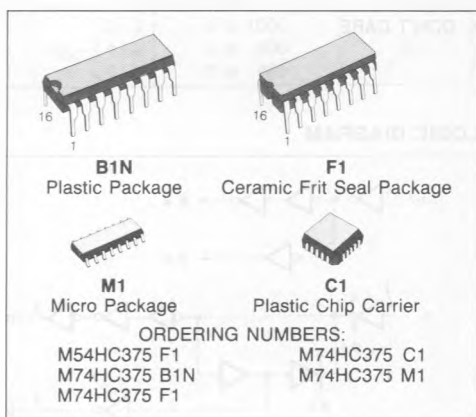


QUAD D TYPE LATCH

- **HIGH SPEED**
 $t_{PD} = 13 \text{ ns (TYP.) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 1 \mu A \text{ (MAX.) at } T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS375

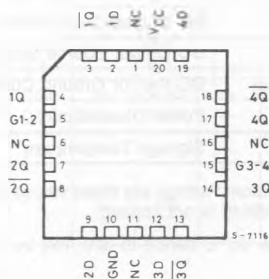
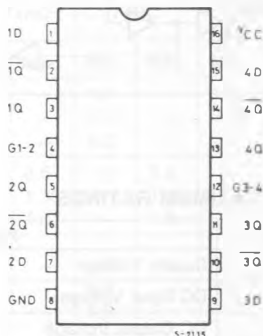


DESCRIPTION

The M54/74HC375 is a high speed CMOS QUAD D TYPE LATCH fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. It contains two groups of 2-bit latches controlled by an enable input (G1·2 or G3·4). These two latch groups can be used in the different circuits. Each latch has Q and $\bar{Q}$ outputs (1Q to 4Q and 1 $\bar{Q}$ to 4 $\bar{Q}$). The data applied to the data input is transferred to the Q and $\bar{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input at that time is retained at the outputs.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



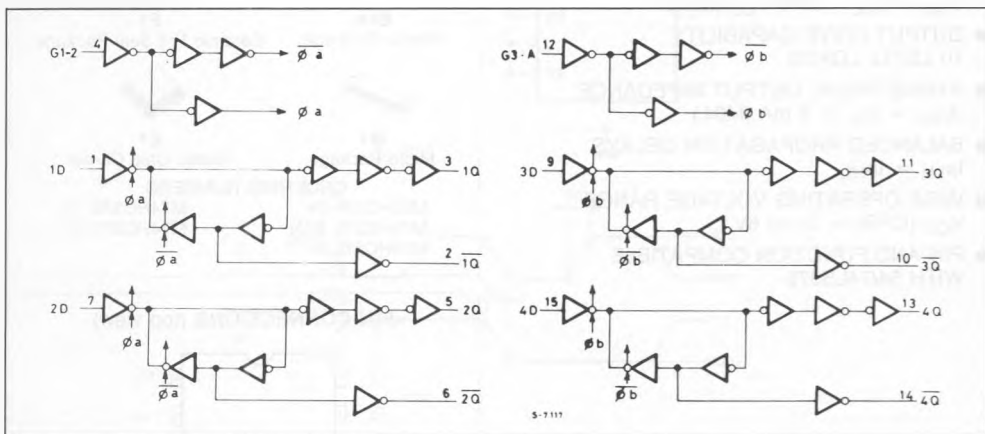
NC =
No Internal
Connection

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	—
H	H	H	L	—
X	L	Qn	$\overline{Qn}$	LATCH

X: DON'T CARE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\cong$ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	V
		4.5	V_{IH} or V_{IL}	- 20 μA	4.4	4.5	—	4.4	—	4.4	
		6.0			5.9	6.0	—	5.9	—	5.9	
		4.5 6.0		- 4.0 mA - 5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	V
		4.5			—	0.0	0.1	—	0.1	—	
		6.0			—	0.0	0.1	—	0.1	—	
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND	—	—	± 0.1	—	± 1.0	—	± 1.0	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND	—	—	2	—	20	—	40	μA

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q, $\bar{Q}$)		12	20	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G - Q, $\bar{Q}$)		17	27	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

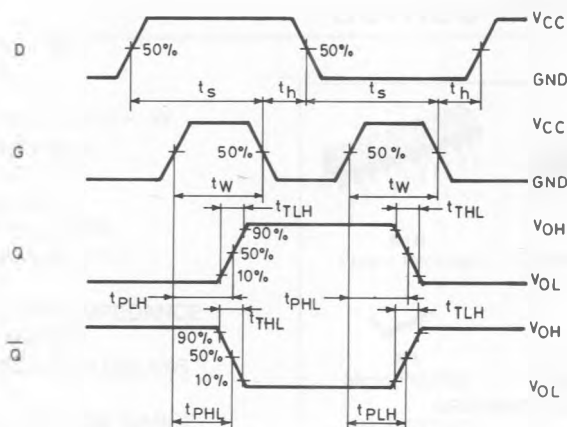
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ C$ 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Q, $\bar{Q}$)	2.0 4.5 6.0		— — —	60 15 13	120 24 20	— — —	150 30 26	— — —	180 36 31	ns
t_{PLH} t_{PHL}	Propagation Delay Time (G - Q, $\bar{Q}$)	2.0 4.5 6.0		— — —	82 20 17	160 32 27	— — —	200 40 34	— — —	240 48 41	ns
$t_{W(H)}$	Minimum Enable Pulse Width (G)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time	2.0 4.5 6.0		— — —	10 2 2	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	5 5 5	— — —	5 5 5	— — —	5 5 5	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	48	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

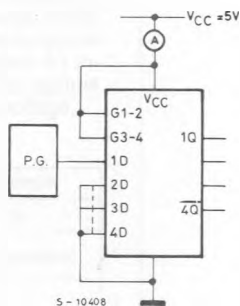
Average operating current can be obtained by the following equation.

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



S-10165

TEST CIRCUIT I_{CC} (Opr.)

INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST