MAXIM

Complete High-Speed CMOS 12-Bit ADC

MAX162/MX7572

General Description

The MAX162 and MX7572 are complete 12-Bit analog-to-digital converters (ADC's) that combine high speed, low power consumption, and an on-chip voltage reference. The conversion times are 3μs (MAX162) and 5 and 12μs (MX7572). The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX162/MX7572 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read ($\overline{RD}$) and Chip Select ($\overline{CS}$) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Features

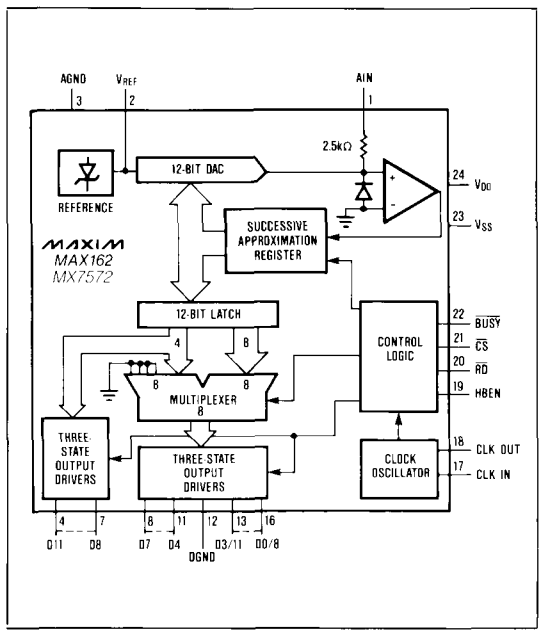
- **12-Bit Resolution and Linearity**
- **3μs (MAX162), 5μs and 12μs (MX7572) Conversion Times**
- **No missing Codes**
- **On-Chip Voltage Reference**
- **90ns Access Time**
- **215mW Max Power Consumption**
- **24-Lead Narrow DIP Package**

Ordering Information

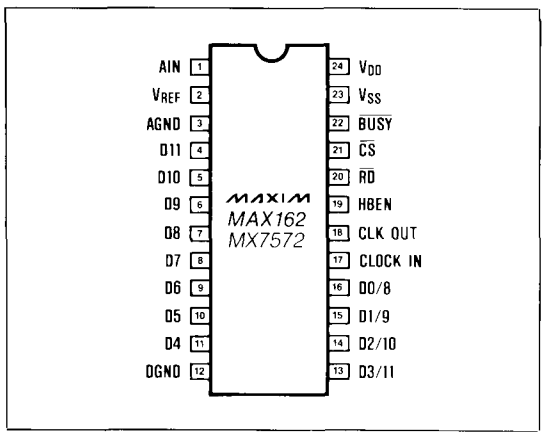
PART	TEMP. RANGE	PACKAGE*	ERROR
3μs CONVERSION TIME			
MAX162ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX162BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX162CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX162ACWG	0°C to +70°C	Wide S.O.	±½ LSB
MAX162BCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX162CCWG	0°C to +70°C	Wide S.O.	±1 LSB
MAX162CC/D	0°C to +70°C	Dice**	±1 LSB
MAX162AING	-25°C to +85°C	Plastic DIP	±½ LSB
MAX162BING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX162CING	-25°C to +85°C	Plastic DIP	±1 LSB
MAX162AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX162BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX162CMRG	-55°C to +125°C	CERDIP	±1 LSB

* *All devices — 24 lead packages*
** *Consult factory for dice specifications*
Ordering Information continued on last page.

Functional Diagram



Pin Configuration



ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V ±5%, V_{SS} = -15V ±5%, Slow Memory Mode: T_A = T_{MIN} to T_{MAX} unless otherwise noted
f_{CLK} = 4MHz for MAX162, 2.5MHz for MX7572XX05 and 1MHz for MX7572XX12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY REJECTION							
V_{DD} Only		FS Change, V_{SS} = -15V, V_{DD} = 4.75 to 5.25V			±1/2		LSB
V_{SS} Only		FS Change, V_{DD} = 5V MAX162/MX7572 MAX162	 V_{SS} = -14.25V to -15.75V V_{SS} = -11.4V to -12.6V		 ±1/8 ±1/8		 LSB LSB
LOGIC INPUTS							
Input Low Voltage	V_{IL}	CS, RD, HBEN, CLKIN				0.8	V
Input High Voltage	V_{IH}	CS, RD, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C_{IN}	CS, RD, HBEN, CLKIN				10	pf
Input Current	I_{IN}	CS, RD, HBEN, CLKIN	 VIN = 0 to V_{DD}			±10 ±20	µA
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, BUSY, CLKOUT	I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	D11-D0/8, BUSY, CLKOUT	I_{SOURCE} = 200µA	4			V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	µA
Floating State Output Capacitance (Note 7)	C_{OUT}					15	pf
CONVERSION TIME							
MAX162	t_{CONV}	f_{CLK} = 4MHz	Synchronous (13 clock cycles) Asynchronous (12 to 13 clock cycles)	3		3.25 3.25	µs
MX7572XX05	t_{CONV}	f_{CLK} = 2.5MHz	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	4.8		5 5.2	µs
MX7572XX12	t_{CONV}	f_{CLK} = 1MHz	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	12		12.5 13	µs
POWER REQUIREMENTS							
V_{DD}		±5% for Specified Performance		4.75	5	5.25	V
V_{SS} (Note 8)		±5% MAX162 ±5% MX7572			-12 or -15 -15		V
I_{DD}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			5	7	mA
I_{SS}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V			8	12	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V			145	215	mW

Note 1: Typical change over temp is ±1LSB
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5.000V, Ideal last code transition = FS -3/2LSB
Note 3: Full Scale TC = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25 C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} TC = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25 C to T_{MIN} or T_{MAX}.
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: V_{SS} = -12V ±5% for the MAX162 only. Functional operation is guaranteed by testing offset error and full scale error.

TIMING CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = -12V or -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX121C/E		MAX121M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CONVST}$ Pulse Width (Note 6)	t_{CW}		20			30		35		ns
Data-Access Time	t_{DA}	C_L = 50pF		25	50		65		80	ns
Data-Hold Time	t_{DH}			25	50		65		80	ns
CLKIN to SCLK	t_{CD}	C_L = 50pF		40	65		85		105	ns
SCLK to SDATA Skew	t_{SC}	C_L = 50pF			±65		±80		±100	ns
SCLK to SFRM or FSTRT Skew	t_{SC}	C_L = 50pF			±25		±35		±40	ns
Acquisition Time (Note 6)	t_{AQ}		400			400		400		ns
Aperture Delay	t_{AP}			10						ns
Aperture Jitter				30						ps
Clock Setup/Hold Time	t_{CK}		10		50	10	50	10	50	ns

Note 5: Control inputs specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V. Output delays are measured to +0.8V if going low, or +2.4V if going high. For a data-hold time, a change of 0.5V is measured. See Figures 4 and 5 for load circuits.

Note 6: Guaranteed, but not tested.

Pin Description

PIN DIP/SO	PIN SSOP	NAME	FUNCTION
1	1	V_{SS}	Negative Power Supply: -12V or -15V
2	2	V_{DD}	Positive Power Supply: +5V
3	3	AIN	Sampling Analog Input: ±5V bipolar input range
4	4	VREF	-5V Reference Output. Bypass to AGND with 22µF II 0.1µF.
5	7	AGND	Analog Ground
6	8	$\overline{INVCLK}$	Invert Serial Clock. Connect to DGND to invert the SCLK output (relative to CLKIN).
7	9	$\overline{INVFRM}$	Invert Serial Frame. This input sets the polarity of the SFRM output as follows: If $\overline{INVFRM}$ = DGND, SFRM is high during a conversion. If $\overline{INVFRM}$ = V_{DD}, SFRM is low during a conversion.
8	10	DGND	Digital Ground
9	11	SFRM	Serial Frame Output. Normally high ($\overline{INVFRM}$ = V_{DD}), falls at the beginning of the conversion and rises at the end (after 16 t_{CLK}) signaling the end of a 16-bit frame.
10	12	FSTRT	Frame Start Output. High pulse that lasts one clock cycle, falling edge indicates that a valid MSB is available.
11	13	SDATA	Serial Data Output. MSB first, twos-complement binary output code.
12	14	SCLK	Serial Clock Output. Same polarity as CLKIN if $\overline{INVCLK}$ = V_{DD}, inverted CLKIN if $\overline{INVCLK}$ = DGND. *Note that SCLK runs whenever CLKIN is active.*
13	17	$\overline{CONVST}$	Active-Low Convert Start Input. Conversions are initiated on falling edges.
14	18	CLKIN	Clock Input. Supply a TTL-/CMOS-compatible clock from 0.1MHz to 5.5MHz, 40%-60% duty cycle.
15	19	$\overline{CS}$	*Active-Low Chip-Select Input. $\overline{CS}$ = DGND enables the three-state outputs. Also, if $\overline{CONVST}$ is low, initiates a conversion on the falling edge of $\overline{CS}$.*
16	20	MODE	Hardwire to set operational mode: V_{DD}: single conversions, DGND: continuous conversions
—	5, 6, 15, 16	N.C.	*No Connect – not internally connected.*

Complete High-Speed CMOS 12-Bit ADC

TIMING CHARACTERISTICS (Note 9)

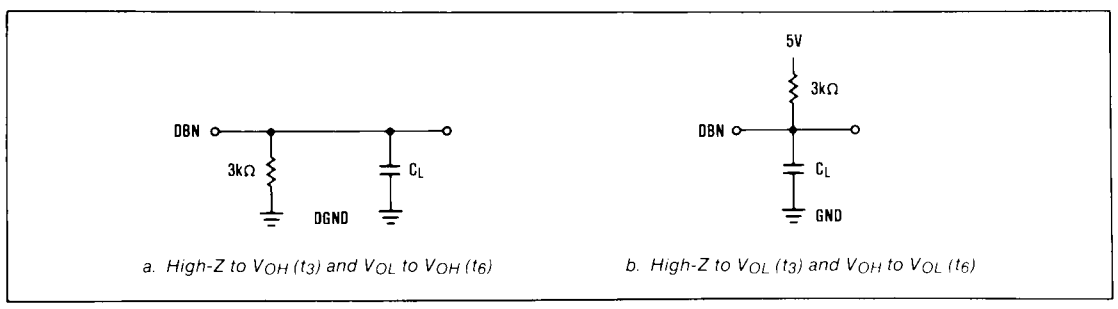
(V_{DD} = +5V, V_{SS} = -15V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C			MAX162C/I MX7572J/K/L MX7572A/B/C		MAX162M MX7572S/T/U		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CS to RD Setup Time	t_1		0			0		0		ns
RD to $\overline{BUSY}$ Delay	t_2	C_L = 50pF		90	190		230		270	ns
Data Access Time (Note 10)	t_3	C_L = 20pF C_L = 100pF		60 70	90 125		110 150		120 170	ns
RD Pulse Width	t_4		t_3			t_3		t_3		
CS to RD Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ Note (10)	t_6				70		90		100	ns
Bus Relinquish Time (Note 11)	t_7		20		75	20	85	20	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to RD Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

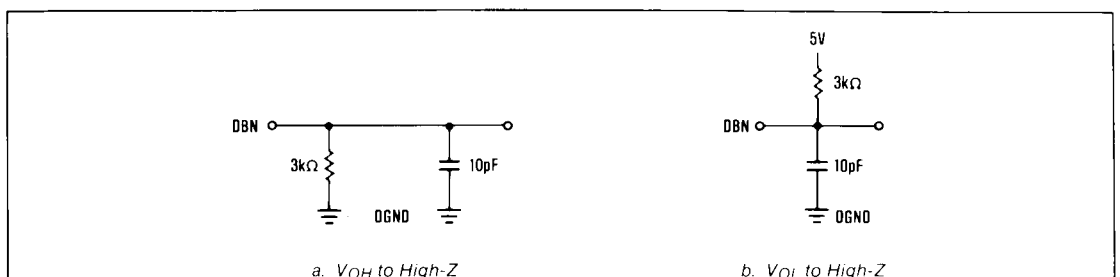
Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6) *b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

Pin Description

PIN	NAME	FUNCTION
1	AIN	Analog Input, 0 to +5V unipolar input
2	V_{REF}	-5.25V Reference Output
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3/11-D0/8	Three-State Data Outputs
17	CLKIN	Clock Input. An external TTL/CMOS compatible clock may be applied to this pin or a crystal can be connected between CLKIN and CLKOUT.
18	CLKOUT	Clock Output. An inverted CLKIN signal appears at this pin.
19	HBEN	High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7-D0/8). HBEN also disables conversion starts when HIGH.
20	$\overline{RD}$	READ Input. This active low signal starts a conversion when CS and HBEN are low. RD also enables the output drivers when CS is low.
21	$\overline{CS}$	The CHIP SELECT Input must be low for the ADC to recognize RD and HBEN inputs.
22	$\overline{BUSY}$	The BUSY Output is low when a conversion is in progress.
23	V_{SS}	Negative Supply, -15V for MX7572 and -15V or -12V for MAX162.
24	V_{DD}	Positive Supply, +5V.

Data Bus Output, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Note:
* D11 . . . D0/8 are the ADC data output pins.
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB.

Converter Operation

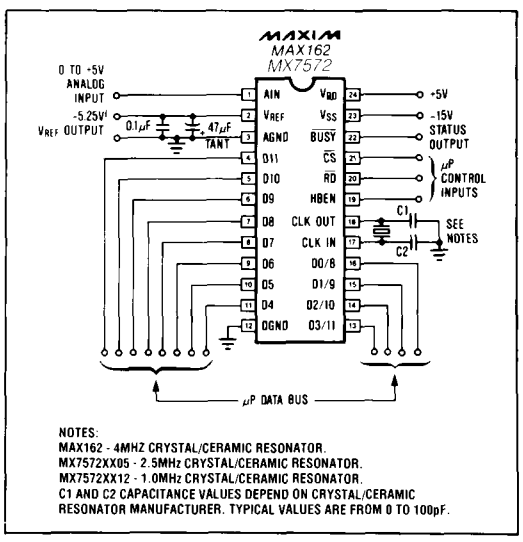


Figure 3. MAX162/MX7572 Operational Diagram

The MAX162 and MX7572 use a successive approximation technique to convert an unknown analog input to a 12 bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only a few external passive components to perform the analog-to-digital function. Figure 3 shows the MAX162/MX7572 in its simplest operational configuration.

Figure 4 shows the MAX162/MX7572analog equivalent circuit. The internal voltage output DAC is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero crossing detector and its output is fed back to the SAR input.

Conversion start is controlled by the CS, RD and HBEN digital inputs. A conversion starts at the falling edge of CS and RD while HBEN is low. Once started, conversion cannot be stopped. The BUSY output goes low as soon as the conversion starts. BUSY may be used to control an external sample-and-hold when wide bandwidth input signals are being measured.

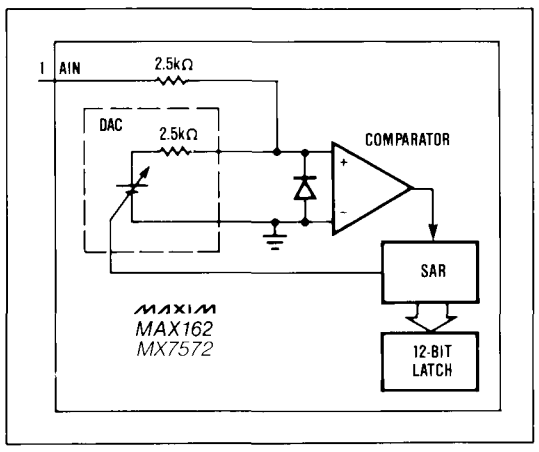


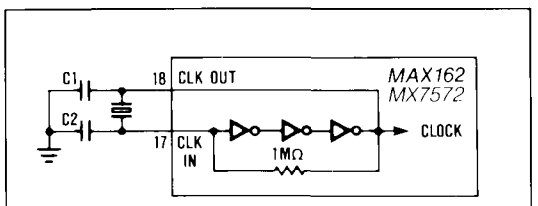
Figure 4. MAX162/MX7572 Analog Equivalent Circuit

The SAR is set to half scale as soon as the $\overline{CS}$ and $\overline{RD}$ inputs go low. This reset is asynchronous with the clock input. The analog input is then compared to one half of the full scale voltage. About 30ns after the second falling edge of CLKIN (or rising edge of CLKOUT), the output of the comparator is latched into the SAR MSB bit (see Figure 5). The bit is kept if the analog input is greater than half scale, or dropped if it is smaller. The next bit (bit 11) is then set with the DAC output either at 1/4 scale (if the MSB was dropped) or 3/4 scale (if the MSB was kept). The conversion continues in this manner until the LSB is tried. Following a falling CLKIN signal, the BUSY output goes high and the SAR result is latched into the three-state output buffers.

Clock Operation

Clock Oscillator

Figure 6 shows the MAX162/MX7572 clock circuitry. The capacitive load on the CLKOUT pin must be minimized for low power dissipation and to avoid digital coupling of the CLKOUT buffer currents to the comparator. If an external clock source is being used to drive CLKIN, CLKOUT should be left open. The external clock source must have a 50% duty cycle. If the internal oscillator is being used, a crystal/ceramic resonator should be connected between CLKOUT and CLKIN as shown in Figure 6.



NOTES:
MAX162 - 4MHZ CRYSTAL/CERAMIC RESONATOR.
MX7572XX05 - 2.5MHz CRYSTAL/CERAMIC RESONATOR.
MX7572XX12 - 1.0MHz CRYSTAL/CERAMIC RESONATOR.
C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 0 TO 100pF.

Figure 6. MAX162/MX7572 Internal Clock Circuit

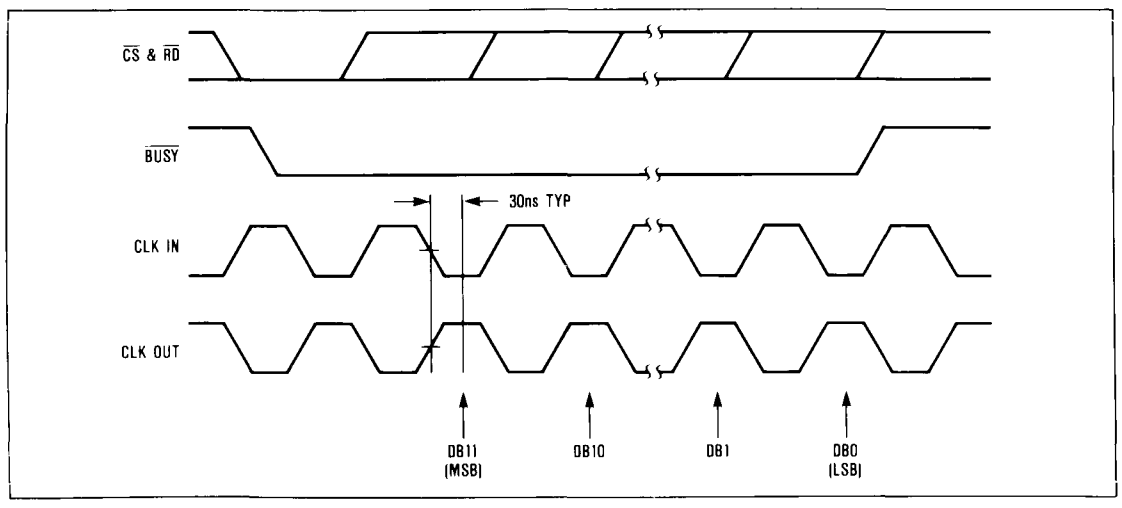


Figure 5. Operating Waveforms Using an External Clock Source for CLKIN.

Control Input Synchronization

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock, the conversion time can vary from 12 to 13 clock cycles. The SAR changes state on the falling edge of the CLKIN input (or rising edge on the CLKOUT pin). To ensure a fixed conversion time use the following guidelines for synchronization:

MAX162

For the MAX162 the $\overline{RD}$ input should go low at the falling edge of CLKIN. In this case the conversion lasts 13 clock cycles and the conversion time is 3.25μs when f_{CLK} = 4MHz. If the CLKIN and $\overline{RD}$ falling edges are skewed, the skew must not be more than 50ns to ensure the 13 period conversion time (See Figure 7). The MSB is tried at the second clock falling edge, leaving two clock cycles for the external sample-and-hold to settle from hold transients.

MX7572

The MX7572 $\overline{RD}$ input can go low at the rising edge of CLKIN. In this case the conversion lasts 12.5 clock cycles and the conversion time is 5μs when f_{CLK} = 2.5MHz and 12.5μs when f_{CLK} = 1MHz. The delay from the falling edge of $\overline{RD}$ to the falling edge of CLKIN must not be less than 180ns to ensure the 12.5 clock cycle conversion time (See Figure 8). This leaves the external sample-and-hold 1.5 clock cycles to settle from hold transients. An additional half clock cycle of settling can be allowed for driving the sample-and-hold by having $\overline{RD}$ go low at the falling edge of CLKIN, similar to the MAX162. This results in a 13 cycle conversion time (5.2μs when f_{CLK} = 2.5MHz, 13μs when f_{CLK} = 1MHz).

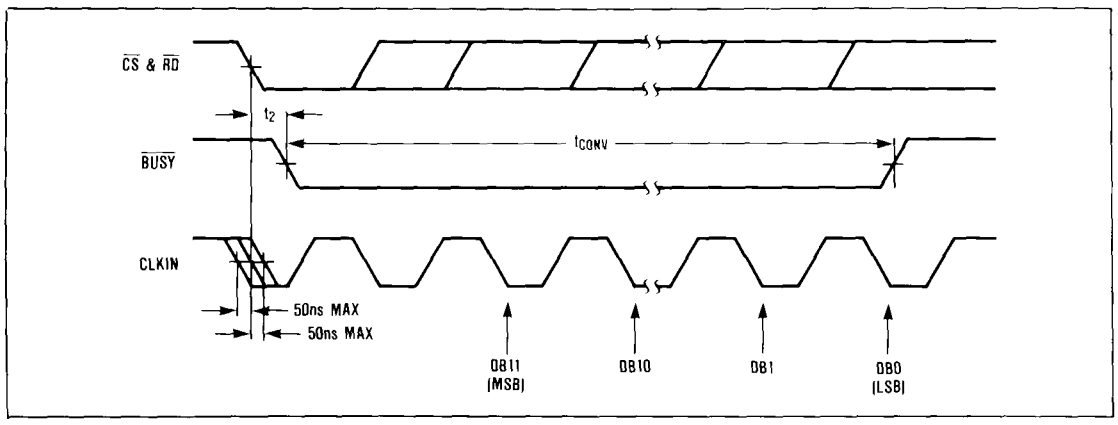


Figure 7. MAX162 $\overline{RD}$ and CLKIN For Synchronous Operation

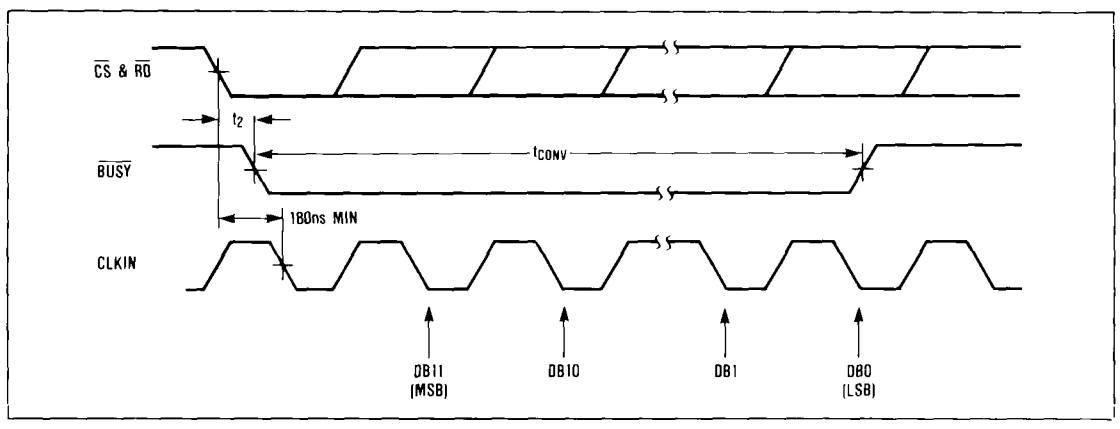


Figure 8. MX7572 $\overline{RD}$ and CLKIN For Synchronous Operation

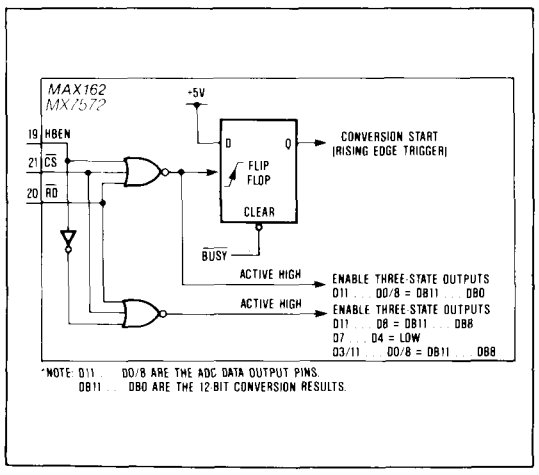


Figure 9. Logic Equivalent for RD, CS and HBEN Inputs

Digital Interface

Output Data Format

The 12 output data bits can either be presented full parallel or in two 8 bit words. To obtain parallel output for 16 bit processors, HBEN should be kept low and the output data D11-D0 will be right justified.

For a two byte data read, outputs D7-D0/8 are used. Byte selection is controlled by HBEN which multiplexes the data outputs. When HBEN is low, the lower 8 bits are presented at the data outputs. When HBEN is high, the upper 4 bits are presented with the leading 4 bits being low for D7-D0/8.

Note that the 4 MSB's always appear at digital outputs D11-D8 whenever the digital drivers are enabled, regardless of the state of HBEN.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs; HBEN, CS and RD. Figure 9 shows the logic equivalent for the conversion and data output control circuitry. A logic low is required on all three inputs to start a conversion. Once a conversion is in progress, it cannot be re-started. The BUSY output is low during the entire conversion cycle.

There are two modes of operation as outlined in the timing diagrams of Figures 10-13. Slow memory mode is intended for processors that can be forced into a WAIT state for periods as long as the MAX162/MX7572 conversion time. ROM mode is for processors that cannot be forced into a wait state. In both operational modes, a processor READ operation to the ADC address starts the conversion. In the ROM mode, a second READ operation is required to access the conversion result.

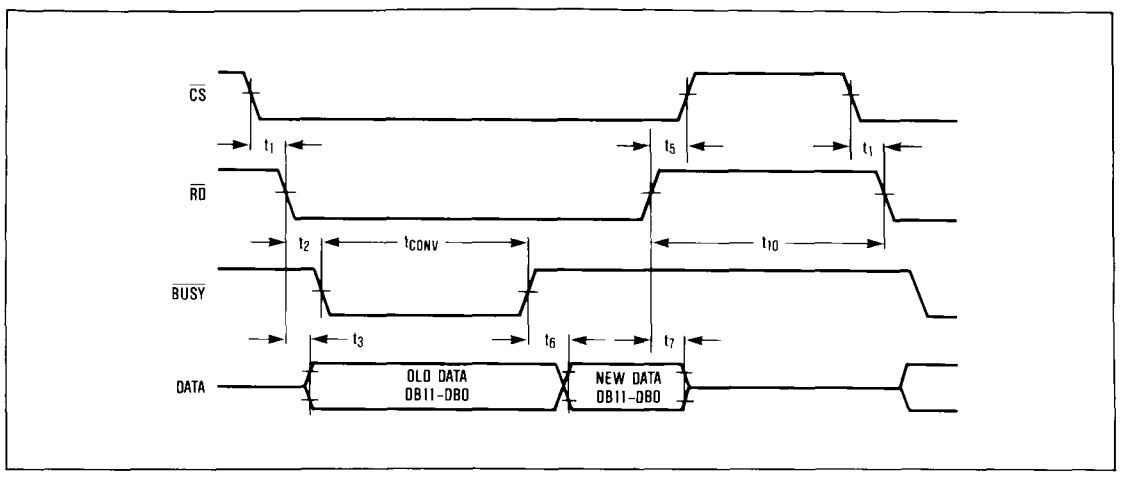


Figure 10. Slow Memory Mode, Parallel Read Timing Diagram

Table 1. Slow Memory Mode, Parallel Read Data Bus Status

MAX162/MX7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

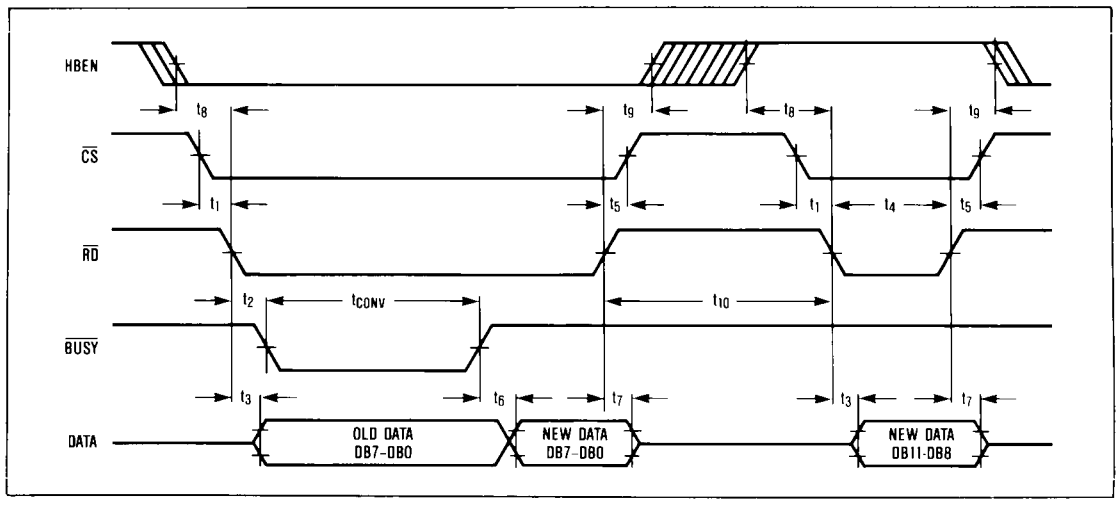


Figure 11. Slow Memory Mode, Two Byte Read Timing Diagram

Table 2. Slow Memory Mode, Two Byte Read Data Bus Status

MAX162/ MX7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

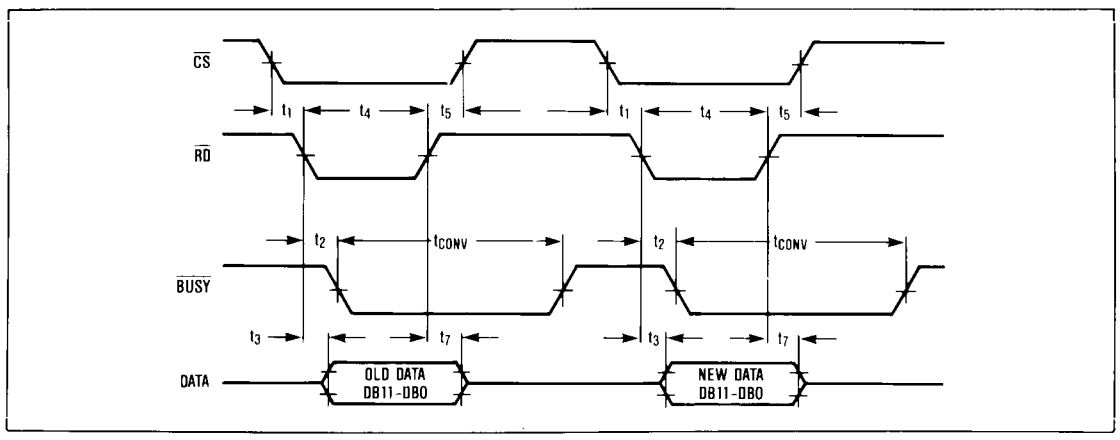


Figure 12. ROM Mode, Parallel Read Timing Diagram

Table 3. ROM Mode, Parallel Read Data Bus Status

MAX162/MX7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

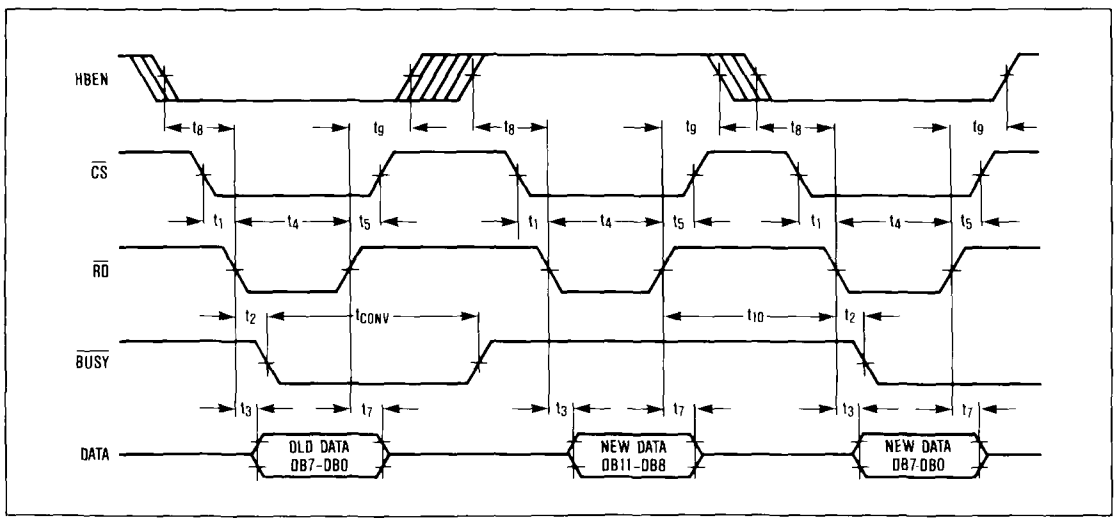


Figure 13. ROM Mode, Two Byte Read Timing Diagram

Table 4. ROM Mode, Two Byte Read Data Bus Status

MAX162/MX7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 10 and Table 1 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. CS and RD going low starts the conversion and BUSY goes low indicating that the conversion is in progress. Data from the previous conversion appears at the digital outputs. At the end of the conversion, BUSY returns high and the output latches are updated to place the digital conversion result on data outputs D11-D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only outputs D7-D0/8 are used. Starting the conversion and reading the 8 LSB's is identical to the Slow Memory Mode, Parallel Read. See Figure 11 and Table 2. A second READ operation with HBEN high places the 4 MSB's with 4 leading zeros on the data outputs D7-D0/8. The high byte read does not start another conversion since HBEN is high.

ROM Mode, Parallel Read (HBEN = LOW)

The ROM mode avoids placing the processor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion appears at the data outputs D11-D0/8 (see Figure 12 and Table 3). This data may be disregarded if not needed. A second READ operation will access the results of the first operation and also start a new conversion. The delay between successive READ operations must be longer than the conversion time for the MAX162/MX7572.

ROM Mode, Two Byte Read

As in the Slow Memory Mode, only data outputs D7-D0/8 should be used for two byte reads. Figure 13 and Table 4 show the operation in this mode. A conversion is started with a READ operation with HBEN low. The data outputs present the 8 LSB's from the previous conversion and this data can be disregarded if not required. Two more READ operations are needed to access the conversion result. The first READ must be with HBEN high, where the 4 MSB's with 4 leading zero's are accessed. The second READ is with HBEN low, which reads in the 8 LSB's and starts a new conversion.

Interface Application Hints

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, LSBs of error can be caused due to coupling from the data pins to the ADC comparator. Using the Slow Memory Mode avoids this problem by placing the processor in a wait state during the conversion. In the ROM mode, if the data bus is going to be active during the conversion, the bus should be isolated from the ADC using three-state drivers.

ROM Mode

Considerable digital noise is generated in the ADC when RD or CS go high and the output data drivers are disabled after a conversion is started. This noise will feed into the ADC comparator and cause large errors if it coincides with the time the SAR is latching a decision to keep or drop a bit. To avoid this problem, RD and CS should be active for less than one clock cycle. In other words, the RD and CS low pulse should be shorter than 250ns for the MAX162, 400ns for the MX7572XX05 and 1μs for the MX7572XX12. If this cannot be done, the RD or CS signal must go high at a rising edge of CLKIN, since the comparator output is always latched at falling edges of CLKIN.

Analog Considerations

Application Hints

Physical Layout

For best system performance printed circuit boards should be used for the MAX162/MX7572. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX162/MX7572 package.

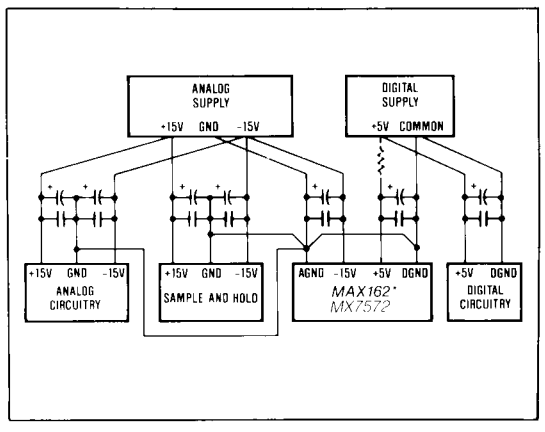


Figure 14. Power Supply Grounding Practice

Grounding

Figure 14 shows the recommended system ground connections. A single point analog STAR ground should be established at pin 3 (AGND) of the MAX162/MX7572 separate from the logic ground. All other analog grounds and pin 12 (DGND) of the MAX162/MX7572 should be connected to this STAR ground and no other digital grounds should be connected to this STAR point. The ground return to the power supply from this STAR ground should be low impedance for noise free operation of the ADC.

Power Supply Bypassing

The high speed comparator in the ADC is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be by-passed to the analog STAR ground with 0.1μF and 10μF by-pass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small (10-20 ohms) resistor can be connected as shown in Figure 14 to filter external noise.

Internal Reference

The MAX162/MX7572 has an internal buried zener reference which provides the DAC reference voltage. The reference voltage is -5.25V $\pm$1% and has a low temperature coefficient. The reference output is available at pin 2, and should be bypassed to analog ground (pin 3) with a 47μF tantalum capacitor in parallel with 0.1μF capacitor to minimize noise and provide low impedance at high frequencies. This by-pass capacitor must not be less than 4.7μF. The internal reference output buffer can sink upto 500μA.

Driving The Analog Input

The input signal leads to AGND and AIN should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5kΩ. The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion (4MHz for MAX162 and 2.5 or 1MHz for the MX7572). The output impedance of the driving amplifier is equal to its open loop output impedance divided by the loop gain at the frequency of interest.

MX7572 The MX7572 maximum clock rate of 2.5MHz makes it possible to drive it with amplifiers like the OP-42, AD711 or OP-27. At 1MHz clock rate a MAX400 or OP-07 can also be used.

MAX162 The MAX162 with a maximum 4MHz clock rate might cause settling problems with the above amplifiers. An LF356, LF400 or LT1056 can be used to drive the input. Alternatively, an emitter follower buffer inside the feedback loop of a OP-42, AD711 or OP-27 can be used to improve high frequency output impedance.

MAX162/MX7572 to Sample-and-Hold Interface

The analog input to the ADC must be stable to within 1/2 LSB during the entire conversion for specified 12 bit accuracy. This limits the input signal bandwidth to less than 6Hz for sinusoidal inputs, even when using the faster MAX162. For higher bandwidth signals a sample-and-hold should be used.

The $\overline{BUSY}$ output from the MAX162/MX7572 may be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. However, since the ADC's DAC is switched at approximately the same time as the BUSY signal goes low, the switching transients at the output of the sample-and-hold caused by the DAC switching may result in code dependent errors due to the aperture delay of the sample-and-hold. A NAND gate may be used to ensure that the sample-and-hold switches to the hold mode BEFORE any disturbances as shown in Figures 15 & 16. The NAND gate solution works only if the width of the $\overline{RD}$ pulse is wider than the $\overline{RD}$ to $\overline{BUSY}$ delay in the MAX162/MX7572. If this is not the case, use a flip flop which is set by the falling edge of $\overline{RD}$ and reset by the rising edge of $\overline{BUSY}$.

For synchronous $\overline{RD}$ and CLKIN as described above, the hold settling time allowed for the sample-and-hold is 500ns, 600ns and 1.5μs for the MAX162, MX7572XX05 and MX7572XX12 respectively.

To achieve the maximum sampling rate, the MAX162/MX7572 data must be read within the time allowed for the sample-and-hold to acquire a new input voltage.

MX7572 Figure 15 shows an AD585 sample-and-hold to MX7572 interface. The MX7572 RD input and BUSY output are used to put the AD585 in hold mode when a conversion is in progress. In this example the analog input range is $\pm$2.5V but other voltage ranges can be configured differently as explained later.

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock allowing for a 3μs sample-and-hold acquisition time.

Although this circuit works quite well for the 1MHz clock rate, at the 2.5MHz clock rate a faster sample-and-hold amplifier such as the HA-5320 is recommended.

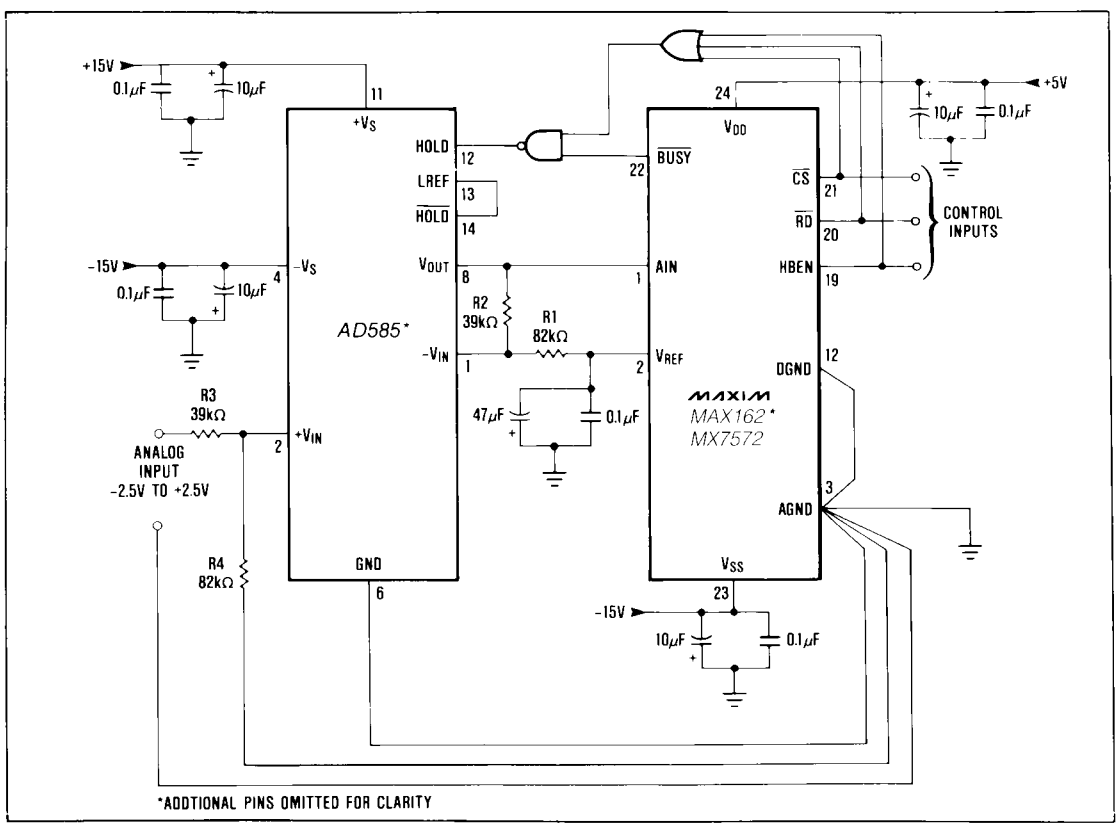


Figure 15. MX7572—AD585 Sample-and-Hold Interface

Complete High-Speed CMOS 12-Bit ADC

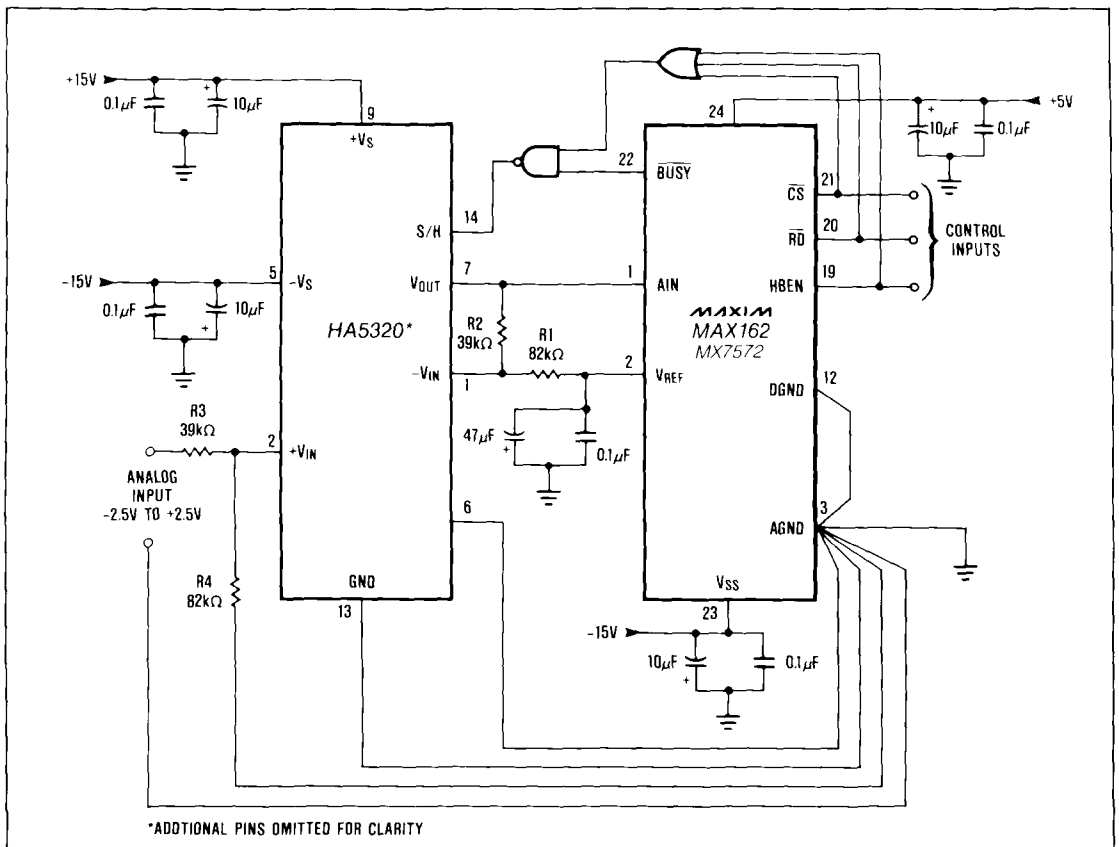


Figure 16. MAX162/MX7572—HA5320 Sample-and-Hold Interface

MAX162 Figure 16 shows the MAX162 to HA5320 interface. The maximum sampling rate is 210kHz with a 4MHz clock which allows for a 1.5μs acquisition time. The HA5320 can also be replaced by a HA5330 for higher throughput.

Unipolar Input Operation

Figure 17 shows the nominal input/output transfer function of the MAX162/MX7572 Code transitions occur half way between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 18. Note that the amplifier shown could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS-3/2LSB (4.99817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 5 and 6.

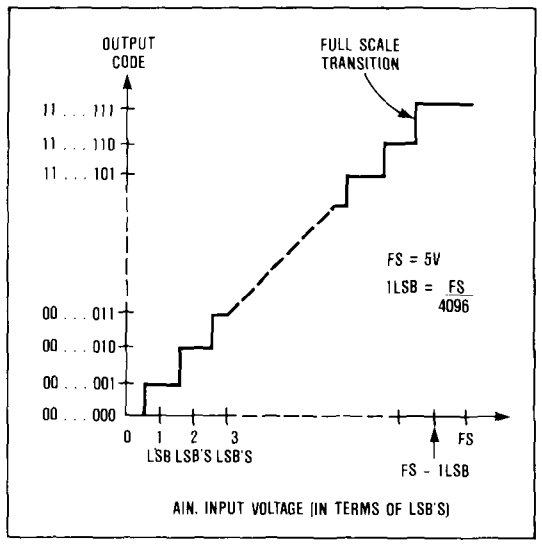


Figure 17. MAX162/MX7572 Transfer Function

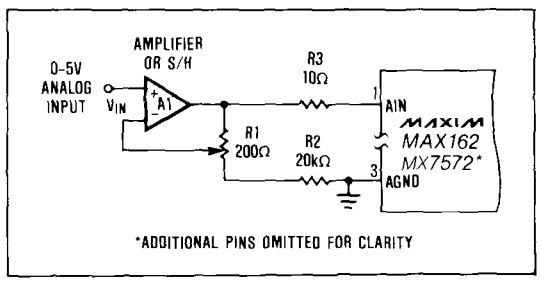


Figure 18. Full-Scale Adjustment

Figure 19 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 20 shows the ideal transfer function for this mode.

Figure 21 shows the bipolar operation in the inverting mode, where the output coding is complementary offset binary. Figure 20 shows the ideal transfer function for the circuit in Figure 21.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drifts. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

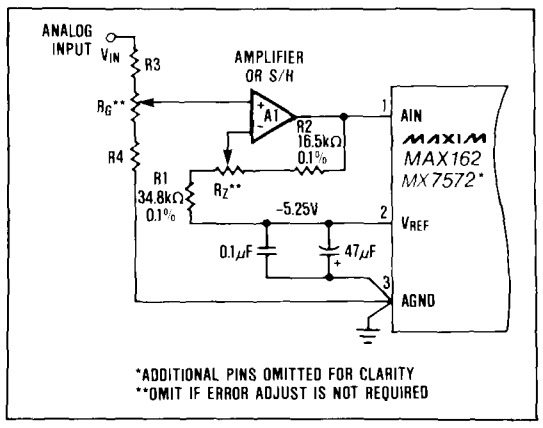


Figure 19. MAX162/MX7572 Non-inverting Bipolar Operation

Table 5. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 19

V_{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

Notes:
* R3 and R4 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

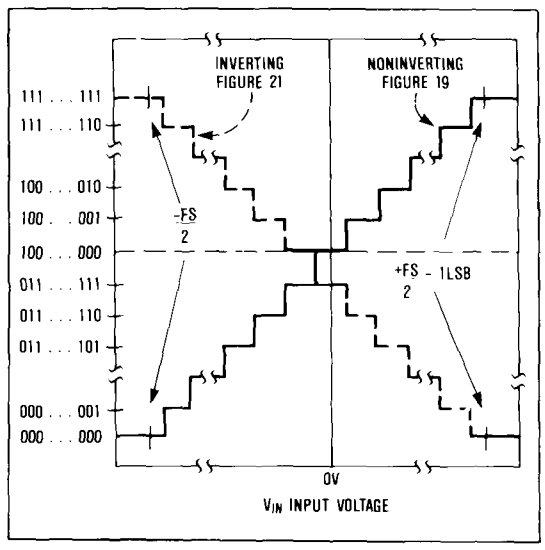


Figure 20. Ideal Input/Output Transfer Characteristic for the Bipolar circuits in Figures 19 and 21.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply +1/2LSB to the analog input (see tables 5 and 6) and adjust R_Z until the output code flickers between the following codes:

For Non-inverting (Figure 19)	1000 0000 0000 1000 0000 0001
For inverting (Figure 21)	0111 1111 1111 0111 1111 1110

Apply FS-3/2LSB (see tables 5 and 6) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-inverting (Figure 19)	1111 1111 1110 1111 1111 1111
For inverting (Figure 21)	0000 0000 0001 0000 0000 0000

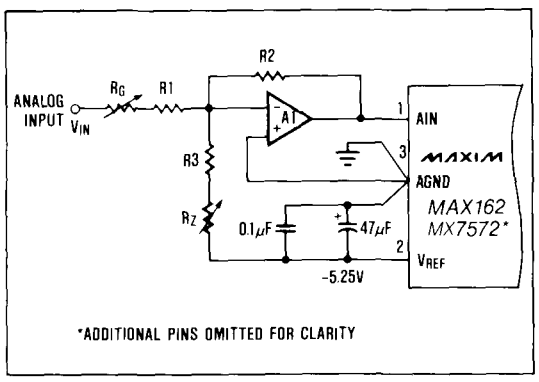


Figure 21. MAX162/MX7572 Inverting Bipolar Operation

Chip Topography

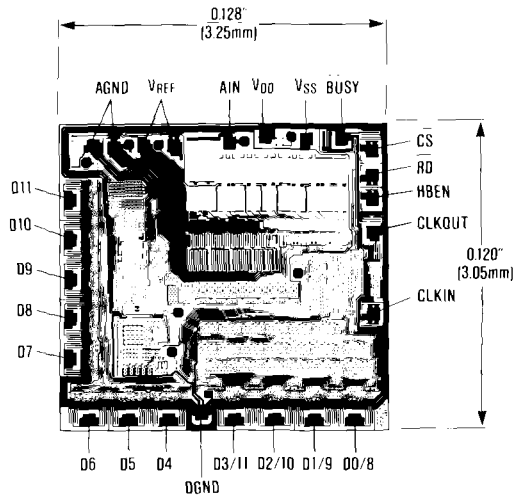


Table 6. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 21

V_{IN} Range (Volts)	R1* (kΩ)	R2* (kΩ)	R3* (kΩ)	R_Z (Ω)	R_G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	20	20.5	42.2	2000	1000	0.61	2.49817
±5.0	20	10.2	21	1000	1000	1.22	4.99634
±10.0	20	5.11	10.5	500	1000	2.44	9.99268

Notes:
* R1, R2, and R3 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
5μs CONVERSION TIME			
MX7572JN05	0°C to +70°C	Plastic DIP	±1 LSB
MX7572KN05	0°C to +70°C	Plastic DIP	±1 LSB
MX7572LN05	0°C to +70°C	Plastic DIP	±½ LSB
MX7572JCWG05	0°C to +70°C	Wide S.O.	±1 LSB
MX7572KCWG05	0°C to +70°C	Wide S.O.	±1 LSB
MX7572LCWG05	0°C to +70°C	Wide S.O.	±½ LSB
MX7572AQ05	-25°C to +85°C	CERDIP	±1 LSB
MX7572BQ05	-25°C to +85°C	CERDIP	+1 LSB
MX7572CQ05	-25°C to +85°C	CERDIP	±½ LSB
MX7572SQ05	-55°C to +125°C	CERDIP	±1 LSB
MX7572TQ05	-55°C to +125°C	CERDIP	±1 LSB
MX7572UQ05	-55°C to +125°C	CERDIP	+½ LSB
12μs CONVERSION TIME			
MX7572JN12	0°C to +70°C	Plastic DIP	±1 LSB
MX7572KN12	0°C to +70°C	Plastic DIP	+1 LSB
MX7572LN12	0°C to +70°C	Plastic DIP	±½ LSB
MX7572JCWG12	0°C to +70°C	Wide S.O.	±1 LSB
MX7572KCWG12	0°C to +70°C	Wide S.O.	+1 LSB
MX7572LCWG12	0°C to +70°C	Wide S.O.	+½ LSB
MX7572AQ12	-25°C to +85°C	CERDIP	±1 LSB
MX7572BQ12	-25°C to +85°C	CERDIP	±1 LSB
MX7572CQ12	-25°C to +85°C	CERDIP	±½ LSB
MX7572SQ12	-55°C to +125°C	CERDIP	±1 LSB
MX7572TQ12	-55°C to +125°C	CERDIP	±1 LSB
MX7572UQ12	-55°C to +125°C	CERDIP	±½ LSB

* *All devices — 24 lead packages*