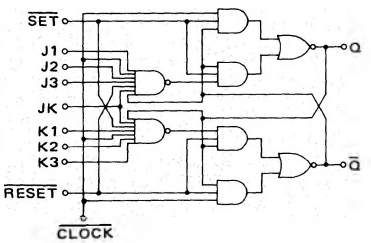
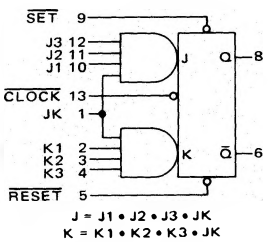
MC3151F • MC3051F
MC3151L • MC3051L,P

This J-K flip-flop triggers on the negative edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and a K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct $\overline{SET}$ and $\overline{RESET}$ are provided to permit presetting data, such as initial conditions into the flip-flop. The direct $\overline{SET}$ and $\overline{RESET}$ fully override the clock; i.e., the direct $\overline{SET}$ and $\overline{RESET}$ control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at the J and K inputs any time in a clock cycle, except during the interval of time between the Set-up and Hold times. The inputs are inhibited when the clock is low, data is entered into the input steering section of the flip-flop when the clock goes high. The input steering section of the flip-flop continually reflects the input state when the clock is high. Data present during the time interval between the Set-up and Hold times is transferred to the bistable section on the negative edge of the clock and the outputs Q and $\bar{Q}$ respond accordingly. The flip-flop can be set or reset directly by applying the low state to the $\overline{SET}$ or $\overline{RESET}$ inputs.

LOGIC DIAGRAM





$J = J1 \bullet J2 \bullet J3 \bullet JK$

$K = K1 \bullet K2 \bullet K3 \bullet JK$

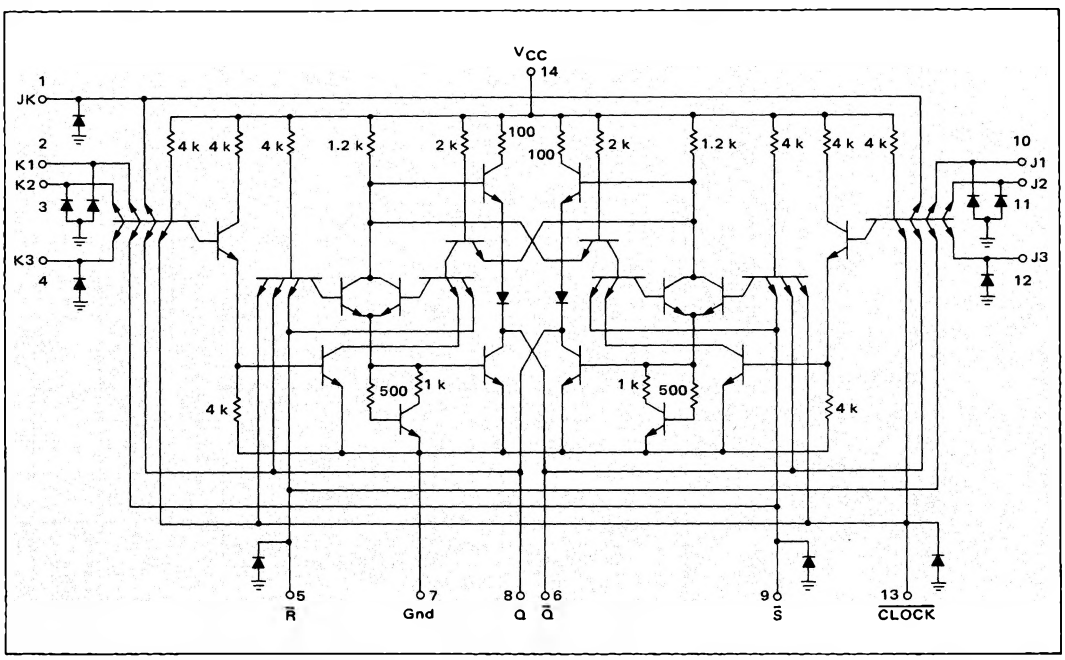
TRUTH TABLE

J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Input Loading Factors:
- J, K = 0.75
- JK = 1.5
- $\overline{Set}$, $\overline{Reset}$ = 2.0
- $\overline{Clock}$ = 2.3

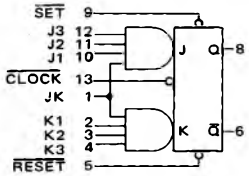
Output Loading Factor = 10

Typical Characteristics (V_{CC} = 5.0 V, T_A = 25°C
- Total Power Dissipation = 50 mW/pkg
- Toggle Frequency = 50 MHz
- Logical "1" Setup Time = 8.0 ns
- Logical "0" Setup Time = 8.0 ns
- Logical "1" and "0" Hold Time = 5.0 ns
- t_{pd-} = 12 ns
- t_{pd+} = 14 ns



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS



@ Test Temperature		TEST CURRENT/VOLTAGE VALUES													
		mAdc				Volts									
		I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_{IL}	V_{IH}	V_R	V_{RH}	V_{CCL}	V_{CCH}	V_{CC}	V_{max}	
MC3151	−55°C	20.0	-2.0	-	-	0.4	1.1	2.0	2.4	4.0	4.5	5.5	5.0	-	
	+25°C	20.0	-2.0	1.0	-10	0.4	1.1	1.8	2.4	4.0	4.5	5.5	5.0	7.0	
	+125°C	20.0	-2.0	-	-	0.4	0.8	1.8	2.4	4.0	4.5	5.5	5.0	-	
MC3051	0°C	20.0	-2.0	-	-	0.4	1.1	2.0	2.5	4.0	4.75	5.25	5.0	-	
	+25°C	20.0	-2.0	1.0	-10	0.4	1.1	1.8	2.5	4.0	4.75	5.25	5.0	7.0	
	+75°C	20.0	-2.0	-	-	0.4	0.9	1.8	2.5	4.0	4.75	5.25	5.0	-	

Characteristic	Symbol	Pin Under Test	MC3151 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC3051 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{in}	I_D	V_F	V_{IL}	V_{IH}	V_R	V_{RH}	V_{CCL}	V_{CCH}	V_{CC}	V_{max}	*	Gnd
Input																													
Forward Current	I_F																												
K		2	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	mAdc	-	-	-	-	2	-	-	-	1,3,4,5,9,13	-	14	-	-	9	7
J		10	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5	-	-1.5		-	-	-	-	10	-	-	-	1,5,9,11,12,13	-		-	-	5	
JK		1	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0		-	-	-	-	1	-	-	-	2,3,4,5,9,10,11,12,13	-		-	-	9	
JK		1	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0	-	-3.0		-	-	-	-	1	-	-	-	2,3,4,5,9,10,11,12,13	-		-	-	5	
$\overline{\text{Set}}$		9	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0		-	-	-	-	9	-	-	-	1,2,3,4,5,10,11,12,13	-		-	-	-	
$\overline{\text{Reset}}$		5	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0	-	-4.0		-	-	-	-	5	-	-	-	1,2,3,4,10,11,12,13	-		-	-	-	
Clock		13	-	-4.6	-	-4.6	-	-4.6	-	-4.6	-	-4.6	-	-4.6		-	-	-	-	13	-	-	-	1,2,3,4,5,9,10,11,12	-		-	-	5	
Clock		13	-	-4.6	-	-4.6	-	-4.6	-	-4.6	-	-4.6	-	-4.6		-	-	-	-	13	-	-	-	1,2,3,4,5,9,10,11,12	-		-	-	9	
Reverse Current	I_R																												
K		2	-	50	-	50	-	50	-	50	-	50	-	50	μAdc	-	-	-	-	-	-	-	2	9	-	14	-	-	-	1,3,4,5,7,13
J		10	-	50	-	50	-	50	-	50	-	50	-	50		-	-	-	-	-	-	-	10	5	-		-	-	-	1,7,9,11,12,13
JK		1	-	100	-	100	-	100	-	100	-	100	-	100		-	-	-	-	-	-	-	1	-	-		-	-	-	2,3,4,5,7,9,10,11,12,13
$\overline{\text{Set}}$		9	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	-	-	-	9	-	-		-	-	-	1,2,3,4,7,13
$\overline{\text{Reset}}$		5	-	140	-	140	-	140	-	140	-	140	-	140		-	-	-	-	-	-	-	5	-	-		-	-	-	1,7,10,11,12,13
Clock		13	-	145	-	145	-	145	-	145	-	145	-	145		-	-	-	-	-	-	-	13	-	-		-	-	-	1,2,3,4,5,7,9,10,11,12
Breakdown Voltage	BV_{in}																												
K		2	-	-	5.5	-	-	-	-	-	5.5	-	-	-	Vdc	-	-	2	-	-	-	-	-	9	-	14	-	-	-	1,3,4,5,7,9,13
J		10	-	-		-	-	-	-	-		-	-	-		-	-	10	-	-	-	-	-	5	-		-	-	-	1,5,7,11,12,13
JK		1	-	-		-	-	-	-	-		-	-	-		-	-	-	-	-	-	-	-	-	-		-	-	-	2,3,4,5,7,9,10,11,12,13
$\overline{\text{Set}}$		9	-	-		-	-	-	-	-		-	-	-		-	-	-	-	-	-	-	-	5	-		-	-	5	1,2,3,4,7,10,11,12,13
$\overline{\text{Reset}}$		5	-	-		-	-	-	-	-		-	-	-		-	-	-	-	-	-	-	-	9	-		-	-	9	1,2,3,4,7,10,11,12,13
Clock		13	-	-		-	-	-	-	-		-	-	-		-	-	-	-	-	-	-	-	-	-		-	-	-	1,2,3,4,5,7,9,10,11,12
Clamp Voltage	V_D																												
K		2	-	-	-	-1.5	-	-	-	-	-	-1.5	-	-	Vdc	-	-	-	2	-	-	-	-	-	14	-	-	-	-	7
J		10	-	-	-		-	-	-	-	-		-	-		-	-	-	10	-	-	-	-	-		-	-	-	-	
JK		1	-	-	-		-	-	-	-	-		-	-		-	-	-	1	-	-	-	-	-		-	-	-	-	
$\overline{\text{Set}}$		9	-	-	-		-	-	-	-	-		-	-		-	-	-	9	-	-	-	-	-		-	-	-	-	
$\overline{\text{Reset}}$		5	-	-	-		-	-	-	-	-		-	-		-	-	-	5	-	-	-	-	-		-	-	-	-	
Clock		13	-	-	-		-	-	-	-	-		-	-		-	-	-	13	-	-	-	-	-		-	-	-	-	
Output																													
Output Voltage	V_{OL}	6	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	Vdc	6	-	-	-	-	9	5	-	-	14	-	-	-	9	7,13
		8	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4		8	-	-	-	-	5	9	-	-	14	-	-	-	5	7,13
	V_{OH}	6	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	6	-	-	-	5	9	-	-	14	-	-	-	5	7,13
		8	2.4	-	2.4	-	2.4	-	2.5	-	2.5	-	2.5	-	Vdc	-	8	-	-	-	9	5	-	-	14	-	-	-	9	7,13
Short Circuit Current	I_{SC}	6	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	9	-	14	-	-	-	5,6,7
		8	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc	-	-	-	-	-	-	-	-	5	-	14	-	-	-	7,8,9
Power Requirements (Total Device) Maximum Power Current	I_{max}	14	-	-	-	21	-	-	-	-	-	21	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	-	14	-	1,7,9,13
Power Supply Drain	I_{PD}	14	-	16	-	16	-	16	-	16	-	16	-	16	mAdc	-	-	-	-	-	-	-	-	-	-	14	-	-	-	1,7,9,13

*Momentary ground before making measurement. If pin number appears in other column, it should be returned to voltage.

OPERATING CHARACTERISTICS

High state data must be present 12 ns prior to the fall of the clock and remain 5.0 ns after the clock signal rises.

Negative edge triggering: When the clock goes from the high state to the low state, the information in the input steering section is transferred to the bistable section.

The direct $\overline{SET}$ and $\overline{RESET}$ inputs may be used any time, regardless of the state of the clock. If these inputs are not used THEY MUST BE TIED to a voltage between 2.0 and 5.5 Vdc.

Unused Inputs:

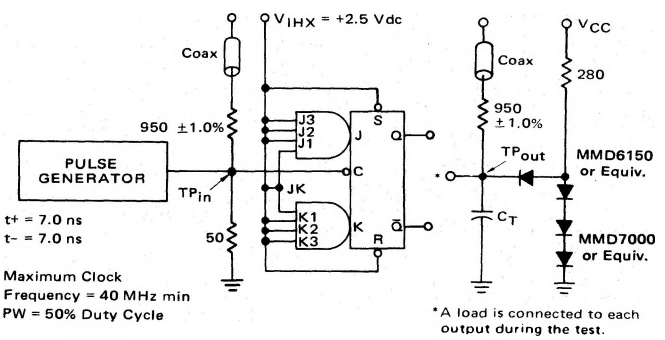
JK input MUST be in the high state to enable the clocked inputs. When the JK input is not used, it should be tied to a voltage between 2.0 and 5.5 Vdc.

Unused J inputs should be tied to used J inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused K inputs should be tied to used K inputs, the used JK input, Q, or a voltage between 2.0 and 5.5 Vdc.

Unused $\overline{SET}$ and $\overline{RESET}$ inputs MUST be tied to a voltage between 2.0 and 5.5 Vdc.

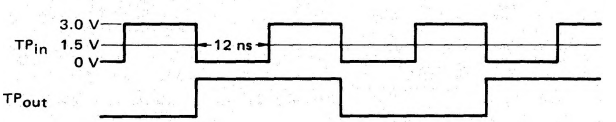
FIGURE 1 – MAXIMUM CLOCK FREQUENCY TEST CIRCUIT



C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

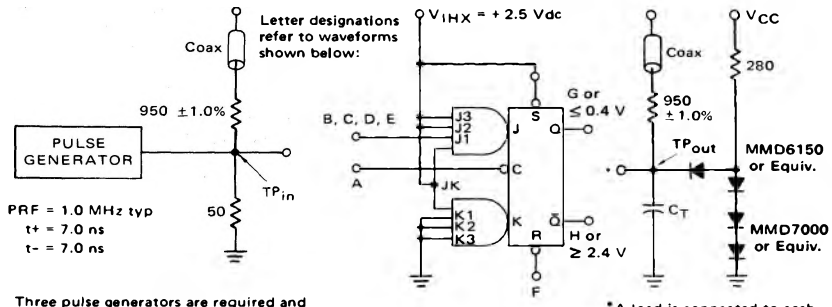
WAVEFORMS AND DEFINITIONS



OPERATING CHARACTERISTICS (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

(For J inputs and RESET input; to test other inputs, refer to Test Procedures Chart)



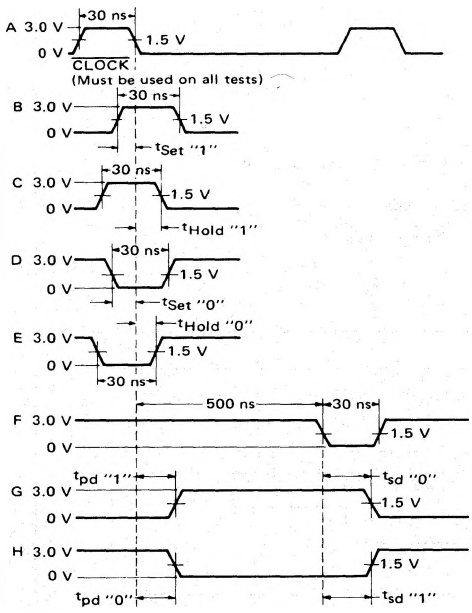
Three pulse generators are required and must be slaved together to provide the waveforms shown.

*A load is connected to each output during the test.

C_T = 25 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

VOLTAGE WAVEFORMS AND DEFINITIONS



TEST PROCEDURES CHART

TEST	INPUT						LIMITS (ns	
	J**	$\overline{SET}$**	$\overline{RESET}$**	K**	Q**	Q̄**	Min	Max
t_{Set} "1" J	B	2.4 V	F	Gnd	G	H	–	12
t_{Hold} "1" J	C	2.4 V	F	Gnd	G	H	–	0
t_{Set} "0" J	D	2.4 V	F	Gnd	≤0.4 V	≥2.4 V	–	12
t_{Hold} "0" J	E	2.4 V	F	Gnd	≤0.4 V	≥2.4 V	–	0
t_{Set} "1" K	Gnd	F	2.4 V	B	H	G	–	12
t_{Hold} "1" K	Gnd	F	2.4 V	C	H	G	–	0
t_{Set} "0" K	Gnd	F	2.4 V	D	≥2.4 V	≤0.4 V	–	12
t_{Hold} "0" K	Gnd	F	2.4 V	E	≥2.4 V	≤0.4 V	–	0
t_{pd} "1"	Delay from $\overline{CLOCK}$ to Q during t_{Set} "1" J test. Delay from $\overline{CLOCK}$ to Q̄ during t_{Set} "1" K test.							18
t_{pd} "0"	Delay from $\overline{CLOCK}$ to Q̄ during t_{Set} "1" J test. Delay from $\overline{CLOCK}$ to Q during t_{Set} "1" K test.							18
t_{sd} "1"	Delay from $\overline{SET}$ to Q during t_{Set} "1" K test. Delay from $\overline{RESET}$ to Q̄ during t_{Set} "1" J test.							18
t_{sd} "0"	Delay from $\overline{SET}$ to Q̄ during t_{Set} "1" K test. Delay from $\overline{RESET}$ to Q during t_{Set} "1" J test.							18

**Letters shown in these columns refer to waveforms at the left.