NXP Semiconductors User's Guide

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Hardware Development Guide for the MIMXRT1050/MIMXRT1060 Processor

1. Introduction

This document's purpose is to help hardware engineers design and test their MIMXRT1050/MIMXRT1060 processor-based designs. It provides information about board layout recommendations and design checklists to ensure first-pass success and avoidance of board bring-up problems. At the same time, as MIMXRT1060 is pin-to-pin compatible with MIMXRT1050, thus IMXRT1050-EVKB shared the same design with MIMXRT1060-EVK, and all the following hardware design guide for MIMXRT1050 is applicable to MIMXRT1060 too. This guide is released along with the relevant device-specific hardware documentation such as data sheets, reference manuals, and application notes available on <u>mxp.com</u>.

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2. Background

The MIMXRT1050/MIMXRT1060 processors are NXP's latest additions to a growing family of realtime processing products, offering high-performance processing optimized for lowest power consumption and best real-time response. The MIMXRT1050/MIMXRT1060 processors feature NXP's advanced implementation of the Arm[®] Cortex[®]-M7 core which operates at speeds of up to 600 MHz. The MIMXRT1050/MIMXRT1060 processors are specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor control
- Home appliances

3. Power supply

See Table 1 for the power domains and power supply decoupling recommendations. Note that the power control diagram is applicable to MIMXRT1050 A1 silicon.

Power rail	MIN (V)	TYP (V)	MAX (V)	Description	
VDD_SOC_IN	0.925	—	1.3	Power for the core supply	
VDD_HIGH_IN	2.8	3.3	3.6	VDD_HIGH_IN supply voltage	
DCDC_IN	2.8 ¹	2.9 ¹	3.3 ¹	Power for the DCDC	
VDD_SNVS_IN	2.4	3	3.6	Power for the SNVS and RTC	
USB_OTG1_VBUS USB_OTG2_VBUS	4.4	5	5.5	Power for the USB VBUS	
VDDA_ADC	3	3.3	3.6	Power for the 12-bit ADC	
VDDA_IN	3	3.3	3.6	Power for the 12-bit ADC	
	2	2.2	3.6	Power for the GPIO in the SDIO1 bank (3.3 V	
	3	3.3		mode)	
NVCC_3D0	1.65	1.8	1.95	Power for the GPIO in the SDIO1 bank (1.8 V	
		1.0		mode)	
	2	2.2	3.6	Power for the GPIO in the SDIO2 bank (3.3 V	
	3	3.3		mode)	
	4.05	1.8	1.95	Power for the GPIO in the SDIO2 bank (1.8 V	
	1.65			mode)	
	•		0.0	IO supply for the GPIO in the EMC bank (3.3 V	
NVCC_EMC		3.3	3.6	mode)	
		1.0	4.05	IO supply for the GPIO in the EMC bank (1.8 V	
	1.65	1.8	1.95	mode)	
	~		0.0		
NVCC_GPIO	3	3.3	3.6	IO power for the GPIO	

Table 1. Power domains

 For A0 silicon, the DCDC_IN voltage domain is 2.8 V ~ 3.0 V, while for A1 silicon and the later DCDC_IN, the voltage domain is 2.8 V~3.6 V.

Power rail	Decoupling and bulk capacitors (min qty)	Description
VDD_SOC_IN	$5 \times 0.22 \ \mu F^2 + 1 \times 4.7 \ \mu F^1 + 1 \times 22 \ \mu F^3$	Place at least one 4.7 μ F capacitor and three 0.22 μ F capacitors next to balls F6, F7, F8, and so on.
VDD_HIGH_IN	1 × 0.22 μF² + 1 × 4.7 μF¹	—
VDD_HIGH_CAP	1 × 0.22 μF² + 1 × 4.7 μF¹	VDDHIGH_CAP is restricted to the MX6RT loads.
DCDC_IN	$3 \times 0.22 \ \mu F^2 + 1 \times 4.7 \ \mu F^1 + 1 \times 22 \ \mu F^3$	Place at least one 4.7 μ F capacitor and one 0.22 μ F capacitor next to ball M1.
VDD_SNVS_IN	1 × 0.22 μF²	_
VDD_SNVS_CAP	1 × 0.22 μF² + 1 × 4.7 μF¹	Select a small capacitor with a low ESR. Do not connect any loads to VDD_SNVS_CAP.
USB_OTG1_VBUS USB_OTG2_VBUS	1 × 1 μF ¹	10-V rated.
VDDA_ADC_3P3	1 × 0.22 μF² + 1 × 1 μF¹	Place the buck and bypass capacitors next to ball N14.
NVCC_SD0	1 × 0.1 μF + 1 × 4.7 μF ¹	Place the buck and bypass capacitors next to ball J6.
NVCC_SD1	1 × 0.1 μF + 1 × 4.7 μF ¹	Place the buck and bypass capacitors next to ball K5.
NVCC_EMC	2 × 0.1 μF + 1 × 4.7 μF ¹	Place the buck and bypass capacitors next to balls F5 and E6.
NVCC_GPIO	3 × 0.1 μF + 1 × 4.7 μF ¹	_

Table 2. Power supply decoupling recommendations

1. For the 4.7- μ F capacitors, use the 0402 package.

2. For the $0.22 - \mu F$ capacitors, use the 0402 package.

3. For the 22-µF capacitors, the 0603 package is preferred; the 0805 and 1206 packages are acceptable.

ltem	Recommendation	Description
1. Power sequence	Comply with the power-up/power-down sequence guidelines (as described in the data sheet) to guarantee a reliable operation of the device.	Any deviation from these sequences may result in these situations: • Excessive current during the power-up phase • Prevention of the device from booting • Irreversible damage to the processor (worst-case scenario)
2. SNVS domain signals	Do not overload the coin cell backup power rail VDD_SNVS_IN. Note that these I/Os are associated with VDD_SNVS_IN (most inputs have on-chip pull resistors and do not require external resistors): • PMIC_STBY_REQ—configurable output • PMIC_ON_REQ—push-pull output • TEST_MODE—on-chip pulldown • WAKEUP—the GPIO that wakes the SoC up in the SNVS mode	Concerning i.MX RT1050: • When VDD_SNVS_IN = VDD_HIGH_IN in the SNVS domain, the current is drawn from both equally. • When VDD_HIGH_IN > VDD_SNVS_IN, VDD_HIGH_IN supplies all the SNVS domain current and the current flows into VDD_SNVS_IN to charge the coin cell battery. • When VDD_SNVS_IN > VDD_HIGH_IN, VDD_SNVS_IN supplies current to SNVS, and a small leakage current flows into VDD_HIGH_IN.
3. Power ripple	Maximum ripple voltage limitation.	The common limitation for the ripple noise shall be less than 5 % Vp-p of the supply voltage average value. The related power rails affected are VDD_xxx_IN and VDD_xxx_CAP. Note that for DCDC_IN, the ripple is within 1 % for A0 silicon.
4. VDD_SNVS_IN and VDD_HIGH_IN	If VDD_SNVS_IN is directly supplied by a coin cell battery, a schottky diode is required between VDD_HIGH_IN and VDD_SNVS_IN. The cathode is connected to VDD_SNVS_IN. Alternately, VDD_HIGH_IN and VDD_SNVS_IN can be tied together if the real-time clock function is not needed during the system power-down.	When no power is supplied to VDD_VSNVS_IN, the diode limits the voltage difference between the two on-chip SNVS power domains to approximately 0.3 V. The processor allows the current to flow between the two SNVS power domains, proportionally to the voltage difference.

 Table 3.
 Power sequence and recommendations

- Power Up Sequence Requirement
 - VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply
 - If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on
 - When internal DCDC is enabled, external delay circuit is required to delay the "DCDC_PSWITCH" signal 1 ms after DCDC_IN is stable
 - POR_B should be held low during the entire power up sequence
- Power Down Sequence Requirement
 - VDD_SNVS_IN supply must be turned off after any other power supply or be connected (shorted) with VDD_HIGH_IN supply
 - If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after any other supply is switched off

Power supply



Figure 1. Power up and power down sequence

- For IMXRT1050-EVKB, see Figure 2.
 - Firstly, it powers up SNVS.
 - PMIC_REQ_ON is then switched on to enable the external DC/DC to power up other power domains.
 - DCDC_PSWITCH is delayed more than 1ms to switch the internal DCDC on.
 - DCDC_OUT output to power the VDD_SOC_IN.
 - The ON/OFF button is used to switch PMIC_REQ_ON on/off to control power modes.
 - The RESET button and the WDOG output are used to reset the system power.

NOTE

For silicon A0 silicon, you need power SNVS domain together with DCDC_IN by 2.8 V ~ 3.0 V, otherwise the on-chip DCDC module does not work properly.

Power supply



Figure 2. Power control diagram

• About on chip DC/DC module

The internal DC/DC switching frequency is about 1.5MHz, DC/DC in working condition need to have external inductor and capacitors, the illustration is as below Figure 3, please pay attention to below items:

- The recommended value for the external inductor is about 4.7u~10uH, saturation current >1A, ESR < 0.20hm;
- The external buck capacitor value together is about 33uF, this includes all the capacitors used on DCDC_OUT and VDD_SOC_IN;
- DCDC_PSWITCH should delay 1ms with respect to DCDC_IN 1ms, this purpose is to wait DCDC_IN stable until DC/DC startup;
- If you want to bypass internal DC/DC, you still need to power DCDC_IN and ground the DCDC_PSWITCH, at the same time keep the DCDC_LP floating;
- Try to keep the DC/DC current loop as small as possible to avoid EMI issues;





Figure 3. DC/DC function diagram

4. Clocks

See Table 4 for the clock configuration. The 32.768-kHz and 24-MHz oscillators are used for the EVK design.

Signal name	Recommended connections	Description
1 RTC, XTAI I/RTC, XTAI O	i. MX 6 Series Processor Oscillation Amplifier Sensing Amplifier Solder bump RTC_XTALL For the precision 32.768-kHz oscillator, connect a crystal between RTC_XTALI and RTC_XTALO. Choose a crystal with a maximum ESR (Equivalent Series Resistance) of 100 k and follow the manufacturer's recommendation for the loading capacitance. Do not use an external biasing resistor because the bias circuit is on the chin	To hit the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitics. The integrated oscillation amplifier is self-biasing, but relatively weak. Care must be taken to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (>100 M). This de-biases the amplifier and reduces the start-up margin.
	For the external kHz source (if feeding an external clock into the device), RTC_XTALI can be driven DC-coupled with RTC_XTALO floating or driven by a complimentary signal.	If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_SNVS_CAP level and the frequency shall be <100 kHz under the typical conditions.
	An on-chip loose-tolerance ring oscillator of approximately 40 kHz is available. If RTC_XTALI is tied to GND and RTC_XTALO is floating, the on-chip oscillator is engaged automatically.	When a high-accuracy real-time clock is not required, the system may use the on-chip 40-kHz oscillator. The tolerance is ±50 %. The ring oscillator starts faster than the external crystal and is used until the external crystal reaches a stable oscillation. The ring oscillator also starts automatically if no clock is detected at RTC_XTALI at any time.
2. XTALI/XTALO	For the precision 24-MHz oscillator, connect a fundamental-mode crystal between XTALI and XTALO. An typical 80 ESR crystal rated for a maximum drive level of 250 μ W is acceptable. Alternately, a typical 50 ESR crystal rated for a maximum drive level of 200 μ W may be used.	The SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24-MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI must be mounted with a typical load capacitor. The logic level of this forcing clock must not exceed the NVCC_PLL level.

Table 4. Clocks' configurations

Debugging and programming

Signal name	Recommended connections	Description
		If this clock is used as a reference for the USB, then there are strict frequency tolerance and jitter requirements. See the OSC24M chapter and the relevant interface specifications chapters for details.
	Bias XTALI with a 2.2-M resistor to GND. Mount the resistor close to the XTALI ball.	The XTALI bias must be adjusted externally to ensure a reasonable start-up time.
3.CCM_CLK1_P/ CCM_CLK1_N	One general-purpose differential high-speed clock input/output (LVDS I/O) is provided. It can be used: • To feed the external reference clock to the PLLs and further to the modules inside the SoC. • To output the internal SoC clock to be used outside the SoC as either a reference clock or a functional clock for the peripherals.	See the <i>i.MX RT1050 Reference</i> <i>Manual</i> for details about the respective clock trees. Alternatively, use a single-ended signal to drive the CLK1_P input. In this case, the corresponding CLK1_N input must be tied to a constant voltage level equal to one half of the input signal swing. The termination must be provided in case of high-frequency signals. After the initialization, the CLK1 input/output can be disabled (if not used). If not used, either one or both CLK1_N/P pairs may remain unconnected.

Table 4.	Clocks'	configurations
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5. Debugging and programming

See Table 5 for the JTAG interface summary and recommendation. The IMXRT1050-EVKB also features an OpenSDA, which makes it easier to debug without an external debugger. At the same time, next version EVK board will change to LPC4322 based FREELINK which implement the same function as K20 based OPENSDA.

JTAG signals	I/O type	On-chip termination	External termination
JTAG_TCK	Input	47 kΩ pull-up	Not required; can use 10 k Ω pull-up
JTAG_TMS	Input	47 kΩ pull-up	Not required; can use 10 k Ω pull-up
JTAG_TDI	Input	47 kΩ pull-up	Not required; can use 10 k Ω pull-up
JTAG_TDO	3-state output	100 kΩ pull-up	Do not use pullup or pull-down
JTAG_TRSTB	Input	47 kΩ pull-up	Not required; can use 10 k Ω pull-up
JTAG_MOD	Input	100 kΩ pull-up	Use 4.7 kΩ pull-down or tie to GND

Table 5.	JTAG interfa	ace summary
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Signals	Recommendation	Description
1. JTAG_TDO	Do not add external pull-up or pull-down resistors on JTAG_TDO.	JTAG_TDO is configured with an on-chip keeper circuit, such that the floating condition is actively eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental. See Table 5 for a summary of the JTAG interface.
2. JTAG_TDO	Ensure that the on-chip pull-up/pull-down configuration is followed if external resistors are used with the JTAG signals (except for JTAG_TDO). For example, do not use an external pull-down on an input that has an on-chip pull-up.	External resistors can be used with all JTAG signals except for JTAG_TDO, but they are not required. See Table 5 for a summary of the JTAG interface.
3. JTAG_MOD	JTAG_MOD is called SJC_MOD in some documents. Both names refer to the same signal. JTAG_MOD shall be externally connected to GND for normal operation in a system. The termination to GND through an external pull-down resistor is allowed. Use a 4.7 -k Ω resistor.	When JTAG_MOD is low, the JTAG interface is configured for a common software debug, adding all the system TAPs to the chain. When JTAG_MOD is high, the JTAG interface is configured to a mode compliant with the IEEE 1149.1 standard.

Table 6. JTAG recommendation

Table 7. OpenSDA recommen

Signals	Recommendation	Description
1. SWD_DIO	Connect to the K20 signal through a buffer	The OpenSDA in the EVK board is
2. SWD_CLK	Connect to the K20 signal through a buffer	implemented as a debugger, which eliminates the cost for the users.
3.UART_TXD/UART_RXD	Connect to the K20 signal through a buffer	The UART signals connected to K20 realize a virtual COM port for the OpenSDA USB for debugging.

Table 8.	Flashloader	peripheral	l/Os
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Signals	Signals Recommendation De		
1.UART1	The Serial Downloader provides a means to download a program image to the chip over the USB and UART serial connections. In this mode, ROM programs WDOG1 for a time-out specified by the fuse WDOG Time-out Select (See the Fusemap chapter for details) if the WDOG_ENABLE eFuse is 1	The ROM code firstly polls the UART1 signals from TXD1/RXD1. Add a 10-k Ω pull up resistor to the TXD1/RXD1 pins to avoid an invalid trigger of the UART port in the serial download mode.	
2. USB1	and continuously poils for the USB and UAR I connection. If no activity is found on USB OTG1 and UART 1/2 and the watchdog timer expires, the Arm core is reset.	If there is no polling activity from UART1 in the serial download mode, the ROM code acts as an HID device for PC downloading.	

6. Boot, reset, and miscellaneous

See Table 9 for the boot, reset, and miscellaneous configurations, such as ON/OFF, TEST_MODE, NC pins, and other.

ltem	Recommendation	Description
1. BOOT_CFG[11:0]	The BOOT_CFG signals are required for a proper functionality and operation and shall not be left floating.	See the "System Boot" chapter in your chip reference manual for the correct boot configuration. Note that an incorrect setting may result in an improper boot sequence.
2. BOOT_MODE[1:0]	For BOOT_MODE1 and BOOT_MODE0, use one of these options to achieve logic 0: • Tie to GND through any-value external resistor • Tie directly to GND For logic 1, use one of these options: • Tie directly to the NVCC_GPIO_XX rail • Tie to the NVCC_GPIO_XX rail • Tie to the NVCC_GPIO_XX rail through an external 10-k Ω resistor. A value of 4.7 k Ω is preferred for high-noise environments. If a switch control is desired, no external pull-down resistors are necessary. Simply connect the SPST switches directly to the NVCC_GPIO_XX rail.	BOOT_MODE1 and BOOT_MODE0 each have on-chip pull-down devices with a nominal value of 100 k Ω , a projected minimum of 60 k Ω , and a projected maximum of 140 k Ω . When the on-chip fuses determine the boot configuration, both boot mode inputs can be disconnected.
3. BOOT_CFG and BOOT_MODE signals multiplexed with LCD signals	To reduce incorrect boot-up mode selections, do one of the following: • Use the LCD boot interface lines only as processes or outputs. Make sure that the LCD boot interface lines are not loaded down (such that the level is interpreted as low during the powerup) when the intent is to be at a high level, or the other way round. • If the LCD boot signal must be configured as an input, isolate the LCD signal from the target driving source with an analog switch and apply the logic value with a second analog switch. Alternately, the peripheral devices with 3-state outputs may be used. Ensure that the output is high-impedance.	Using the LCD boot interface lines as inputs may result in a wrong boot because of the source overcoming the pull resistor value. A peripheral device may require the LCD signal to have an external or on-chip resistor to minimize signal floating. If the usage of the LC boot signal affects the peripheral device, then an analog switch, an open collector buffer, or an equivalent shall isolate the path. A pull-up or pull-down resistor at the peripheral device may be required to maintain the desired logic level. See the switch or device data sheet for the operating specifications.

Table 9. Boot configuration

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Boot, reset, and miscellaneous



Figure 4. Boot mode setting

ltem	Recommendation	Description
1. POR_B	If the external POR_B signal is used to control the processor POR, then POR_B must be immediately asserted at the powerup and remain asserted until the VDD_HIGH_CAP and VDD_SNVS_CAP supplies are stable. VDD_SOC_IN may be applied in either order with no restrictions. In the absence of an external reset feeding the SRC_POR_B input, the internal POR module takes control.	See the "System Boot" chapter in your chip reference manual for the correct boot configuration. Note that an incorrect setting may result from an improper boot sequence. POR_B signal has internal 100K pull up to SNVS domain, should pull up to VDD_SNVS_IN if need to add external pull up resistor, otherwise it will cause additional leakage during SNVS mode.
2. ON/OFF	For portable applications, the ON/OFF input may be connected to the ON/OFF SPST push-button. The on-chip debouncing is provided, and this input has an on-chip pullup. If not used, ON/OFF can be a no-connect. A 4.7- $k\Omega$ to 10- $k\Omega$ series resistor can be used when the current drain is critical.	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF. Both boot mode inputs can be disconnected.
3. TEST_MODE	The TEST_MODE input is internally connected to an on-chip pull-down device. You may either float this signal or tie it to GND.	This input is reserved for NXP manufacturing use.
4. GPANAIO	GPANAIO must be a no-connect.	This output is reserved for NXP manufacturing use.
5. NC pin	The NC contacts are no-connect and shall float.	Depending on the feature set, some versions of ICs may have the NC contacts connected inside the BGA.

Peripheral Instance		Port (IO function)	PAD	Mode	
		LPUART1 TX	GPIO AD B0 12	ALT2	
LPUART	1	LPUART1_RX	GPIO_AD_B0_13	ALT2	
		LPSPI1_SCK	GPIO_SD_B0_00	ALT4	
	4	LPSPI1_SDO	GPIO_SD_B0_02	ALT4	
	1	LPSPI1_SDI	GPIO_SD_B0_03	ALT4	
		LPSPI1_PCS0	GPIO_SD_B0_01	ALT4	
		LPSPI2_SCK	GPIO_SD_B1_07	ALT4	
		LPSPI2_SDO	GPIO_SD_B1_08	ALT4	
	2	LPSPI2_SDI	GPIO_SD_B1_09	ALT4	
		LPSPI2_PCS0	GPIO_SD_B1_06	ALT4	
LPSPI		LPSPI3_SCK	GPIO_AD_B0_00	ALT7	
		LPSPI3_SDO	GPIO_AD_B0_01	ALT7	
	3	LPSPI3_SDI	GPIO_AD_B0_02	ALT7	
		LPSPI3_PCS0	GPIO_AD_B0_03	ALT7	
		LPSPI4_SCK	GPIO_B0_03	ALT3	
	4	LPSPI4_SDO	GPIO_B0_02	ALT3	
	4	LPSPI4_SDI	GPIO_B0_01	ALT3	
		LPSPI4_PCS0	GPIO_B0_00	ALT3	
		SEMC_DATA00	GPIO_EMC_00	ALT0	
		SEMC_DATA01	GPIO_EMC_01	ALT0	
		SEMC_DATA02	GPIO_EMC_02	ALT0	
		SEMC_DATA03	GPIO_EMC_03	ALT0	
		SEMC_DATA04	GPIO_EMC_04	ALT0	
		SEMC_DATA05	GPIO_EMC_05	ALT0	
		SEMC_DATA06	GPIO_EMC_06	ALT0	
		SEMC_DATA07	GPIO_EMC_07	ALT0	
		SEMC_DATA08	GPIO_EMC_30	ALT0	
	_	SEMC_DATA09	GPIO_EMC_31	ALT0	
SEMC NAND		SEMC_DATA10	GPIO_EMC_32	ALT0	
		SEMC_DATA11	GPIO_EMC_33	ALT0	
		SEMC_DATA12	GPIO_EMC_34	ALT0	
		SEMC_DATA13	GPIO_EMC_35	ALT0	
		SEMC_DATA14	GPIO_EMC_36	ALT0	
		SEMC_DATA15	GPIO_EMC_37	ALT0	
		SEMC_ADDR9	GPIO_EMC_18	ALT0	
		SEMC_ADDR11	GPIO_EMC_19	ALT0	
		SEMC_ADDR12	GPIO_EMC_20	ALT0	
		SEMC_BA1	GPIO_EMC_22	ALT0	
		SEMC_CSX0	GPIO_EMC_41	ALT0	
		SEMC_DATA00	GPIO_EMC_00	ALT0	
		SEMC_DATA01	GPIO_EMC_01	ALT0	
		SEMC_DATA02	GPIO_EMC_02	ALT0	
		SEMC_DATA03	GPIO_EMC_03	ALT0	
		SEMC_DATA04	GPIO_EMC_04	ALT0	
		SEMC_DATA05	GPIO_EMC_05	ALT0	
		SEMC_DATA06	GPIO_EMC_06	ALT0	
		SEMC_DATA07	GPIO_EMC_07	ALT0	
		SEMC_DATA08	GPIO_EMC_30	ALT0	
		SEMC_DATA09	GPIO_EMC_31	ALT0	
		SEMC_DATA10	GPIO_EMC_32	ALT0	
		SEMC_DATA11	GPIO_EMC_33	ALT0	
		SEMC_DATA12	GPIO_EMC_34	ALT0	
	ļ Ē	SEMC_DATA13	GPIO_EMC_35	ALTO	

Table 11.	ROM Bootloader	Peripheral PinMux
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SD SEMC DATA15 GPIO ENC 36 ALTO SEMC ADDR0 GPIO ENC 37 ALTO SEMC ADDR1 GPIO ENC 09 ALTO SEMC ADDR2 GPIO ENC 10 ALTO SEMC ADDR3 GPIO ENC 11 ALTO SEMC ADDR4 GPIO ENC 12 ALTO SEMC ADDR5 GPIO ENC 13 ALTO SEMC ADDR5 GPIO ENC 15 ALTO SEMC ADDR1 GPIO ENC 16 ALTO SEMC ADDR1 GPIO ENC 16 ALTO SEMC ADDR1 GPIO ENC 16 ALTO SEMC ADDR1 GPIO ENC 21 ALTO SEMC ADDR1 GPIO ENC 21 ALTO SEMC BAD GPIO ENC 22 ALTO SEMC CSN0 GPIO ENC 21 ALTO USDHC1 CALX GPIO SD 80 00 ALTO USDHC1 DATA GPIO SD 80 02 ALTO USDHC2 DATA3 GPIO SD 80 02 ALTO USDHC2 DATA3 GPIO SD 80 03 ALTO USDHC2 DATA4 GPIO SD 81 02 ALTO USDHC2 DATA4 <	Peripheral	Peripheral Instance		PAD	Mode
SD SEMC_DATA15 GPIO_EMC.97 ALTO SEMC_ADDR0 GPIO_EMC.09 ALTO SEMC_ADDR1 GPIO_EMC.10 ALTO SEMC_ADDR3 GPIO_EMC.11 ALTO SEMC_ADDR3 GPIO_EMC.12 ALTO SEMC_ADDR5 GPIO_EMC.13 ALTO SEMC_ADDR6 GPIO_EMC.14 ALTO SEMC_ADDR7 GPIO_EMC.16 ALTO SEMC_ADDR8 GPIO_EMC.16 ALTO SEMC_ADDR1 GPIO_EMC.16 ALTO SEMC_ADDR3 GPIO_EMC.21 ALTO SEMC_ADDR3 GPIO_EMC.21 ALTO SEMC_CSX0 GPIO_EMC.21 ALTO SEMC_CSX0 GPIO_EMC.21 ALTO SEMC_CSX0 GPIO_EMC.21 ALTO USDHC1_CATA GPIO_SD_80_00 ALTO USDHC1_DATA GPIO_SD_80_01 ALTO USDHC2_DATA2 GPIO_SD_80_05 ALTO USDHC2_DATA2 GPIO_SD_81_00 ALTO USDHC2_DATA2 GPIO_SD_81_02 ALTO USDHC2_DATA4 <			SEMC_DATA14	GPIO_EMC_36	ALT0
SEMC_ADDR0 GPIO_EMC_09 ALTO SEMC_ADDR1 GPIO_EMC_10 ALTO SEMC_ADDR3 GPIO_EMC_11 ALTO SEMC_ADDR4 GPIO_EMC_13 ALTO SEMC_ADDR5 GPIO_EMC_13 ALTO SEMC_ADDR4 GPIO_EMC_15 ALTO SEMC_ADDR5 GPIO_EMC_16 ALTO SEMC_ADDR1 GPIO_EMC_12 ALTO SEMC_ADDR1 GPIO_EMC_16 ALTO SEMC_BAD GPIO_EMC_22 ALTO SEMC_BAD GPIO_EMC_22 ALTO SEMC_CSA0 GPIO_EMC_22 ALTO SEMC_CADD GPIO_SD_80_00 ALTO USDHC1_DATA GPIO_SD_80_00 ALTO USDHC1_DATA3 GPIO_SD_80_00 ALTO USDHC2_DATA3 GPIO_SD_80_06 ALTO USDHC2_DATA3 GPIO_SD_81_00 ALTO USDHC2_DATA4 GPIO_SD_81_00 ALTO USDHC2_DATA4 GPIO_SD_81_00 ALTO USDHC2_DATA4 GPIO_SD_81_00 ALTO USDHC2_DATA4 GPIO_SD_81			SEMC_DATA15	GPIO_EMC_37	ALT0
SEMC_ADDR1 GPIO_EMC_10 ALTO SEMC_ADDR2 GPIO_EMC_11 ALTO SEMC_ADDR3 GPIO_EMC_12 ALTO SEMC_ADDR5 GPIO_EMC_14 ALTO SEMC_ADDR5 GPIO_EMC_14 ALTO SEMC_ADDR3 GPIO_EMC_14 ALTO SEMC_ADDR3 GPIO_EMC_16 ALTO SEMC_ADDR4 GPIO_EMC_12 ALTO SEMC_ADDR4 GPIO_EMC_20 ALTO SEMC_ADDR1 GPIO_EMC_20 ALTO SEMC_ADDR1 GPIO_EMC_20 ALTO SEMC_CSN0 GPIO_EMC_20 ALTO SEMC_CSN0 GPIO_EMC_20 ALTO USDHC1_CMD GPIO_SD_80_00 ALTO USDHC1_DATA GPIO_SD_80_00 ALTO USDHC1_DATA GPIO_SD_80_03 ALTO USDHC2_DATA GPIO_SD_81_00 ALTO USDHC2_DATA GPIO_SD_81_00 ALTO USDHC2_DATA GPIO_SD_81_04 ALTO USDHC2_DATA GPIO_SD_81_06 ALTO USDHC2_DATA GPIO_SD_81_06 <td></td> <td></td> <td>SEMC_ADDR0</td> <td>GPIO_EMC_09</td> <td>ALT0</td>			SEMC_ADDR0	GPIO_EMC_09	ALT0
SEMC. ADDR2 GPIO. EMC. 11 ALTO SEMC. ADDR3 GPIO. EMC. 12 ALTO SEMC. ADDR5 GPIO. EMC. 13 ALTO SEMC. ADDR6 GPIO. EMC. 15 ALTO SEMC. ADDR7 GPIO. EMC. 15 ALTO SEMC. ADDR1 GPIO. EMC. 16 ALTO SEMC. ADDR1 GPIO. EMC. 16 ALTO SEMC. ADDR12 GPIO. EMC. 11 ALTO SEMC. BA1 GPIO. EMC. 21 ALTO SEMC. CSX0 GPIO. EMC. 21 ALTO SEMC. CSX0 GPIO. EMC. 21 ALTO USDHC1. DATA GPIO. SD. 80. 00 ALTO USDHC1. DATA3 GPIO. SD. 80. 01 ALTO USDHC1. DATA3 GPIO. SD. 80. 02 ALTO USDHC2. DATA3 GPIO. SD. 81. 01 ALTO USDHC2. DATA3 GPIO. SD. 81. 03 ALTO USDHC2. CML GPIO. SD. 81. 03 ALTO USDHC2. DATA4 GPIO. SD. 81. 04 ALTO USDHC2. DATA4 GPIO. SD. 81. 04 ALTO USDHC2. DATA4 GPIO. SD. 81. 04 ALTO<			SEMC_ADDR1	GPIO_EMC_10	ALT0
SD SEMC_ADDR3 GPIO_EMC_12 ALT0 SEMC_ADDR4 GPIO_EMC_13 ALT0 SEMC_ADDR5 GPIO_EMC_16 ALT0 SEMC_ADDR7 GPIO_EMC_16 ALT0 SEMC_ADDR7 GPIO_EMC_18 ALT0 SEMC_ADDR1 GPIO_EMC_20 ALT0 SEMC_BA0 GPIO_EMC_21 ALT0 SEMC_BA0 GPIO_EMC_21 ALT0 SEMC_BA0 GPIO_EMC_21 ALT0 SEMC_CSX0 GPIO_EMC_21 ALT0 SEMC_CDR1 GPIO_SD_B0_00 ALT0 USDHC1_CLM GPIO_SD_B0_01 ALT0 USDHC1_DATA GPIO_SD_B0_02 ALT0 USDHC1_DATA GPIO_SD_B0_03 ALT0 USDHC2_DATA3 GPIO_SD_B1_04 ALT0 USDHC2_DATA4 GPIO_SD_B1_04 ALT0 USDHC2_DATA4 GPIO_SD_B1_04 ALT0 USDHC2_DATA4 GPIO_SD_B1_04 ALT0 USDHC2_DATA4 GPIO_SD_B1_04 ALT0 USDHC2_DATA6 GPIO_SD_B1_04 ALT0 USDHC2_DATA6			SEMC_ADDR2	GPIO_EMC_11	ALT0
SD SEMC_ADDR4 SEMC_ADDR5 GPIO_EMC_13 GPIO_EMC_16 ALT0 ALT0 SEMC_ADDR6 GPIO_EMC_16 ALT0 SEMC_ADDR1 GPIO_EMC_19 ALT0 SEMC_ADDR11 GPIO_EMC_20 ALT0 SEMC_ADDR12 GPIO_EMC_21 ALT0 SEMC_BAD GPIO_EMC_21 ALT0 SEMC_BA1 GPIO_EMC_21 ALT0 SEMC_BA1 GPIO_EMC_21 ALT0 SEMC_BA1 GPIO_SD_B0_00 ALT0 USDHC1_CLK GPIO_SD_B0_01 ALT0 USDHC1_DATA0 GPIO_SD_B0_02 ALT0 USDHC1_DATA3 GPIO_SD_B0_04 ALT0 USDHC2_DATA3 GPIO_SD_B1_01 ALT0 USDHC2_DATA3 GPIO_SD_B1_02 ALT0 USDHC2_CATA GPIO_SD_B1_03 ALT0 USDHC2_DATA4 GPIO_SD_B1_04 ALT0 USDHC2_DATA6 GPIO_SD_B1_06 ALT0 USDHC2_DATA6 GPIO_SD_B1_06 ALT0 USDHC2_DATA6 GPIO_SD_B1_00 ALT0 USDHC2_DATA6 GPIO_SD_B1_00 ALT1			SEMC_ADDR3	GPIO_EMC_12	ALT0
SEMC_ADDRS GPIO_EMC_14 ALT0 SEMC_ADDR3 GPIO_EMC_15 ALT0 SEMC_ADDR7 GPIO_EMC_16 ALT0 SEMC_ADDR11 GPIO_EMC_20 ALT0 SEMC_BA0 GPIO_EMC_21 ALT0 SEMC_BA0 GPIO_EMC_22 ALT0 SEMC_CSN0 GPIO_EMC_22 ALT0 SEMC_CSN0 GPIO_EMC_24 ALT0 USDHC1_CLK GPIO_SD_B0_01 ALT0 USDHC1_DATA GPIO_SD_B0_02 ALT0 USDHC1_DATA GPIO_SD_B0_03 ALT0 USDHC1_DATA3 GPIO_SD_B0_03 ALT0 USDHC2_DATA3 GPIO_SD_B1_00 ALT0 USDHC2_DATA3 GPIO_SD_B1_00 ALT0 USDHC2_DATA4 GPIO_SD_B1_04 ALT0 USDHC2_DATA6 GPIO_SD_B1_06 ALT0 USDHC2_DATA6 GPIO_SD_B1_04 ALT0 USDHC2_DATA6 GPIO_SD_B1_04 ALT0 USDHC2_DATA6 GPIO_SD_B1_04 ALT0 USDHC2_DATA6 GPIO_SD_B1_04 ALT0 USDHC2_DATA6			SEMC_ADDR4	GPIO_EMC_13	ALT0
SEMC. ADDR6 GPIO_EMC_16 A.LT0 SEMC. ADDR7 GPIO_EMC_16 A.LT0 SEMC. ADDR11 GPIO_EMC_20 A.LT0 SEMC. BAD GPIO_EMC_21 A.LT0 SEMC. BA0 GPIO_EMC_22 A.LT0 SEMC. BA0 GPIO_EMC_22 A.LT0 SEMC. SSN GPIO_EMC_21 A.LT0 SEMC. SSN GPIO_EMC_22 A.LT0 SEMC. SSN GPIO_EMC_21 A.LT0 USDHC1. CLK GPIO_SD_B0.00 A.LT0 USDHC1. DATA0 GPIO_SD_B0.02 A.LT0 USDHC1. DATA1 GPIO_SD_B0.03 A.LT0 USDHC1. DATA3 GPIO_SD_B1.00 A.LT0 USDHC2.DATA2 GPIO_SD_B1.00 A.LT0 USDHC2.DATA3 GPIO_SD_B1.01 A.LT0 USDHC2.DATA4 GPIO_SD_B1.03 A.LT0 USDHC2.CLX GPIO_SD_B1.04 ALT0 USDHC2.DATA4 GPIO_SD_B1.04 ALT0 USDHC2.DATA4 GPIO_SD_B1.06 ALT0 USDHC2.DATA5 GPIO_SD_B1.06 ALT0 USDHC			SEMC_ADDR5	GPIO_EMC_14	ALT0
SEMC_ADDR1 GPIO_EMC_16 A.IT0 SEMC_ADDR11 GPIO_EMC_20 A.IT0 SEMC_BA0 GPIO_EMC_21 A.IT0 SEMC_BA1 GPIO_EMC_21 A.IT0 SEMC_BA1 GPIO_EMC_22 A.IT0 SEMC_BA1 GPIO_EMC_21 A.IT0 SEMC_BA1 GPIO_EMC_21 A.IT0 USDHC1_CLK GPIO_SD_B0.00 A.IT0 USDHC1_DATA0 GPIO_SD_B0.02 A.IT0 USDHC1_DATA1 GPIO_SD_B0.02 A.IT0 USDHC1_DATA3 GPIO_SD_B0.03 A.IT0 USDHC2_DATA3 GPIO_SD_B1.00 A.IT0 USDHC2_DATA3 GPIO_SD_B1.01 A.IT0 USDHC2_DATA2 GPIO_SD_B1.01 A.IT0 USDHC2_DATA2 GPIO_SD_B1.04 A.IT0 USDHC2_DATA4 GPIO_SD_B1.06 A.IT0 USDHC2_DATA5 GPIO_SD_B1.06 A.IT0 USDHC2_DATA6 GPIO_SD_B1.06 A.IT0 USDHC2_DATA6 GPIO_SD_B1.06 A.IT0 USDHC2_DATA5 GPIO_SD_B1.04 A.IT0 US			SEMC_ADDR6	GPIO_EMC_15	ALT0
SEMC_ADDR11 GPIQ_EMC_20 ALTO SEMC_ADDR12 GPIQ_EMC_20 ALTO SEMC_BA1 GPIQ_EMC_21 ALTO SEMC_SA1 GPIQ_EMC_21 ALTO SEMC_CSX0 GPIQ_EMC_21 ALTO SEMC_CSX0 GPIQ_EMC_21 ALTO USDHC1_CMD GPIQ_SD_80_00 ALTO USDHC1_DATA1 GPIQ_SD_80_00 ALTO USDHC1_DATA2 GPIQ_SD_80_02 ALTO USDHC1_DATA3 GPIQ_SD_80_03 ALTO USDHC2_DATA3 GPIQ_SD_80_05 ALTO USDHC2_DATA3 GPIQ_SD_81_00 ALTO USDHC2_DATA3 GPIQ_SD_81_02 ALTO USDHC2_DATA4 GPIQ_SD_81_02 ALTO USDHC2_DATA4 GPIQ_SD_81_00 ALTO USDHC2_DATA5 GPIQ_SD_81_00 ALTO USDHC2_DATA6 GPIQ_SD_81_00 ALTO USDHC2_DATA6 GPIQ_SD_81_00 ALTO USDHC2_DATA6 GPIQ_SD_81_00 ALTO USDHC2_DATA6 GPIQ_SD_81_00 ALTO USDHC2_DATA6<			SEMC_ADDR7	GPIO_EMC_16	ALT0
SEMC ADDR12 GPIO EMC 20 AL10 SEMC BA0 GPIO EMC 21 ALT0 SEMC BA1 GPIO EMC 22 ALT0 SEMC CSX0 GPIO EMC 22 ALT0 SEMC CX0 GPIO EMC 21 ALT0 USDHC1 CMD GPIO SD 80.00 ALT0 USDHC1 DATA0 GPIO SD 80.01 ALT0 USDHC1 DATA1 GPIO SD 80.02 ALT0 USDHC1 DATA2 GPIO SD 80.03 ALT0 USDHC1 DATA3 GPIO SD 80.06 ALT0 USDHC2 DATA3 GPIO SD 80.06 ALT0 USDHC2 DATA3 GPIO SD 81.00 ALT0 USDHC2 DATA1 GPIO SD 81.02 ALT0 USDHC2 DATA1 GPIO SD 81.03 ALT0 USDHC2 DATA4 GPIO SD 81.06 ALT0 USDHC2 DATA4 GPIO SD 81.06 ALT0 USDHC2 DATA4 GPIO SD 81.00 ALT0 USDHC2 DATA4 GPIO SD 81.00 ALT0 USDHC2 DATA6 GPIO SD 81.00 ALT0 USDHC2 DATA6 GPIO SD 81.00 ALT1 FLEXSPL B D			SEMC_ADDR11	GPIO_EMC_19	ALT0
Start Start GPIO EMC 21 ALTO SEMC SEMC GPIO EMC 21 ALTO SEMC SEMC GPIO EMC 24 ALTO SEMC SEMC GPIO SEMC 41 ALTO USDHC1 CM GPIO SD 00 ALTO USDHC1 DATA0 GPIO SD 80.00 ALTO USDHC1 DATA1 GPIO SD 80.02 ALTO USDHC1 DATA2 GPIO SD 80.03 ALTO USDHC2 DATA3 GPIO SD BO.05 ALTO USDHC2 DATA3 GPIO SD BI.00 ALTO USDHC2 DATA2 GPIO SD BI.04 ALTO USDHC2 DATA0 GPIO SD BI.04 ALTO USDHC2 DATA0 GPIO SD BI.06 ALTO USDHC2 DATA1 GPIO			SEMC_ADDR12	GPIO_EMC_20	ALT0
Stem C SX0 GPIO E MC 41 ALTO SEMC CSX0 GPIO SD 80.00 ALTO USDHC1_CMD GPIO SD 80.00 ALTO USDHC1_CLK GPIO SD 80.01 ALTO USDHC1_DATA0 GPIO SD 80.02 ALTO USDHC1_DATA0 GPIO SD 80.02 ALTO USDHC1_DATA0 GPIO SD 80.06 ALTO USDHC1_DATA1 GPIO SD 80.06 ALTO USDHC1_DATA3 GPIO SD 81.06 ALTO USDHC2_DATA3 GPIO SD 81.00 ALTO USDHC2_DATA2 GPIO SD 81.02 ALTO USDHC2_DATA2 GPIO SD 81.02 ALTO USDHC2_DATA2 GPIO SD 81.05 ALTO USDHC2_DATA4 GPIO SD 81.06 ALTO USDHC2_DATA6 GPIO SD 81.06 ALTO USDHC2_DATA6 GPIO SD 81.06 ALTO USDHC2_DATA6 GPIO SD 81.01 ALT1			SEMC_BA0	GPIO_EMC_21	ALT0
Image: Selection of the selection			SEMC_BA1	GPIO_EMC_22	ALTO
Image: Second			SEMC_CSX0	GPIO_EMC_41	ALTO
Image: Subscription of the second s			USDHC1_CMD	GPIO_SD_B0_00	ALTO
1 USDHC1_DATA1 USDHC1_DATA2 GPIO_SD_B0_03 OR ALTO USDHC1_DATA2 GPIO_SD_B0_03 ALTO USDHC1_DATA3 GPIO_SD_B0_04 ALTO USDHC1_DATA3 GPIO_SD_B1_00 ALTO USDHC2_DATA3 GPIO_SD_B1_00 ALTO USDHC2_DATA3 GPIO_SD_B1_02 ALTO USDHC2_DATA3 GPIO_SD_B1_02 ALTO USDHC2_DATA0 GPIO_SD_B1_03 ALTO USDHC2_DATA4 GPIO_SD_B1_06 ALTO USDHC2_CLK GPIO_SD_B1_06 ALTO USDHC2_DATA6 GPIO_SD_B1_06 ALTO USDHC2_DATA6 GPIO_SD_B1_08 ALTO USDHC2_DATA6 GPIO_SD_B1_08 ALTO USDHC2_DATA6 GPIO_SD_B1_01 ALTO USDHC2_DATA6 GPIO_SD_B1_03 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_03 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_03 ALT1 FLEXSPI_B_DATA2 GPIO_SD_B1_04 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_03 ALT1 FLEXSPI_B_SO_B GPIO_SD_			USDHC1_CLK	GPIO_SD_B0_01	ALTO
SD USDHC1_DATA2 USDHC1_DATA3 GPIO_SD_B0_04 (PIO_SD_B0_04) ALTO USDHC1_DATA3 GPIO_SD_B1_00 ALTO USDHC2_DATA3 GPIO_SD_B1_00 ALTO USDHC2_DATA2 GPIO_SD_B1_01 ALTO USDHC2_DATA2 GPIO_SD_B1_02 ALTO USDHC2_DATA1 GPIO_SD_B1_03 ALTO USDHC2_CLK GPIO_SD_B1_03 ALTO USDHC2_CLK GPIO_SD_B1_06 ALTO USDHC2_CLK GPIO_SD_B1_06 ALTO USDHC2_DATA6 GPIO_SD_B1_06 ALTO USDHC2_DATA6 GPIO_SD_B1_06 ALTO USDHC2_DATA6 GPIO_SD_B1_00 ALTO USDHC2_DATA6 GPIO_SD_B1_00 ALTO USDHC2_DATA6 GPIO_SD_B1_00 ALTO USDHC2_DATA7 GPIO_SD_B1_00 ALT1 FLEXSPLB_DATA1 GPIO_SD_B1_00 ALT1 FLEXSPLB_DATA0 GPIO_SD_B1_00 ALT1 FLEXSPLB_DATA0 GPIO_SD_B1_03 ALT1 FLEXSPLB_DATA0 GPIO_SD_B1_02 ALT1 FLEXSPLB_DATA0 GPI		1		GPIO_SD_B0_02	AL TO
SD USDHC1_DATA2 GPIO_SD_B0_05 ALT0 USDHC2_DATA3 GPIO_SD_B0_05 ALT0 USDHC2_DATA3 GPIO_SD_B1_00 ALT0 USDHC2_DATA1 GPIO_SD_B1_02 ALT0 USDHC2_DATA1 GPIO_SD_B1_02 ALT0 USDHC2_DATA1 GPIO_SD_B1_02 ALT0 USDHC2_DATA0 GPIO_SD_B1_04 ALT0 USDHC2_CKL GPIO_SD_B1_04 ALT0 USDHC2_CAX GPIO_SD_B1_06 ALT0 USDHC2_DATA4 GPIO_SD_B1_04 ALT0 USDHC2_DATA5 GPIO_SD_B1_04 ALT0 USDHC2_DATA6 GPIO_SD_B1_04 ALT0 USDHC2_DATA6 GPIO_SD_B1_04 ALT0 USDHC2_DATA5 GPIO_SD_B1_04 ALT0 USDHC2_DATA5 GPIO_SD_B1_04 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_04 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_04 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_04 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B0_04				GPIO_SD_B0_03	AL TO
SD OSDHC1_DATAS GPIO_SD_B1_003 AL10 SD USDHC2_DATAS GPIO_SD_B1_003 AL10 USDHC2_DATA2 GPIO_SD_B1_01 ALT0 USDHC2_DATA1 GPIO_SD_B1_02 ALT0 USDHC2_DATA0 GPIO_SD_B1_03 ALT0 USDHC2_CLK GPIO_SD_B1_03 ALT0 USDHC2_CLK GPIO_SD_B1_04 ALT0 USDHC2_CLK GPIO_SD_B1_05 ALT0 USDHC2_DATA4 GPIO_SD_B1_06 ALT0 USDHC2_DATA4 GPIO_SD_B1_06 ALT0 USDHC2_DATA5 GPIO_SD_B1_06 ALT0 USDHC2_DATA6 GPIO_SD_B1_01 ALT0 USDHC2_DATA6 GPIO_SD_B1_01 ALT0 USDHC2_DATA6 GPIO_SD_B1_01 ALT0 USDHC2_DATA6 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA2 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA2 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_02 ALT1 FLEXSPI_B_SOLB GPIO_SD_B0_05 ALT1 FLEXSPI_B_SOLB GPIO_S					
SD ISDHC2_DATAS GPIO_3D_B1_00 ALT0 SD USDHC2_DATA3 GPIO_SD_B1_01 ALT0 USDHC2_DATA0 GPIO_SD_B1_02 ALT0 USDHC2_CLK GPIO_SD_B1_03 ALT0 USDHC2_CLK GPIO_SD_B1_04 ALT0 USDHC2_DATA0 GPIO_SD_B1_06 ALT0 USDHC2_DATA4 GPIO_SD_B1_06 ALT0 USDHC2_DATA4 GPIO_SD_B1_08 ALT0 USDHC2_DATA6 GPIO_SD_B1_08 ALT0 USDHC2_DATA6 GPIO_SD_B1_09 ALT0 USDHC2_DATA6 GPIO_SD_B1_09 ALT0 USDHC2_DATA6 GPIO_SD_B1_01 ALT1 USDHC2_DATA5 GPIO_SD_B1_01 ALT0 USDHC2_DATA6 GPIO_SD_B1_01 ALT1 USDHC2_DATA6 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B0_05 ALT1 FLEXSPI_B_DAS1_B GPI					
SD USDHC2_DATA1 GPIO_SD_B1_01 ALT0 USDHC2_DATA1 GPIO_SD_B1_02 ALT0 USDHC2_CLK GPIO_SD_B1_03 ALT0 USDHC2_CLK GPIO_SD_B1_06 ALT0 USDHC2_CLK GPIO_SD_B1_06 ALT0 USDHC2_CLK GPIO_SD_B1_06 ALT0 USDHC2_DATA4 GPIO_SD_B1_06 ALT0 USDHC2_DATA6 GPIO_SD_B1_06 ALT0 USDHC2_DATA6 GPIO_SD_B1_06 ALT0 USDHC2_DATA6 GPIO_SD_B1_00 ALT0 USDHC2_DATA6 GPIO_SD_B1_00 ALT0 USDHC2_DATA6 GPIO_SD_B1_00 ALT1 USDHC2_DATA6 GPIO_SD_B1_00 ALT1 USDHC2_DATA6 GPIO_SD_B1_00 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_00 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DAS0 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DAS0 GPIO_SD_B1_04					
SD USDHC2_DATA0 GPIO_SD_B1_02 ALT0 USDHC2_DATA0 GPIO_SD_B1_03 ALT0 USDHC2_CLK GPIO_SD_B1_04 ALT0 USDHC2_CMD GPIO_SD_B1_06 ALT0 USDHC2_DATA4 GPIO_SD_B1_06 ALT0 USDHC2_DATA4 GPIO_SD_B1_08 ALT0 USDHC2_DATA4 GPIO_SD_B1_08 ALT0 USDHC2_DATA5 GPIO_SD_B1_08 ALT0 USDHC2_DATA6 GPIO_SD_B1_08 ALT0 USDHC2_DATA6 GPIO_SD_B1_00 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_00 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_04 ALT1 FLEXSPI_B_DAS GPIO_SD_B1_06 ALT1 FLEXSPI_A_DAS GPIO_SD_B1_06	SD		USDHC2_DATA1	GPIO_SD_B1_01	
PiexSPI 1 Observed USDHC2_CLK GPIO_SD_B1_04 ALTO 2 USDHC2_CMD GPIO_SD_B1_05 ALTO USDHC2_RESET_B GPIO_SD_B1_06 ALTO USDHC2_DATA4 GPIO_SD_B1_06 ALTO USDHC2_DATA5 GPIO_SD_B1_08 ALTO USDHC2_DATA6 GPIO_SD_B1_09 ALTO USDHC2_DATA6 GPIO_SD_B1_00 ALTO USDHC2_DATA6 GPIO_SD_B1_00 ALTO USDHC2_DATA6 GPIO_SD_B1_00 ALTO USDHC2_DATA6 GPIO_SD_B1_00 ALT1 FLEXSPI_B_DATA3 GPIO_SD_B1_00 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_03 ALT1 FLEXSPI_B_DQS GPIO_SD_B1_04 ALT1 FLEXSPI_B_SS1_B GPIO_SD_B1_04 ALT1 FLEXSPI_B_SS1_B GPIO_SD_B0_01 ALT6 FLEXSPI_A_SS0_B GPIO_SD_B1_05 ALT1 FLEXSPI_A_SS1_B GPIO_SD_B1_06 ALT1 FLEXSPI_A_DATA0 GPIO_SD_B1_06 ALT1	00			GPIO SD B1 03	
2 USDHC2_CMD GPIO_SD_B1_05 ALTO USDHC2_RESET_B GPIO_SD_B1_06 ALTO USDHC2_DATA4 GPIO_SD_B1_06 ALTO USDHC2_DATA4 GPIO_SD_B1_08 ALTO USDHC2_DATA4 GPIO_SD_B1_09 ALTO USDHC2_DATA6 GPIO_SD_B1_01 ALTO USDHC2_DATA7 GPIO_SD_B1_00 ALT1 FLEXSPI_B_DATA2 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DCK GPIO_SD_B1_04 ALT1 FLEXSPI_B_DQS GPIO_SD_B1_04 ALT1 FLEXSPI_B_DQS GPIO_SD_B1_04 ALT1 FLEXSPI_B_ADQS GPIO_SD_B1_06 ALT1 FLEXSPI_A_DQS GPIO_SD_B1_06 ALT1 FLEXSPI_A_DATA0 GPIO_SD_B1_07				GPIO_SD_B1_03	
FlexSPI 1 1 0 </td <td></td> <td>2</td> <td>USDHC2_CMD</td> <td>GPIO_SD_B1_04</td> <td></td>		2	USDHC2_CMD	GPIO_SD_B1_04	
FlexSPI 1 1 0 0 0 0 0 1 1 FlexSPI 1 <		2	USDHC2 RESET B	GPIO_SD_B1_06	
FlexSPI 1 Image: Sign of the second			USDHC2 DATA4	GPIO_SD_B1_08	AL TO
FlexSPI 1 Image: Sign of the system of the			USDHC2 DATA5	GPIO SD B1 09	ALT0
FlexSPI 1 Image: Mark and the second			USDHC2 DATA6	GPIO SD B1 10	ALT0
FlexSPI 1 FLEXSPI_B_DATA3 GPIO_SD_B1_00 ALT1 FLEXSPI_B_DATA2 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_03 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_04 ALT1 FLEXSPI_B_SO_B GPIO_SD_B0_05 ALT4 FLEXSPI_B_SS0_B GPIO_SD_B0_04 ALT4 FLEXSPI_B_SS1_B GPIO_SD_B1_06 ALT1 FLEXSPI_A_DQS GPIO_SD_B1_05 ALT1 FLEXSPI_A_SS0_B GPIO_SD_B1_06 ALT1 FLEXSPI_A_DQS GPIO_SD_B1_06 ALT1 FLEXSPI_A_DAS0_B GPIO_SD_B1_07 ALT1 FLEXSPI_A_DATA0 GPIO_SD_B1_07 ALT1 FLEXSPI_A_DATA1 GPIO_SD_B1_09 ALT1 FLEXSPI_A_DATA2 GPIO_SD_B1_10 ALT1 FLEXSPI_A_DATA2 GPIO_SD_B1_10 ALT1 FLEXSPI_A_DATA3 GPIO_SD_B1_10 ALT1 FLEXSPI_A_DATA3 GPIO_SD_B1_10 ALT1			USDHC2 DATA7	GPIO SD B1 11	ALT0
FlexSPI_B_DATA2 GPIO_SD_B1_01 ALT1 FLEXSPI_B_DATA1 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_03 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_04 ALT1 FLEXSPI_B_SCLK GPIO_SD_B0_05 ALT4 FLEXSPI_B_SO_B GPIO_SD_B0_04 ALT4 FLEXSPI_B_SS1_B GPIO_SD_B0_01 ALT6 FLEXSPI_A_DQS GPIO_SD_B1_05 ALT1 FLEXSPI_A_DQS GPIO_SD_B1_06 ALT1 FLEXSPI_A_SO_B GPIO_SD_B1_06 ALT1 FLEXSPI_A_SS1_B GPIO_SD_B1_06 ALT1 FLEXSPI_A_SS1_B GPIO_SD_B1_07 ALT1 FLEXSPI_A_DATA0 GPIO_SD_B1_07 ALT1 FLEXSPI_A_DATA1 GPIO_SD_B1_09 ALT1 FLEXSPI_A_DATA2 GPIO_SD_B1_09 ALT1 FLEXSPI_A_DATA2 GPIO_SD_B1_10 ALT1 FLEXSPI_A_DATA3 GPIO_SD_B1_00 ALT1 FLEXSPI_A_DATA3 GPIO_SD_B1_00 ALT1 FLEXSPI_A_DATA5 GPIO_SD_B1_01 ALT1 FLEXSPI_A_DATA5 GP			FLEXSPI B DATA3	GPIO_SD_B1_00	ALT1
FlexSPI 1 FLEXSPI_B_DATA1 GPIO_SD_B1_02 ALT1 FLEXSPI_B_DATA0 GPIO_SD_B1_03 ALT1 FLEXSPI_B_SCLK GPIO_SD_B1_04 ALT1 FLEXSPI_B_DQS GPIO_SD_B0_05 ALT4 FLEXSPI_B_SS0_B GPIO_SD_B0_04 ALT4 FLEXSPI_B_SS1_B GPIO_SD_B0_01 ALT6 FLEXSPI_A_DQS GPIO_SD_B1_05 ALT1 FLEXSPI_A_DQS GPIO_SD_B1_06 ALT1 FLEXSPI_A_DQS GPIO_SD_B1_06 ALT1 FLEXSPI_A_DQS GPIO_SD_B1_06 ALT1 FLEXSPI_A_DQS GPIO_SD_B1_07 ALT1 FLEXSPI_A_SS1_B GPIO_SD_B1_07 ALT1 FLEXSPI_A_DATA0 GPIO_SD_B1_09 ALT1 FLEXSPI_A_DATA1 GPIO_SD_B1_09 ALT1 FLEXSPI_A_DATA2 GPIO_SD_B1_10 ALT1 FLEXSPI_A_DATA3 GPIO_SD_B1_00 ALT1 FLEXSPI_A_DATA3 GPIO_SD_B1_00 ALT1 FLEXSPI_A_DATA5 GPIO_SD_B1_01 ALT1			FLEXSPI B DATA2	GPIO_SD_B1_01	ALT1
FLEXSPI_B_DATA0GPIO_SD_B1_03ALT1FLEXSPI_B_SCLKGPIO_SD_B1_04ALT1FLEXSPI_B_DQSGPIO_SD_B0_05ALT4FLEXSPI_B_SS0_BGPIO_SD_B0_04ALT4FLEXSPI_B_SS1_BGPIO_SD_B0_01ALT6FLEXSPI_A_DQSGPIO_SD_B1_05ALT1FLEXSPI_A_SS0_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B1_07ALT1FLEXSPI_A_SS1_BGPIO_SD_B1_07ALT1FLEXSPI_A_ACKKGPIO_SD_B1_08ALT1FLEXSPI_A_DATA0GPIO_SD_B1_09ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_00ALT1FLEXSPI_A_DATA5GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_B_DATA1	GPIO_SD_B1_02	ALT1
FlexSPI1FLEXSPI_B_SCLKGPIO_SD_B1_04ALT1FLEXSPI_B_DQSGPIO_SD_B0_05ALT4FLEXSPI_B_SS0_BGPIO_SD_B0_04ALT4FLEXSPI_B_SS1_BGPIO_SD_B0_01ALT6FLEXSPI_A_DQSGPIO_SD_B1_05ALT1FLEXSPI_A_SS0_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B1_07ALT1FLEXSPI_A_SCLKGPIO_SD_B1_07ALT1FLEXSPI_A_DATA0GPIO_SD_B1_08ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_00ALT1FLEXSPI_A_DATA6GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_B_DATA0	GPIO_SD_B1_03	ALT1
FlexSPI1FLEXSPI_B_DQSGPIO_SD_B0_05ALT4FLEXSPI_B_SS0_BGPIO_SD_B0_04ALT4FLEXSPI_B_SS1_BGPIO_SD_B0_01ALT6FLEXSPI_A_DQSGPIO_SD_B1_05ALT1FLEXSPI_A_SS0_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B0_00ALT6FLEXSPI_A_SS1_BGPIO_SD_B1_07ALT1FLEXSPI_A_DATA0GPIO_SD_B1_07ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_00ALT1FLEXSPI_A_DATA6GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_B_SCLK	GPIO_SD_B1_04	ALT1
FlexSPI1FLEXSPI_B_SS0_BGPIO_SD_B0_04ALT4FLEXSPI_B_SS1_BGPIO_SD_B0_01ALT6FLEXSPI_A_DQSGPIO_SD_B1_05ALT1FLEXSPI_A_SS0_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B0_00ALT6FLEXSPI_A_SCLKGPIO_SD_B1_07ALT1FLEXSPI_A_DATA0GPIO_SD_B1_08ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_09ALT1FLEXSPI_A_DATA3GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_10ALT1FLEXSPI_A_DATA5GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_B_DQS	GPIO_SD_B0_05	ALT4
FlexSPI1FLEXSPI_B_SS1_BGPIO_SD_B0_01ALT6FLEXSPI_A_DQSGPIO_SD_B1_05ALT1FLEXSPI_A_SS0_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B0_00ALT6FLEXSPI_A_SCLKGPIO_SD_B1_07ALT1FLEXSPI_A_DATA0GPIO_SD_B1_08ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_10ALT1FLEXSPI_A_DATA4GPIO_SD_B1_11ALT1FLEXSPI_A_DATA5GPIO_SD_B1_00ALT1FLEXSPI_A_DATA5GPIO_SD_B1_01ALT1			FLEXSPI_B_SS0_B	GPIO_SD_B0_04	ALT4
FlexSPI1FLEXSPI_A_DQSGPIO_SD_B1_05ALT1FLEXSPI_A_SS0_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B0_00ALT6FLEXSPI_A_SCLKGPIO_SD_B1_07ALT1FLEXSPI_A_DATA0GPIO_SD_B1_08ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA6GPIO_SD_B1_00ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_B_SS1_B	GPIO_SD_B0_01	ALT6
FlexSPI1FLEXSPI_A_SS0_BGPIO_SD_B1_06ALT1FLEXSPI_A_SS1_BGPIO_SD_B0_00ALT6FLEXSPI_A_SCLKGPIO_SD_B1_07ALT1FLEXSPI_A_DATA0GPIO_SD_B1_08ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_11ALT1FLEXSPI_A_DATA6GPIO_SD_B1_00ALT1FLEXSPI_A_DATA5GPIO_SD_B1_01ALT1			FLEXSPI_A_DQS	GPIO_SD_B1_05	ALT1
FLEXSPI_A_SS1_BGPIO_SD_B0_00ALT6FLEXSPI_A_SCLKGPIO_SD_B1_07ALT1FLEXSPI_A_DATA0GPIO_SD_B1_08ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_00ALT1FLEXSPI_A_DATA6GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1	FlexSPI	1	FLEXSPI_A_SS0_B	GPIO_SD_B1_06	ALT1
FLEXSPI_A_SCLKGPIO_SD_B1_07ALT1FLEXSPI_A_DATA0GPIO_SD_B1_08ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_00ALT1FLEXSPI_A_DATA6GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1		Į.	FLEXSPI_A_SS1_B	GPIO_SD_B0_00	ALT6
FLEXSPI_A_DATA0GPIO_SD_B1_08ALT1FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_00ALT1FLEXSPI_A_DATA6GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_A_SCLK	GPIO_SD_B1_07	ALT1
FLEXSPI_A_DATA1GPIO_SD_B1_09ALT1FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_00ALT1FLEXSPI_A_DATA6GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_A_DATA0	GPIO_SD_B1_08	ALT1
FLEXSPI_A_DATA2GPIO_SD_B1_10ALT1FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_00ALT1FLEXSPI_A_DATA6GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_A_DATA1	GPIO_SD_B1_09	ALT1
FLEXSPI_A_DATA3GPIO_SD_B1_11ALT1FLEXSPI_A_DATA7GPIO_SD_B1_00ALT1FLEXSPI_A_DATA6GPIO_SD_B1_01ALT1FLEXSPI_A_DATA5GPIO_SD_B1_02ALT1			FLEXSPI_A_DATA2	GPIO_SD_B1_10	ALT1
FLEXSPI_A_DATA7 GPIO_SD_B1_00 ALT1 FLEXSPI_A_DATA6 GPIO_SD_B1_01 ALT1 FLEXSPI_A_DATA5 GPIO_SD_B1_02 ALT1			FLEXSPI_A_DATA3	GPIO_SD_B1_11	ALI1
FLEXSPI_A_DATA6 GPIO_SD_B1_01 ALT1 FLEXSPI_A_DATA5 GPIO_SD_B1_02 ALT1			FLEXSPI_A_DATA7	GPIO_SD_B1_00	ALI1
FLEASPI_A_DATAS GPIO_SD_B1_02 ALT1			FLEXSPI_A_DATA6		AL 11
			FLEASFI_A_DATAS	GPIO SD B1 02	

Table 11.	ROM Bootloader	Peripheral PinMux
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7. Layout recommendations

7.1. Stackup

A high-speed design requires a good stackup to have the right impedance for the critical traces.

.062" THK +/- 10%		F[N[SHED Cu) WEIGHT
A_TARGET 3 NILS (B_TARGET 52 NILS (LAYER 1 LAYER 2 LAYER 3	COMPONENT SIDE GROUND PLANE POWER PLANE	1/2az+plating 1 az. 1 az.
C_TARGET: 3 NILS	LAYER 4	SOLDER SIDE	1/2az+plating

Figure 5. IMXRT1050-EVKB stackup

The constraints for the trace width depend on many factors, such as the board stackup and the associated dielectric and copper thickness, required impedance, and required current (for power traces). The stackup also determines the constraints for routing and spacing. Consider the following when designing the stackup and selecting the material for your board:

- The board stackup is critical for the high-speed signal quality.
- Preplan the impedance of the critical traces.
- The high-speed signals must have reference planes on adjacent layers to minimize crosstalk.
- The NXP reference design equals Isola FR4.
- The NXP validation boards equal Isola FR4.
- The recommended stackup is four layers, with the layer stack shown in Figure 5. The left-hand image shows the detail provided by NXP inside the fabrication detail as a part of the Gerber files. The right-hand side shows the solution suggested by the PCB fabrication company for the requirements. Figure 6 shows the IMXRT1050-EVKB PCB stackup implementation:

	Single	Ended	Differential		Dífferential			
Layers	Frace Width (Nils	Impedance (Öhms	Trace Width (Nils)	Trace Spacing "Airgap" (Nils]	Impedance (Ohms	Trace Nidlh (Nils)	Trace Spacing 'Airgap' (Mils)	Impedance (Ohms
LI	5,00	50	42	6,00	100	4 70	5,00	90
L4	5,00	50				4 70	5,00	90

7.2. Placement of bulk and decoupling capacitors

Place the small decoupling capacitors and the larger bulk capacitors on the bottom side of the CPU. The 0402 decoupling capacitors and the 0603 bulk capacitors must be placed as close as possible to the power balls. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure the high-speed transient current demand of the processor. The correct via size, trace width,

and trace space are critical to preserve the adequate routing space. The recommended geometry is as follows:

- For the BGA constraint area:
 - The via type is 14/8 mils, the trace width is 4 mils, and the trace space is 3.79 mils.
- For the default area (except for the BGA):
 - The via type is 18/8 mils, the trace width is 5 mils, and the trace space is 7 mils.
 - The preferred BGA power-decoupling design layout is available at <u>nxp.com</u>.
 - Use the NXP design strategy for power and decoupling.

7.3. SDRAM

The SDRAM interface (running at up to 166 MHz) is one of the critical interfaces for the chip routing. The controlled impedance for the single-ended traces must be 50 Ω . Ideally, route all signals at the same length as the EVK board. See the IMXRT1050-EVKB layout to route all signals at the same length (±50 mils).

The SDRAM routing must be separated into three groups: data, address, and control. See the EVK layout to separate all SDRAM signals into two groups:

- All data lines and DM[x]
- All address lines and control lines

Because the RT1050-EVK is a 4-layer board design, both routing groups refer to the GND plane for the impedance control. One group is routed at the top layer (the reference plane is the second layer), while the other group is routed at the bottom layer (the reference plane is the third layer).

7.4. USB

Use these recommendations for the USB:

- Route the high-speed clocks and the DP and DM differential pair firstly.
- Route the DP and DM signals on the top (or bottom) layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω .
- Route the traces over the continuous planes (power and ground):
 - They must not pass over any power/GND plane slots or anti-etch.
 - When placing the connectors, make sure that the ground plane clearouts around each pin have ground continuity between all pins.
- Maintain the parallelism (skew-matched) between DP and DM, and match the overall differential length difference to less than 5 mils.
- Maintain the symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces (and/or data buses).
- Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.

- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum amount of corners. Use 45-degree turns instead of 90-degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.

7.5. High-speed signal routing recommendations

The following list provides recommendations for routing the traces for high-speed signals. Note that the propagation delay and the impedance control must match to have a correct communication with the devices.

- The high-speed signals (SDRAM, RMII, Display, Hyperflash, SD card) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in the reference planes. Review the via voids to ensure that they do not create splits (space out vias).
- Provide the ground return vias within a 100-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- A solid GND plane must be directly under the crystal-associated components, and traces.
- The clocks or strobes that are on the same layer need at least 2.5× spacing from the adjacent traces (2.5× height from the reference plane) to reduce crosstalk.
- Provide the ground return vias within a 100-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- All synchronous modules must have the bus length matching and relative clock length control.
- For the SD module interfaces:
 - Match the data, clock, and CMD trace lengths (length delta depends on the bus rates).
 - Follow similar SDRAM rules for data, address, and control as for the SD module interfaces.

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