SGS-THOMSON MICROELECTRONICS

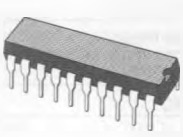
MK4505M/S -25/33/50

VERY HIGH-SPEED CMOS CLOCKED FIFO

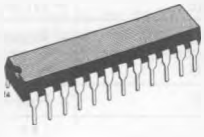
- 1024 x 5 ORGANIZATION
- VERY HIGH PERFORMANCE

Part No	Cycle Time	Cycle Frequency	Access Time
4505-25	25ns	40MHz	15ns
4505-33	33ns	30MHz	20ns
4505-50	50ns	20MHz	25ns

- RISING EDGE TRIGGERED CLOCK INPUTS
- SUPPORTS FREE-RUNNING 40% TO 60% DUTY CYCLE CLOCK INPUTS
- SEPARATE READ AND WRITE ENABLE INPUTS
- BiPORT™ RAM ARCHITECTURE ALLOWS FULLY ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE OPERATION
- CASCADABLE TO ANY DEPTH WITH NO ADDITIONAL LOGIC
- WIDTH EXPANDABLE TO MORE THAN 40 BITS WITH NO ADDITIONAL LOGIC
- HALF FULL STATUS FLAG
- FULL AND EMPTY FLAGS, ALMOST FULL, ALMOST EMPTY, INPUT READY, OUTPUT VALID STATUS FLAGS (4505M)
- FULLY TTL COMPATIBLE



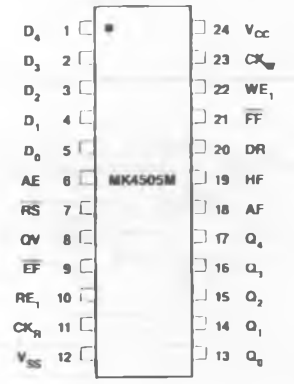
N
PDIP20
(300-Mil PDIP)

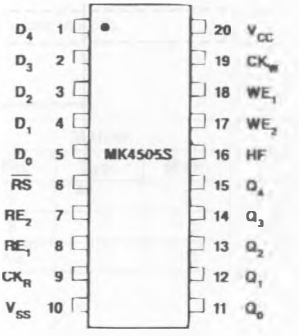


N
PDIP24
(300-Mil PDIP)

(Ordering Information at the end of the datasheet)

Figure 1 : Pin Configurations.





DESCRIPTION

The MK4505 is a Very High Speed 1K x 5 Clocked FIFO memory. It achieves its high performance through the use of a pipelined architecture, a 1.2µ full CMOS, single poly, double level metal process, and a memory array constructed using SGS-THOMSON'S 8 transistor BiPORT memory cell.

The device is designed for use in applications where data is moving through a system on a square wave clock ; applications such as digitized video and audio, image processing, A-to-D and D-to-A conversions, high speed data links, Radar return sampling or data tracing.

The device is available in two versions ; a Master, the MK4505M, and a Slave, the MK4505S. The Master provides all of the control signals necessary for reliable, full speed, fully asynchronous width expansion and/or depth expansion. The Master also provides a full compliment of status flags, including Output Valid, Empty, Almost Empty, Half Full, Al-

most Full, Full, and Input Ready. The Master cannot be written while Full or read while Empty. The Slave, in contrast, can be forced to write and/or read continuously regardless of device status ; a feature useful in triggered data acquisitions, or for retransmit (repeat reading) applications.

PIN NAMES

D_0 - D_4	– Data Input
Q_0 - Q_4	– Data Output
CK_W, CK_R	– Write and Read Clock
WE_1	– Write Enable Input 1
RE_1	– Read Enable Input 1
RS	– Reset (active low)
HF	– Half Full Flag
V_{CC}, V_{SS}	– + 5 Volt, Ground

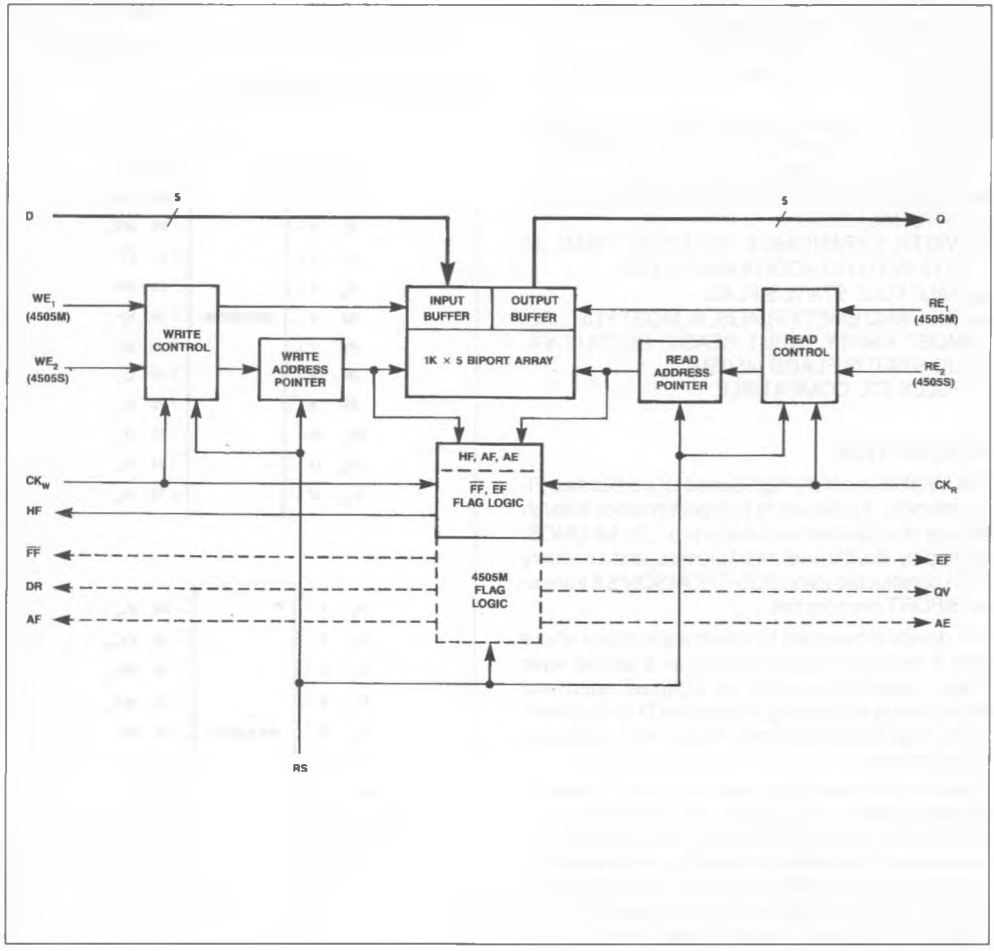
4505M only

FF, EF	– Full and Empty Flag (active low)
AF, AE	– Almost Full, Almost Empty Flag
DR, QV	– Input Ready, Output Valid

4505S only

WE_2	– Write Enable Input 2
RE_2	– Read Enable Input 2 (rising edge triggered 3 state control)

Figure 2 : Block Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	– 1.0 to 7.0	V
T_A	Ambient Operating Temperature	0 to + 70	°C
T_{stg}	Ambient Storage Temperature (plastic)	– 55 to + 125	°C
P_D	Total Device Power Dissipation	1	Watt
I_P	Output Current per Pin	25	mA

Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq + 70°C$)

Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		V_{CC} + 1.0	V	1
V_{IL}	Logic 0 Input	– 0.3		0.8	V	1

Note : 1. All voltages referenced to GND.

DC ELECTRICAL CHARACTERISTICS
($T_A = 0°C$ to $70°C$, $V_{CC} = 5.0 \pm 10\%$)

Symbol	Parameter	4505-25			4505-33			4505-50			Unit	Note
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{CC}	Average Power Supply Current		115	140		95	140		75	140	mA	1

Symbol	Parameter	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current	– 1	+ 1	µA	2
I_{OL}	Output Leakage Current	– 10	+ 10	µA	2, 3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = – 4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4

Notes : 1. Measured with both ports operating at t_{CK} Min, 50% duty cycle, outputs open, V_{CC} max. Typical values reflect t_{CK} Min, outputs open, with V_{CC} = 5.0, 25°C, with 50% duty cycle.
2. Measured with V = 0.0V to V_{CC}.
3. Measured at $Q_0 - Q_4$, with QV = Low (4505M) ; after clocking with RE_2 = Low (4505S).
4. All voltages referenced to GND.

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

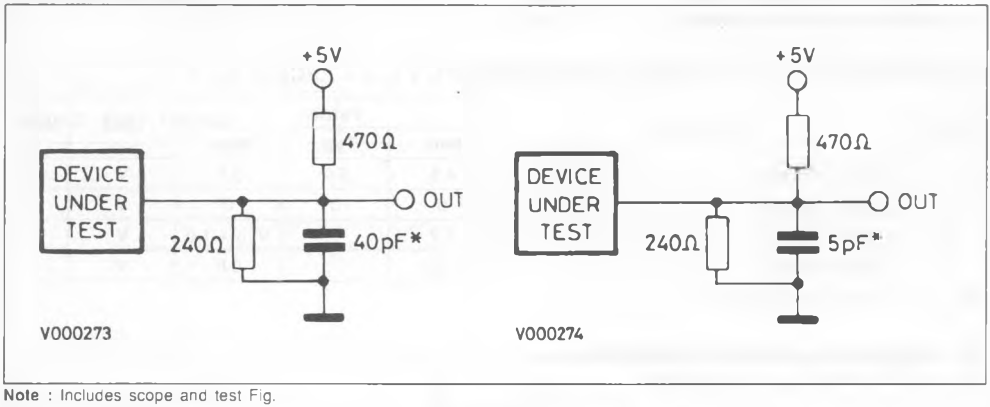
Symbol	Parameter	Value			Unit	Note
		Min.	Typ.	Max.		
C_I	Input Capacitance	4		5	pF	1
CO_1	Output Capacitance	8		10	pF	1, 2
CO_2	Output Capacitance	12		15	pF	1, 3

Notes : 1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data and flag outputs except $\overline{EF}$ and $\overline{FF}$.
3. Measured at $\overline{EF}$ and $\overline{FF}$.

AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Times	5	ns
Input and Output Timing Reference Levels	1.5	V
Ambient Temperature	0 to 70	°C
V_{CC}	5.0 ± 10%	V

Figure 3 : Output Load Circuit.



Note : Includes scope and test Fig.

READ AND HOLD OPERATIONS

The device will perform a Read on the next rising edge of the Read Clock (CK_R) whenever (see figure 4) :

- (4505S) RE_1 and RE_2 are high at the rising edge of the clock.
- (4505M) RE_1 and $\overline{EF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Empty Flag ($\overline{EF}$) on the rising edge of CK_R, the appearance of an active Empty Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CK_R will generate an inhibit condition. All Q outputs will be High Z at t_{QZ} from the rising edge of CK_R. $\overline{EF}$ is latched between subsequent read clocks.

The device will perform a Hold Cycle (hold over previous data) if RE_1 is low at the rising edge of the clock (CK_R). If $\overline{EF}$ (4505M) or RE_2 (4505S) is low at the rising edge of the clock, then the outputs will go to High-Z.

WRITE OPERATIONS

The device will perform a Write on the next rising edge of the Write Clock (CK_W) whenever (see figure 5) :

- (4505S) WE_1 and WE_2 are high at the rising edge of the clock.
- (4505M) WE_1 and $\overline{FF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Full Flag ($\overline{FF}$) on the rising edge of CK_W, the appearance of an active Full Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CK_W will generate a No-Op condition. $\overline{FF}$ is latched between subsequent write clocks.

MK4505M (Master) WRITE TRUTH TABLE

CK_W	Present State			Operation	Next State	
	$\overline{RS}$	WE_1	$\overline{FF}$		$\overline{FF}$	Data In
X	0	X	X	Reset	1	Don't Care
↑	1	0	0	No-Op	?	Don't Care
↑	1	0	1	No-Op	1	Don't Care
↑	1	1	0	No-Op	?	Don't Care
↑	1	1	1	Write	?	Data In

? = Device Status is referenced to the "next state" logic conditions.
The "next state" flag logic level is unknown due to the possible occurence of a read operation.

MK4505M (Master) READ TRUTH TABLE

CK_R	Present State			Operation	Next State	
	$\overline{RS}$	RE_1	$\overline{EF}$		$\overline{EF}$	Q_{OUT}
X	0	X	X	Reset	0	Hi Z
↑	1	0	0	Inhibit	?	Hi Z
↑	1	0	1	Hold	1	Previous Q
↑	1	1	0	Inhibit	?	Hi Z
↑	1	1	1	Read	?	Data Out

? = Device Status is referenced to the "next state" flag logic and Q_{OUT} conditions.
The "next state" flag logic level is unknown due to the possible occurrence of a write operation.

MK4505S (Slave) WRITE TRUTH TABLE

CK_W	Present State			Operation	Next State
	$\overline{RS}$	WE_1	WE_2		Data
X	0	X	X	Reset	Don't Care
↑	1	0	0	No-Op	Don't Care
↑	1	0	1	No-Op	Don't Care
↑	1	1	0	No-Op	Don't Care
↑	1	1	1	Write	Data In

MK4505S (Slave) READ TRUTH TABLE

CK_W	Present State			Operation	Next State
	$\overline{RS}$	RE_1	RE_2		Q_{OUT}
X	0	X	X	Reset	Hi Z
↑	1	0	0	Inhibit	Hi Z
↑	1	0	1	Hold	Previous Q
↑	1	1	0	Inhibit	Hi Z
↑	1	1	1	Read	Data Out

RESET

$\overline{RS}$ is an asynchronous master reset input. A Reset is required after power-up, before first write. Reset commences on the falling edge of $\overline{RS}$ irrespective of the state of any other input or output. The user is required to observe Reset Set Up Time (t_{RSS}) only if the device is enabled (see figure 7). The t_{RSS} specification is a don't care if the device remains disabled ($WE_1 = RE_1 = LOW$). All status flag outputs will be valid t_{RSA} from the falling edge of $\overline{RS}$, and all Q data outputs will be high impedance t_{RSQZ} from the same falling edge.

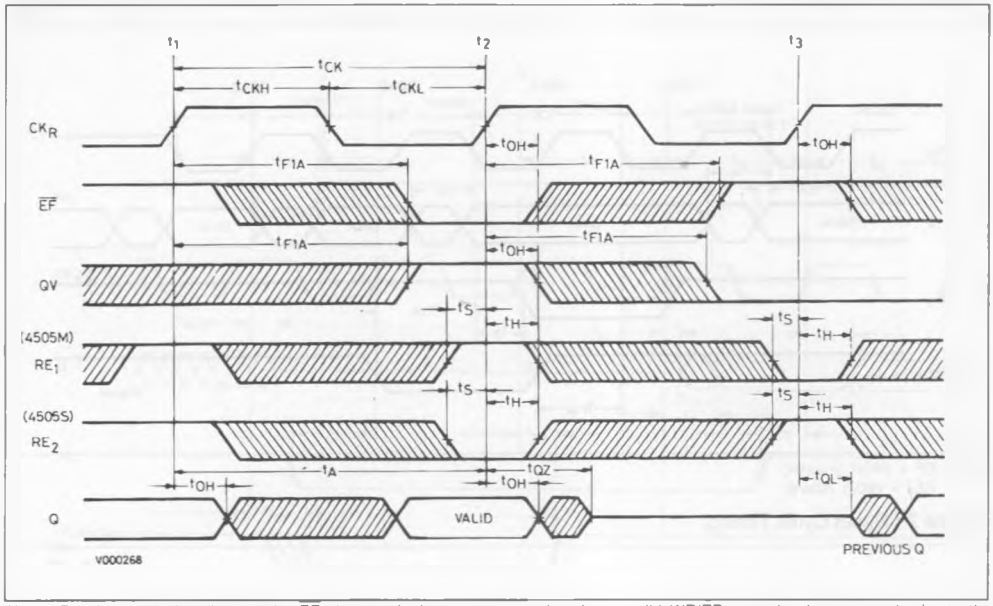
After Reset, if no valid Read operations have been performed since Reset, the "previous data" that will be output when executing the first Hold cycle will be all zeros (see figure 8).

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	4505-25		4505-33		4505-50		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CK}	Clock Cycle Time	25		33		50		ns	1
t_{CKH}	Clock High Time	10		13		20		ns	1
t_{CKL}	Clock Low Time	10		13		20		ns	1
t_S	Set Up Time	10		13		16		ns	1
t_H	Hold Time	0		0		0		ns	
t_A	Output (Q) Access Time		15		20		25	ns	1, 2
t_{F1A}	Flag 1 Access Time(7)		15		20		25	ns	1, 2
t_{F2A}	Flag 2 Access Time(8)		20		25		30	ns	1, 2
t_{OH}	Output Hold Time	5		5		5		ns	1, 2
t_{OZ}	Clock to Outputs High-Z		15		20		25	ns	1, 3
t_{OL}	Clock to Outputs Low-Z	5		5		5		ns	1, 3
t_{RSS}	Reset Set Up Time	12		16		25		ns	1, 4
t_{RS}	Reset Pulse Width	25		33		50		ns	
t_{RSA}	Reset Flag Acces Time		50		66		100	ns	1, 3
t_{RSOZ}	Reset to Outputs High-Z		25		33		50	ns	1, 3
t_{FRL}	First Read Latency	50		66		100		ns	1, 5
t_{FFL}	First Flag Cycle Latency	25		33		50		ns	1, 6

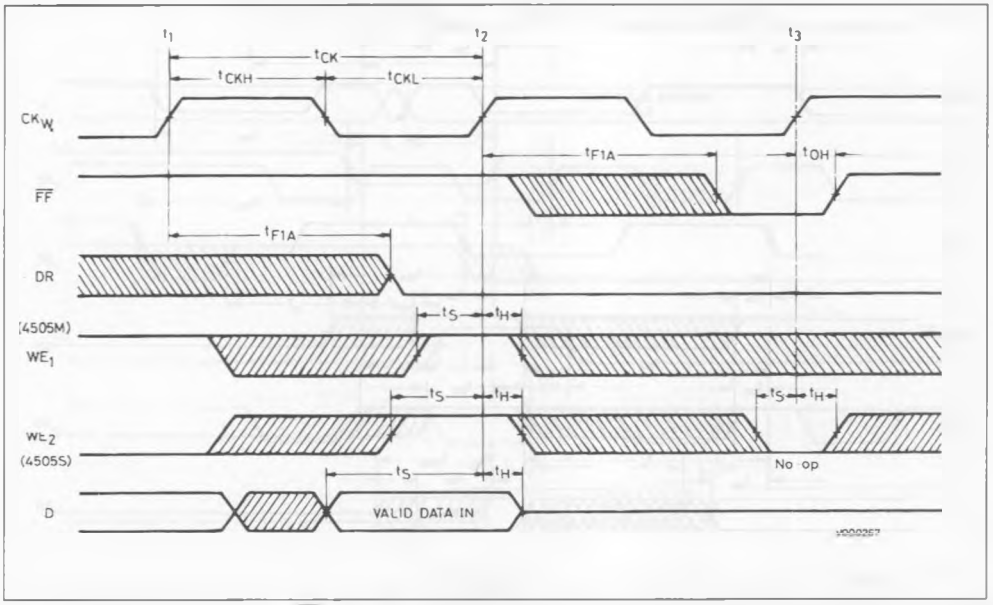
Notes : 1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/40pf Output Load (figure 3A).
3. Measured w/5pf Output Load (figure 3B).
4. Need not be met unless device is Read and/or Write Enabled.
5. Minimum first Write to first Read delay required to assure valid first Read.
6. Minimum first Write to first Read Clock delay required to assure clearing the Empty Flag.
7. Flag 1 = $\overline{EF}$, $\overline{FF}$, QV, DR.
8. Flag 2 = AE, AF, HF.

Figure 4 : Read Cycle Timing.



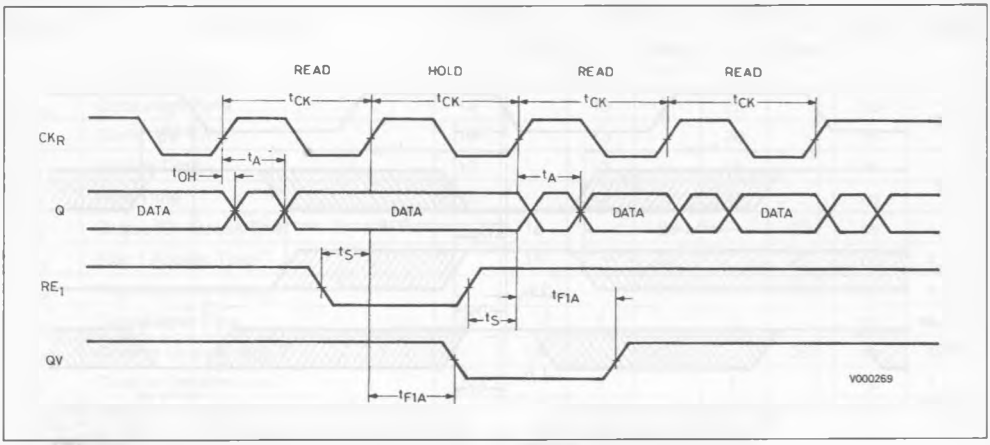
Note : For this particular diagram the $\overline{EF}$ changes logic states presuming that a valid WRITE operation has occured prior to the rising edge of CK_R at t_2.

Figure 5 : Write Cycle Timing.



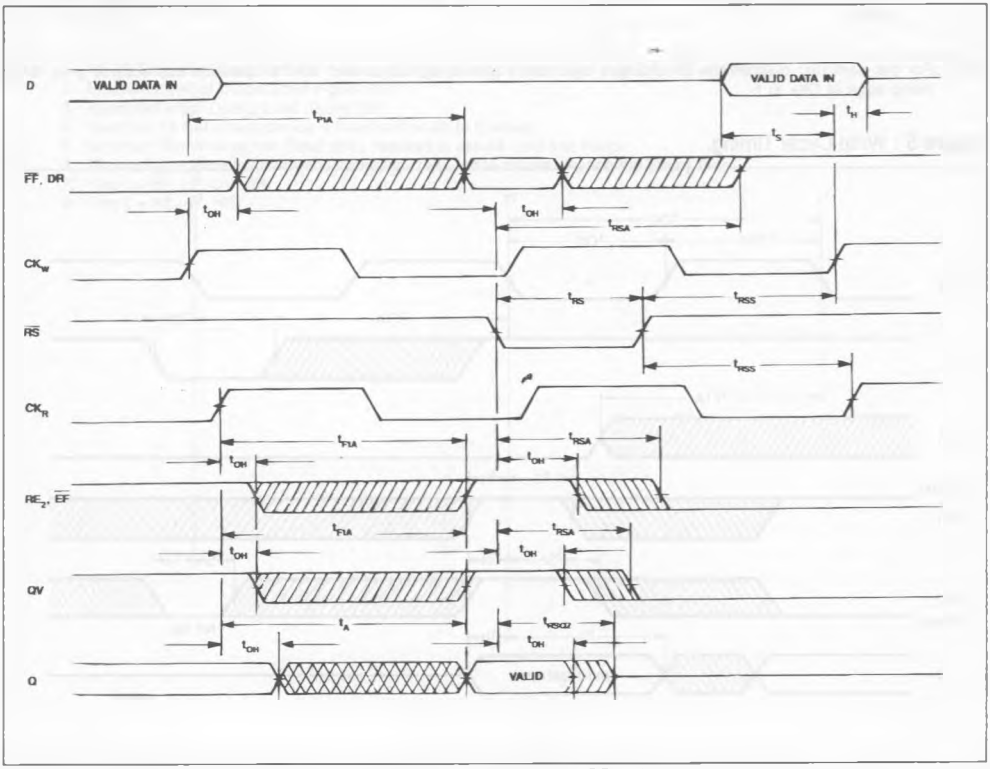
Note : For this particular diagram the $\overline{FF}$ changes logic states presuming that a valid READ operation has occured prior to the rising edge of CK_W at t_3.

Figure 6 : Hold Cycle Timing.



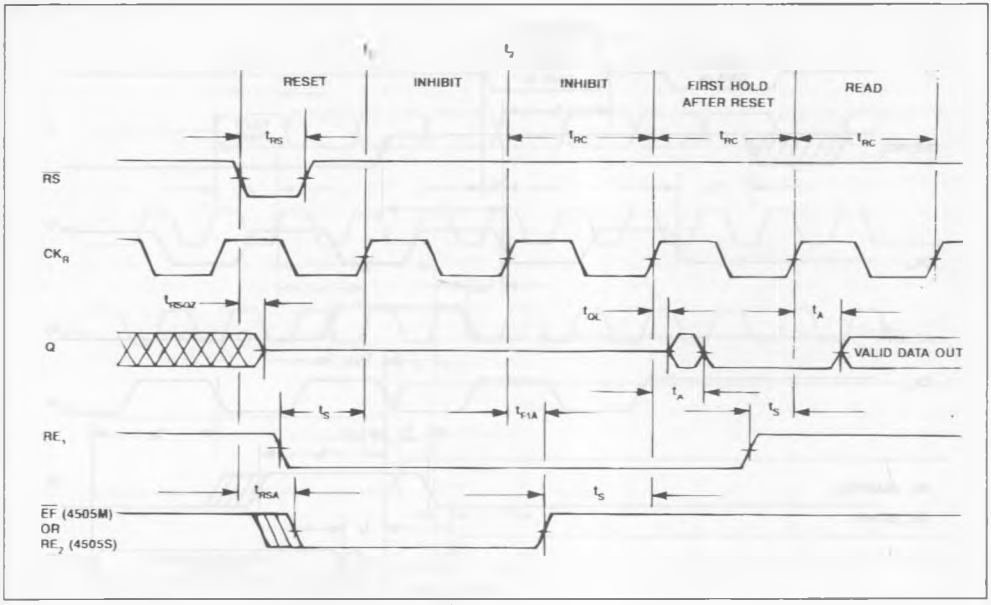
Note : $\overline{EF}$ = HIGH (master)
RE_2 = HIGH (slave)

Figure 7 : Reset Cycle Timing.



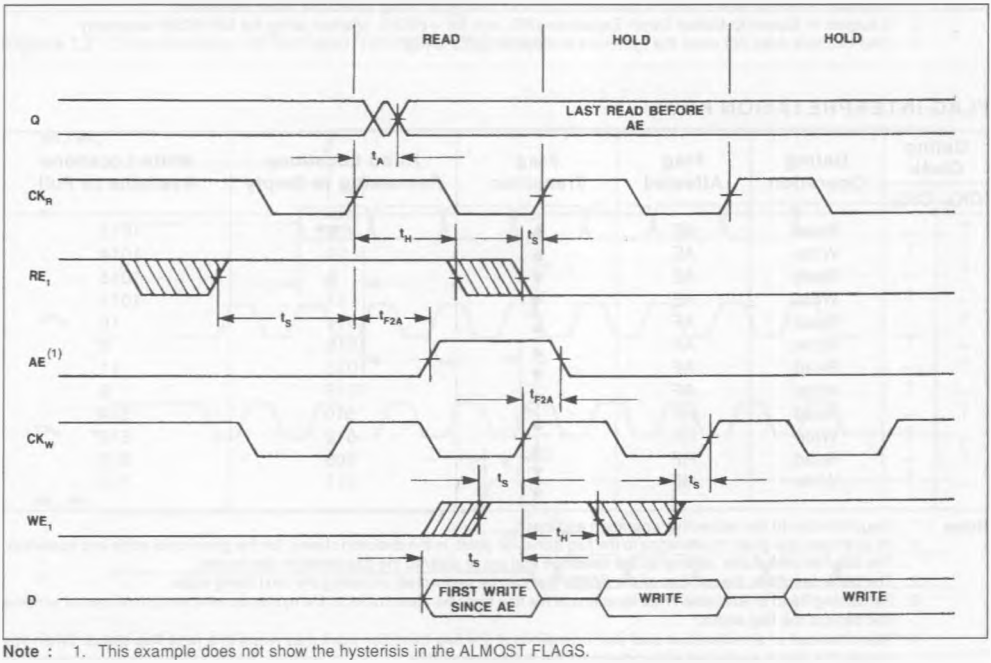
Note : t_{RSS} must be met if the device is read AND/OR write enabled (WE_1, RE_1 = High).

Figure 8 : First Hold After Reset.



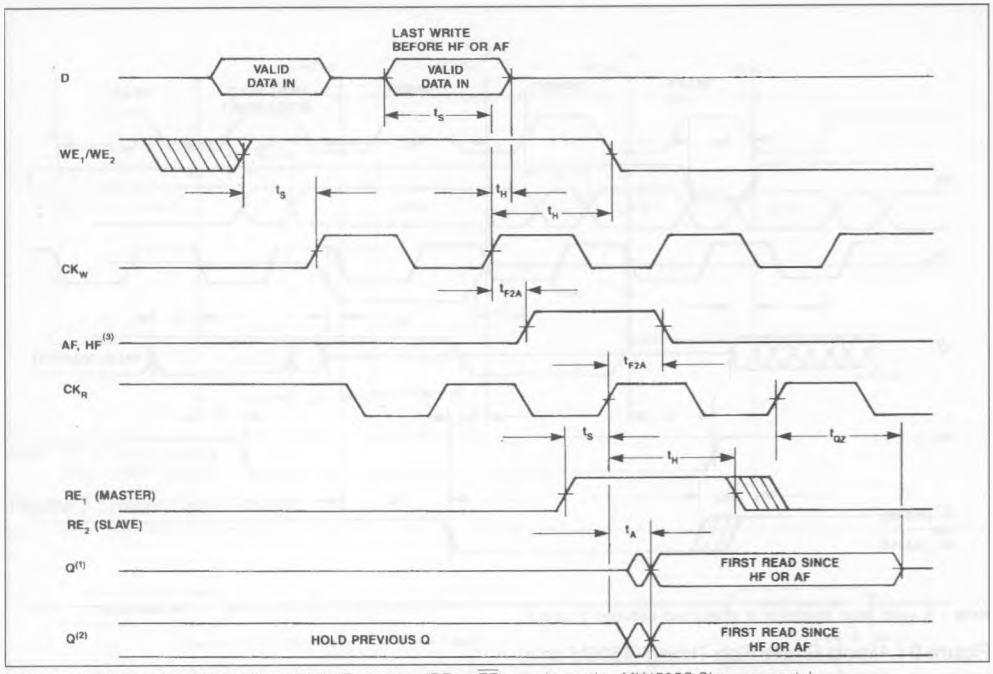
Note : A valid write operation is presumed between t_1 and t_2

Figure 9 : Almost Empty Flag Timing (4505M only).



Note : 1. This example does not show the hysterisis in the ALMOST FLAGS.

Figure 10 : Almost Full, Half Full Flag Timing.



Notes : 1. Q outputs in Master/Slave Width Expansion ($RE_2 = \overline{EF}$), or when using MK4505S Slave separately.
2. Q outputs in Master-to-Master Depth Expansion (RE_1 with $\overline{EF}$ = HIGH), or when using the MK4505M separately.
3. This example does not show the hysterisis in the ALMOST FLAGS.

FLAG INTERPRETATION KEY

Gating Clock		Gating Operation	Flag Affected	Flag Transition	Read Locations Remaining to Empty	Write Locations Available to Full
CK_R	CK_W					
↑	–	Read	AE	▲	8*	1016
–	↑	Write	AE	▲	10	1014
↑	–	Read	AE	▼	9	1015
–	↑	Write	AE	▼	11	1013
↑	–	Read	AF	▲	1014	10
–	↑	Write	AF	▲	1016	8*
↑	–	Read	AF	▼	1013	11
–	↑	Write	AF	▼	1015	9
↑	–	Read	HF	▲	510	514
–	↑	Write	HF	▲	512	512*
↑	–	Read	HF	▼	509	515
–	↑	Write	HF	▼	511	513

Notes : *. Flag definition to the respective operation and clock.
1. All examples are given in reference to the flag transition point, in the direction shown, for the given clock edge and operation. The flag remains stable as long as the condition that set or cleared the flag exists in the device.
2. The table describes the number of the cycles that can be performed, including the next rising edge.
3. Remaining Read or Available Write locations at the flag transition point reflects the hysterisis inherent to the internal scheme that detects the flag status.
4. Asynchronous or simultaneous dual port operations at the flag transition point may result in a false flag status. When this occurs, the flag is evaluated and updated on the subsequent clock.

Figure 11 : Simultaneous Write/Read Timing (4505M only).

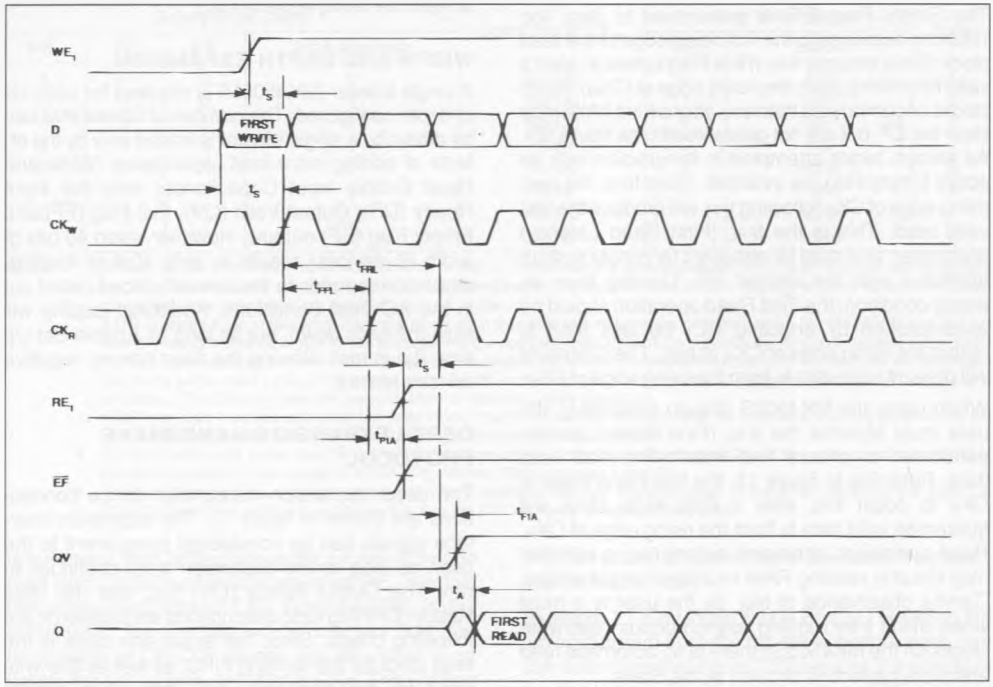
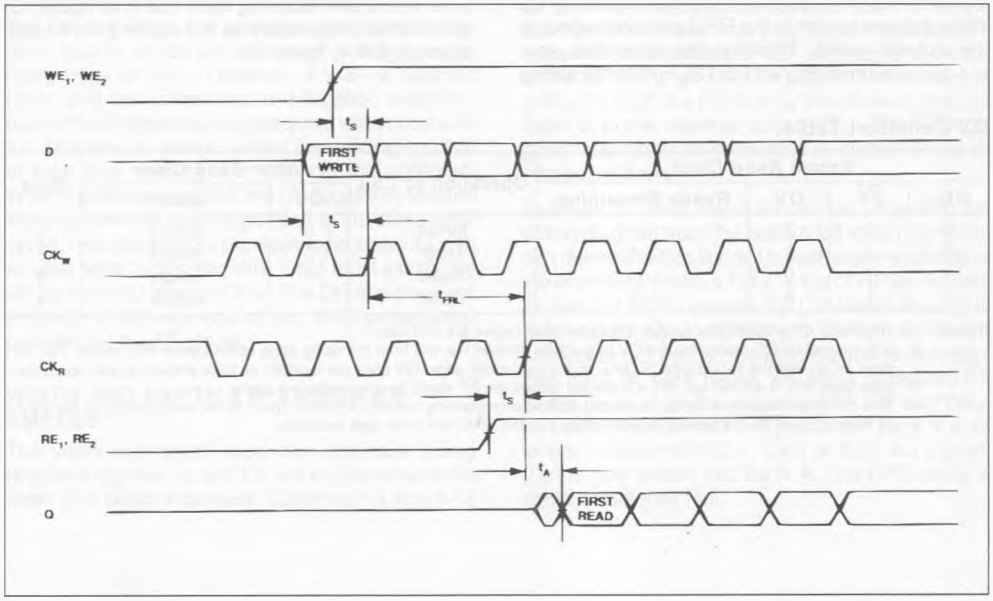


Figure 12 : Simultaneous Write/Read Timing (4505S only).



SIMULTANEOUS WRITE/READ TIMING

The Empty Flag ($\overline{EF}$) is guaranteed to clear (go HIGH) in response to the first rising edge of the read clock (CK_R) to occur t_{FFL} (First Flag Latency) after a valid First Write (from the rising edge of CK_W). Read clocks occurring less than t_{FFL} after a First Write may clear the $\overline{EF}$, but are not guaranteed (see figure 10). As always, reads attempted in conjunction with an active Empty Flag are inhibited. Therefore, the next rising edge of CK_R following t_{FFL} will produce the first valid read. This is the t_{FRL} (First Read Latency) parameter, and must be observed for proper system operation with the latched $\overline{EF}$. Coming from an empty condition, the First Read operation should be accomplished by enabling RE_1 no less than ts before the rising edge of CK_R at t_{FRL}. The Q outputs will present valid data t_A from the rising edge of CK_R.

When using the MK4505S (Slave) separately, the user must observe the t_{FRL} (First Read Latency) parameter to ensure first-write-to-first-read valid data. Referring to figure 12, the first rising edge of CK_R to occur t_{FRL} after a First Write clock will guarantee valid data t_A from the rising edge of CK_R. Read operations attempted before t_{FRL} is satisfied may result in reading RAM locations not yet written. Careful observance of t_{FRL} by the user is a must when using free running asynchronous read/write clocks on the MK4505S ; there is no automatic read and write protection circuitry in the Slave.

It should also be noted that the MK4505M/S has an expected "fall-through delay time" described as First Write data presented to the FIFO and clocked out to the outside world. This can be calculated as : $t_S + t_{FRL} + t_A$ (from figure 11 or 12). Further occurring valid read clocks will present data to the Q outputs t_A from the rising edge of CK_R.

WIDTH AND DEPTH EXPANSION

A single Master (MK4505M) is required for each 1K of depth configured. The number of Slaves that can be driven by a single Master is limited only by the effects of adding extra load capacitance (Write and Read Enable Input Capacitance) onto the Input Ready (DR), Output Valid (QV), Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) outputs. However, even 40 bits of width (8 devices) results in only 40pf of loading, which corresponds to the amount of load called out in the AC Test Conditions. Additional loading will slow the flags down, but as long as Enable Set Up time (t_S) is met, slowing the flags has no negative consequences.

DEPTH EXPANSION HANDSHAKE PROTOCOL

The depth expansion handshake device connections are shown in figure 13. The expansion interface signals can be considered transparent to the user, as long as the expansion clock continues to run. The Output Ready (QV) flag, and the Data Ready (DR) flag logic descriptions are detailed in the following charts. Since the expansion clock is the read clock for the sending FIFO, as well as the write clock for the receiving FIFO, these two signals prevent data loss during depth expansion applications where the receiving bank (bank B, figure 13) goes full simultaneously as the sending bank goes empty (bank A, figure 13).

QV Definition Table.

Before Read Clock				Operation at CK_R	After Read Clock		Note
RE_1	$\overline{EF}$	QV	Reads Remaining		QV	Status	
X	0	X	0	Inhibit	0	Empty	1
0	1	1	≥ 1	Hold	0	Active	2
1	1	0	1	Read	1	Empty	3
1	1	X	≥ 2	Read	1	Active	4

Notes : 1. Whenever EF is active low, further attempted read cycles are inhibited.
2. QV is gated by RE_1 such that the QV flag will be latched low t_{E1A} from the rising edge of CK_R when RE_1 is low. The RE1 input must meet the set-up time (t_S) prior to the read clock edge. QV does not logically allow or prevent a read operation.
3. Whenever RE_1 is active high, QV will always follows the $\overline{EF}$ signal by one read clock cycle.
4. This condition displays a typical read operation when remaining memory locations (prior to the read operation) are from 2 to 1024. $\overline{EF}$ and QV continue to acknowledge that the FIFO has more data available.

DR Definition Table.

Before Write Clock				Operation at CK_W	After Write Clock		Note
WE_1	$\overline{FF}$	DR	Write Available		DR	Status	
X	0	0	0	No-Op	0	Full	1
0	1	0	1	No-Op	1	Full-1	2
0	1	1	1	No-Op	0	Full-1	2
1	1	X	1	Write	0	Full	1
0	1	X	2	No-Op	1	Active	3
1	1	1	2	Write	0	Full-1	4
0	1	1	≥ 3	No-Op	1	Active	
1	1	1	≥ 3	Write	1	Active	5

Notes : 1. DR can be low only when the MK4505M is full or (full-1). Whenever the device goes full ($\overline{FF}$ = low), then DR will be latched low t_{F1A} from the same write clock edge (CK_W) regardless of the logic state of the DR flag at the clock transition. Further attempted write operations are blocked since FF is low.

2. If DR changes logic states after the write clock, then this example reflects the condition when the MK4505M has one (1) memory location available (full-1). DR will presume the opposite logic state of the previous cycle for subsequent write clocks if WE_1 is disabled (low) and one memory location is available. Whenever the MK4505M goes full ($\overline{FF}$ = low), DR will be latched low in the same clock cycle. (This is part of the Depth Expansion Protocol, and acts to notify the sending unit that space is available.) The DR flag does not logically allow or prevent a write operation.

3. If DR is a logic 1 before and after the write clock, then this example signifies that the available memory locations in the MK4505M are greater than or equal to 2, after the completed write operation.

4. During a valid write cycle, the DR flag will go inactive low t_{F1A} from the rising edge of CK_W if the write counter is (full-2) at the clock transition. This results is a (full-1) condition. (Refer to notes 1 and 2.)

5. This condition displays a typical write cycle, where available memory locations (prior to the write operation) are from 3 to 1024. DR and $\overline{FF}$ continue to acknowledge that the FIFO is ready to accept more data.

In summary, the QV flag follows the $\overline{EF}$ signal by one read clock cycle (in all instances) when RE_1 is active high at the rising edge of CK_R. Whenever RE_1 is disabled (low), the QV flag will go low t_{F1A} from the rising edge of CK_R. Of course, the RE_1 input must satisfy the set-up time (t_S) prior to CK_R. The QV flag does not enable or inhibit read operations. Read protection is provided by the EF signal.

The DR flag will go low one cycle prior to a full condition (full-1), or DR will go high at (full-2) from the rising edge of CK_W. However, if WE_1 is disabled (low), and the device has one location available, then DR will toggle each subsequent write cycle until full. This way the device notifies the sending unit that at least one more byte of data can be accepted. When the device goes full, the DR flag will be latched low t_{F1A} from the clock edge (during the same write cycle), regardless of its previous logic state. As with all valid write cycles, the WE_1 input must satisfy the set-up time (t_S) prior to CK_W. The DR flag does not enable or inhibit write operations. Write protection is provided by the $\overline{FF}$ signal.

WIDTH AND DEPTH EXPANSION EXAMPLES

The width and depth expansion interface timing diagrams (figures 14 and 15) are in reference to the width and depth expansion schematic in figure 13 (For simplicity all clocks have the same frequency and transition rate).

Example 1 - First Write Since Empty - Reading the timing diagram from the top left to bottom right, one can determine that figure 13 illustrates the effects of the first WRITE/READ cycles from an EMPTY array of FIFOs. Both of the $\overline{EF}$ pins are initially low ($\overline{EF_X}$, $\overline{EF}$ and RE_2). As data is written into Bank A, the expansion clock reads data from Bank A and writes it to Bank B, the interface $\overline{EF}$ ($\overline{EF}$ and RE_2) and the external $\overline{EF}$ ($\overline{EF_X}$) go inactive (logic 1) while data is shifted through the FIFO array from Bank A through Bank B to the external output (Q_X). The $\overline{EF}$ logic goes valid (logic 0) once data is shifted out of its respective bank.

Example 2 - First Read Since Full - Reading the timing diagram from the bottom left to top right, one can determine that figure 15 illustrates the effects of the first READs from a FULL array of FIFOs. As data is read out of the system (Q_X), it allows Bank B to receive data (Q_{EXP}) shifted from Bank A. As Bank B shifts data out via Q_X, allowing Bank A to shift data into Bank B, both banks will show a cleared $\overline{FF}$ status (logic 1) on the expansion $\overline{FF}$ ($\overline{FF}$ and WE_2) as well as the internal $\overline{FF}$ ($\overline{FF_X}$). When Bank A is no longer considered FULL, Data In from the system (D_X) is now written into Bank A. The FIFO array is again completely Full.

APPLICATION

The MK4505 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK4505 can also interface to 5V CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK4505, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. A high frequency decoupling capacitor should be placed next to each FIFO. The capacitor should be 0.1μF or larger. Also, a pull-up resistor in the range of 1KΩ is recommended for the $\overline{\text{RESET}}$ input pin to improve proper operation.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10Ω to 33Ω often prove most suitable.

Figure 13 : MK4505M/S 2K x 10 Width and Depth Expansion Schematic.

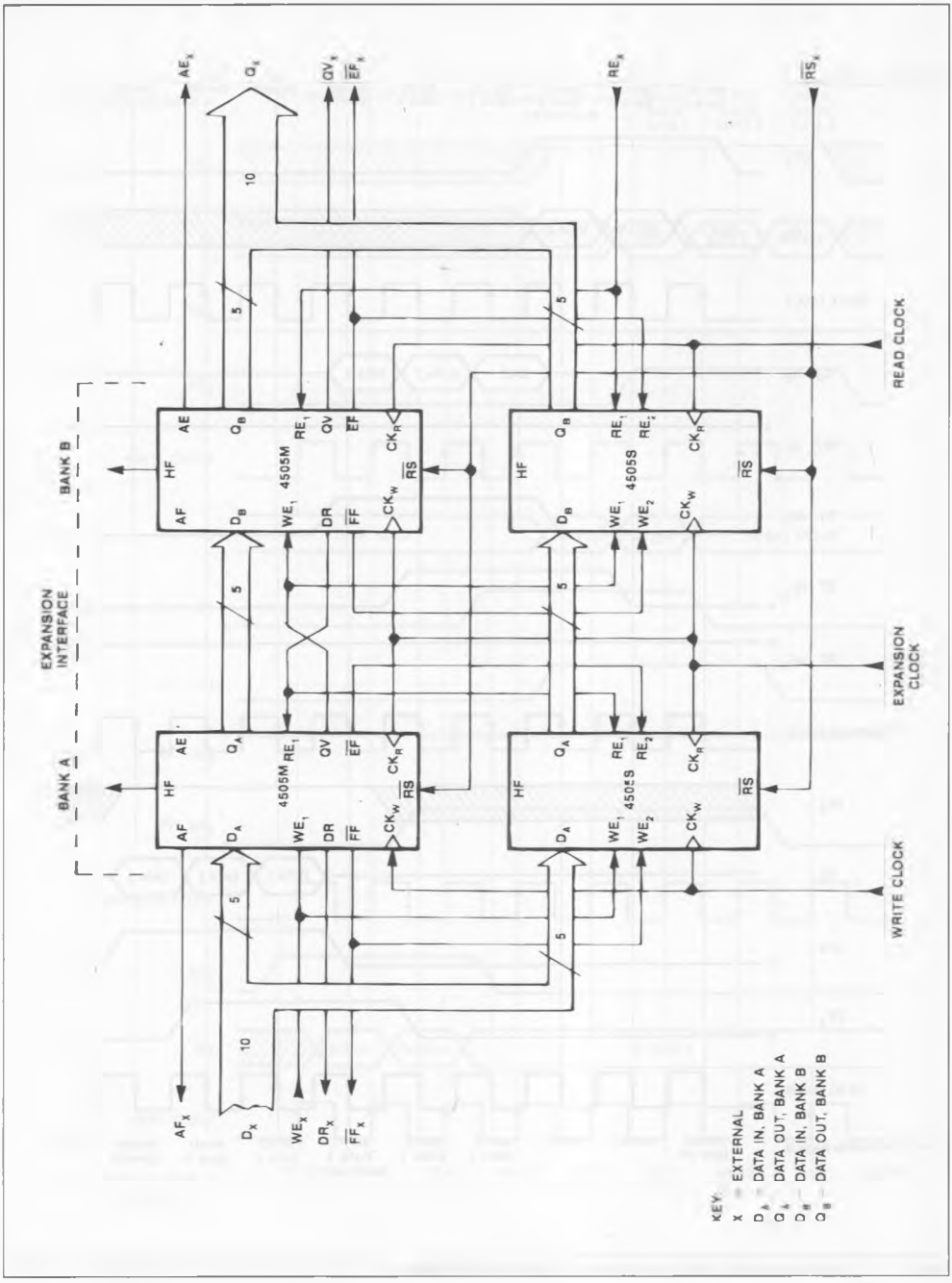
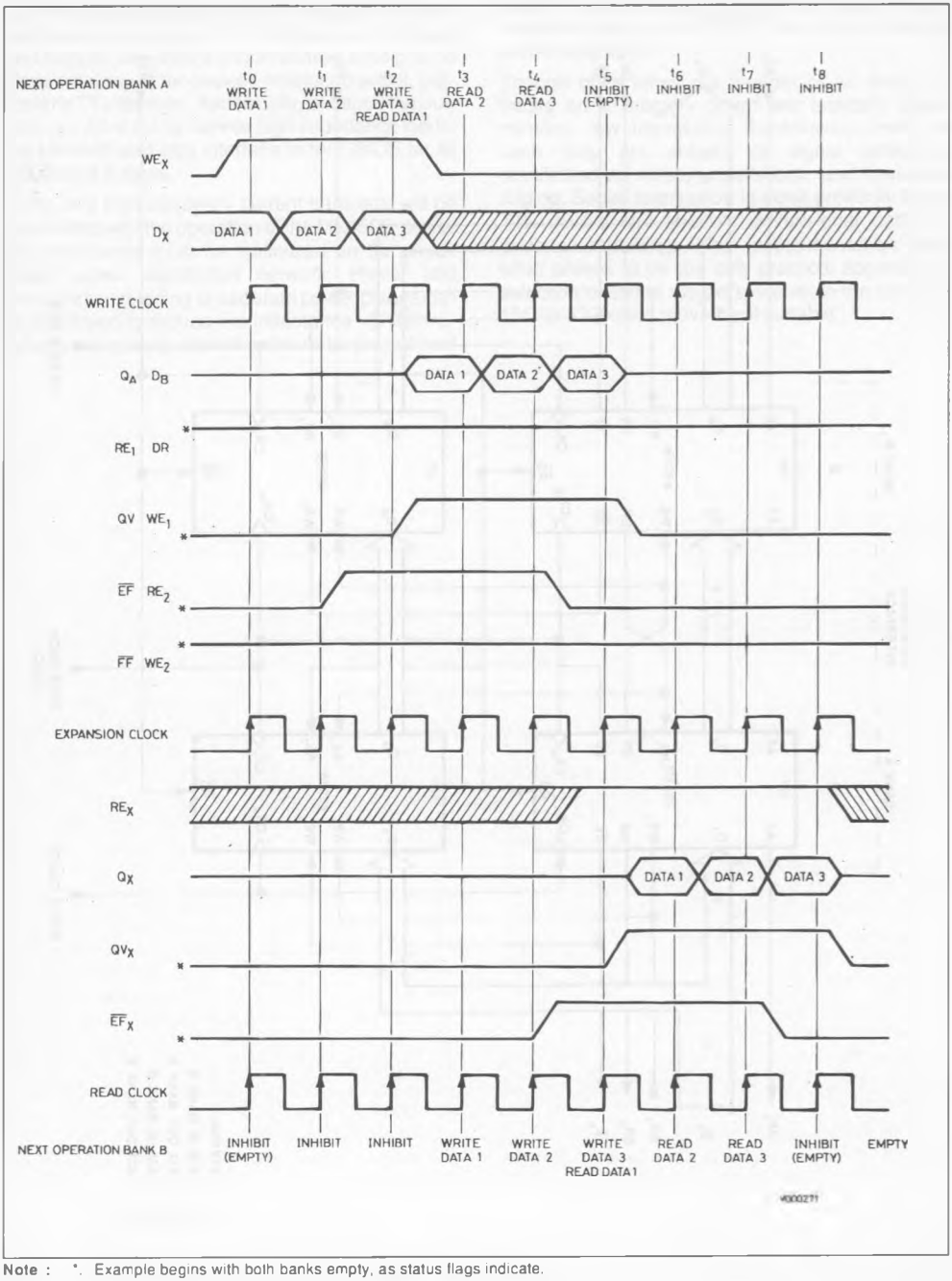
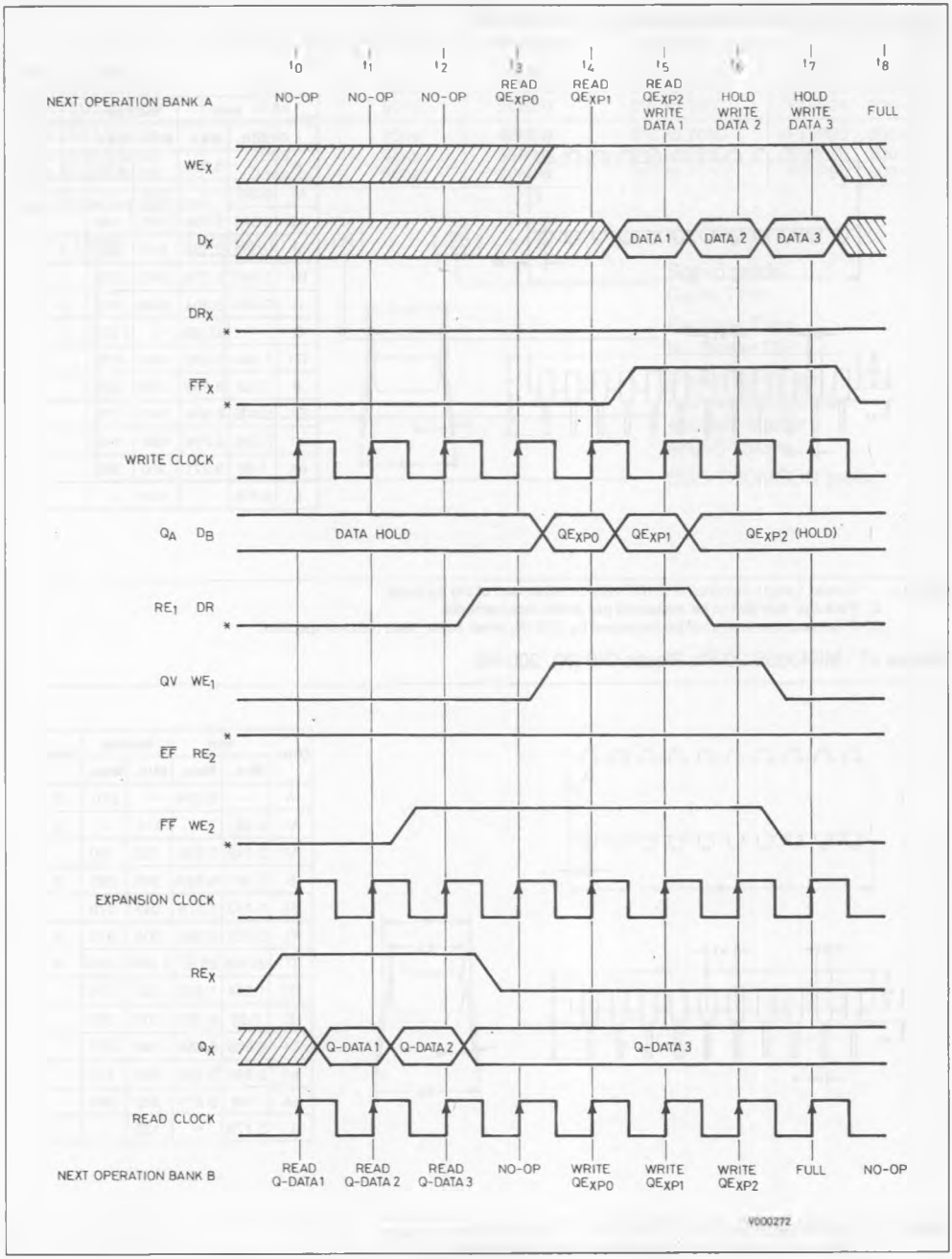


Figure 14 : Example 1 - Width and Depth Expansion Interface Timing.



Note : *. Example begins with both banks empty, as status flags indicate.

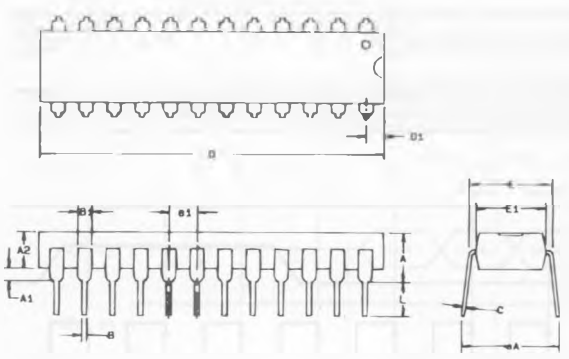
Figure 15 : Example 2 - Width and Depth Expansion Interface Timing.



Note : *. Example begins with both banks full, as indicated by status flags.

PACKAGES MECHANICAL DATA

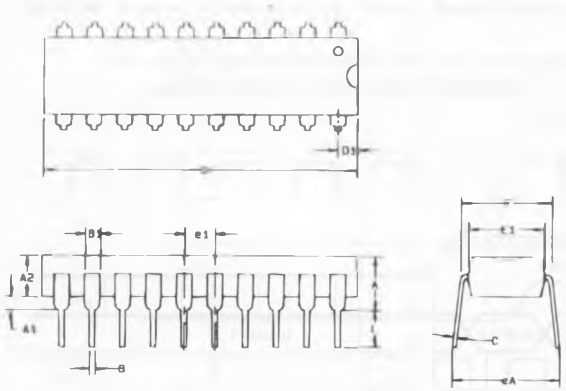
Figure 16 : MK4505M 24-Pin Plastic DIP (N), 300-Mil.



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A	–	5.334	–	.210	2
A1	0.381	–	.015	–	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	–	32.258	–	1.270	1
D1	1.524	2.286	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.906	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	–	.125	–	

Notes : 1. Overall Length includes .010 IN.Flash on either end of the package.
2. Package standoff to be measured per Jedec requirements.
3. The maximum limit shall be increased by .003 IN. when solder lead finish is specified.

Figure 17 : MK4505S 20-Pin Plastic DIP (N), 300-Mil.



Dim.	mm		Inches		Notes
	Min.	Max.	Min.	Max.	
A	–	5.334	–	.210	2
A1	0.381	–	.015	–	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	1.524	1.905	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.906	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	–	.125	–	

Notes : 1. Overall Length includes .010 IN. Flash on either end of the package.
2. Package standoff to be measured per Jedec requirements.
3. The maximum limit shall be increased by .003 IN. when solder lead finish is specified.

ORDERING INFORMATION

Part Number	Access Time	Cycle Time	Cycle Frequency	Temperature Range	Package Type
MK4505MN-25	15ns	25ns	40MHz	0°C to 70°C	PDIP24 300-MIL
MK4505MN-33	20ns	33ns	30MHz	0°C to 70°C	PDIP24 300-MIL
MK4505MN-50	25ns	50ns	20MHz	0°C to 70°C	PDIP24 300-MIL
MK4505SN-25	15ns	25ns	40MHz	0°C to 70°C	PDIP20 300-MIL
MK4505SN-33	20ns	33ns	30MHz	0°C to 70°C	PDIP20 300-MIL
MK4505SN-50	25ns	50ns	20MHz	0°C to 70°C	PDIP20 300-MIL

Note : PDIP = Plastic DIP.