

FEATURES

- Extended operating temperature range ($-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$)
- 44 hr. min., 125°C burn-in plus industrial screening for greater reliability (see Figure 3 for processing description)
- Recognized industry standard 16-pin configuration from Mostek
- 150 ns access time, 320 ns cycle (MKI4116-72)
200 ns access time, 375 ns cycle (MKI4116-73)
250 ns access time, 410 ns cycle (MKI4116-74)
- $\pm 10\%$ tolerance on all power supplies ($+12\text{ V}, \pm 5\text{ V}$)

- Low power: 462 mW active, 30 mW standby (max)
- Output data controlled by CAS and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-modify-write, RAS-only refresh, and page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles (2 msec refresh interval)
- MKB military version available (-55 to 110°C)

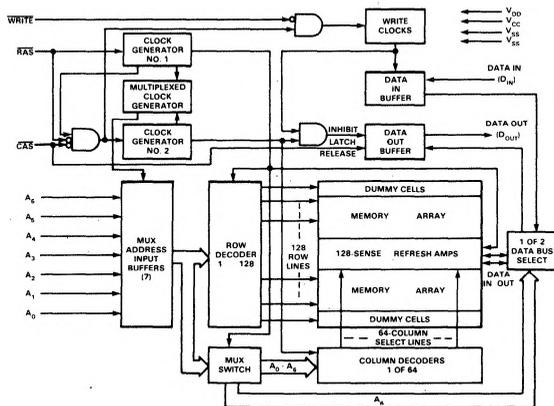
DESCRIPTION

The MKI4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MKI4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in Mostek's high performance MK4027 (4K RAM).

The technology used to fabricate the MKI4116 is Mostek's double-poly, N-channel silicon gate, POLY I™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximal circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MKI4116 a truly superior RAM product.

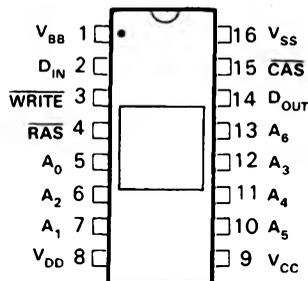
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



PIN NAMES

| Pin Name | Function | Power |
|---------------------------------|---------------------|------------------------------|
| A ₀ - A ₆ | Address Inputs | |
| CAS | Col. Address Strobe | V _{BB} Power (-5V) |
| D _{IN} | Data In | V _{CC} Power (+5V) |
| D _{OUT} | Data Out | V _{DD} Power (+12V) |
| RAS | Row Address Strobe | V _{SS} Ground |
| WRITE | Write Input | |

ABSOLUTE MAXIMUM RATINGS*

| | |
|--|-------------------|
| Voltage on any pin relative to V_{BB} | -0.5 V to +20 V |
| Voltage on V_{DD} , V_{CC} supplies relative to V_{SS} | -1.0 V to +15.0 V |
| $V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0$ V) | 0V |
| Operating Temperature, T_A (Ambient) | -40°C to +85°C |
| Storage Temperature (Ambient) | -65°C to +150°C |
| Short Circuit Output Current | .50 mA |
| Power Dissipation | 1 Watt |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

(-40°C ≤ T_A ≤ +85°C)

| SYM | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|-----------|---|------|------|------|-------|-------|
| V_{DD} | Supply Voltage | 10.8 | 12.0 | 13.2 | V | 2 |
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 2,3 |
| V_{SS} | Supply Voltage | 0 | 0 | 0 | V | 2 |
| V_{BB} | Supply Voltage | -4.5 | -5.0 | -5.5 | V | 2 |
| V_{IHC} | Input High (Logic 1) Voltage, RAS, CAS, WRITE | 2.7 | — | 7.0 | V | 2 |
| V_{IH} | Input High (Logic 1) Voltage, all inputs except RAS, CAS, WRITE | 2.4 | — | 7.0 | V | 2 |
| V_{IL} | Input Low (Logic 0) Voltage, all inputs | -1.0 | — | .8 | V | 2 |

DC ELECTRICAL CHARACTERISTICS

(-40°C ≤ T_A ≤ +85°C) ($V_{DD} = 5.0$ V ± 10%; -5.5 V ≤ $V_{BB} ≤ -4.5$ V; $V_{SS} = 0$ V)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|-------------------------------------|---|-----|-------------------|----------------|--------|
| I_{DD1} I_{CC1} I_{BB1} | OPERATING CURRENT Average power supply operating current (RAS, CAS cycling; $t_{RC} = t_{RC}(\text{min})$) | | 35 400 | mA μA | 4 5 |
| I_{DD2} I_{CC2} I_{BB2} | STANDBY CURRENT Power supply standby current ($\overline{\text{RAS}} = V_{IHC}$, $D_{OUT} = \text{High Impedance}$) | -10 | 2.25 10 200 | mA μA μA | |
| I_{DD3} I_{CC3} I_{BB3} | REFRESH CURRENT Average power supply current, refresh mode (RAS cycling, CAS = V_{IHC} ; $t_{RC} = t_{RC}(\text{min})$) | -10 | 27 10 400 | mA μA μA | 4 |
| I_{DD4} I_{CC4} I_{BB4} | PAGE MODE CURRENT Average power supply current, page-mode operation (RAS = V_{IL} , CAS cycling; $t_{PC} = t_{PC}(\text{min})$) | | 27 400 | mA μA | 4 5 |
| $I_{(L)}$ | INPUT LEAKAGE Input leakage, any input ($V_{BB} = -5$ V, 0 V ≤ $V_{IN} ≤ +7.0$ V, all other pins not under test = 0 volts) | -10 | 10 | μA | |
| $I_{(L)}$ | OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0 V ≤ $V_{OUT} ≤ +5.5$ V) | -10 | 10 | μA | |
| V_{OH} V_{OL} | OUTPUT LEVELS Output high (Logic 1) voltage ($I_{OUT} = -5$ mA) Output low (Logic 0) voltage ($I_{OUT} = 4.2$ mA) | 2.4 | 0.4 | V V | 3 |

RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS^(6,7,8)
 $(-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C})^1$ ($V_{DD} = 12.0\text{ V} \pm 10\%$; $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $-5.5\text{ V} \leq V_{BB} \leq -4.5\text{ V}$)

| SYM | PARAMETER | MKI4116-72 | | MKI4116-73 | | MKI4116-74 | | UNITS | NOTES |
|-----------|---|------------|------|------------|------|------------|------|-------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t_{RC} | Random read or write cycle time | 320 | | 375 | | 410 | | ns | 9 |
| t_{RWC} | Read-write cycle time | 320 | | 375 | | 425 | | ns | 9 |
| t_{RMW} | Read-modify-write cycle time | 320 | | 405 | | 500 | | ns | 9 |
| t_{PC} | Page mode cycle time | 170 | | 225 | | 275 | | ns | 9 |
| t_{RAC} | Access time from $\overline{\text{RAS}}$ | | 150 | | 200 | | 250 | ns | 10,12 |
| t_{CAC} | Access time from $\overline{\text{CAS}}$ | | 100 | | 135 | | 165 | ns | 11,12 |
| t_{OFF} | Output buffer turn-off delay | 0 | 40 | 0 | 50 | 0 | 60 | ns | 13 |
| t_T | Transition time (rise and fall) | 3 | 35 | 3 | 50 | 3 | 50 | ns | 8 |
| t_{RP} | RAS precharge time | 100 | | 120 | | 150 | | ns | |
| t_{RAS} | $\overline{\text{RAS}}$ pulse width | 150 | 5000 | 200 | 5000 | 250 | 5000 | ns | |
| t_{RSH} | $\overline{\text{RAS}}$ hold time | 100 | | 135 | | 165 | | ns | |
| t_{CSH} | $\overline{\text{CAS}}$ hold time | 150 | | 200 | | 250 | | ns | |
| t_{CAS} | $\overline{\text{CAS}}$ pulse width | 100 | 5000 | 135 | 5000 | 165 | 5000 | ns | |
| t_{RCD} | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time | 20 | 50 | 25 | 65 | 35 | 85 | ns | 15 |
| t_{CRP} | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | 0 | | 0 | | 0 | | ns | |
| t_{ASR} | Row Address set-up time | 0 | | 0 | | 0 | | ns | |
| t_{RAH} | Row Address hold time | 20 | | 25 | | 35 | | ns | |
| t_{ASC} | Column Address set-up time | 0 | | 0 | | 0 | | ns | |
| t_{CAH} | Column Address hold time | 45 | | 55 | | 75 | | ns | |
| t_{AR} | Column Address hold time referenced to $\overline{\text{RAS}}$ | 95 | | 120 | | 160 | | ns | |
| t_{RCS} | Read command set-up time | 0 | | 0 | | 0 | | ns | |
| t_{RCH} | Read command hold time | 0 | | 0 | | 0 | | ns | |
| t_{WCH} | Write command hold time | 45 | | 55 | | 75 | | ns | |
| t_{WCR} | Write command hold time referenced to $\overline{\text{RAS}}$ | 95 | | 120 | | 160 | | ns | |
| t_{WP} | Write command pulse width | 45 | | 55 | | 75 | | ns | |
| t_{RWL} | Write command to $\overline{\text{RAS}}$ lead time | 50 | | 70 | | 85 | | ns | |
| t_{CWL} | Write command to $\overline{\text{CAS}}$ lead time | 50 | | 70 | | 85 | | ns | |
| t_{DS} | Data-in set-up time | 0 | | 0 | | 0 | | ns | 15 |
| t_{DH} | Data-in hold time | 45 | | 55 | | 75 | | ns | 15 |
| t_{DHR} | Data-in hold time referenced to $\overline{\text{RAS}}$ | 95 | | 120 | | 160 | | ns | |
| t_{CP} | $\overline{\text{CAS}}$ precharge time (for page-mode cycle only) | 60 | | 80 | | 100 | | ns | |

RECOMMENDED AC OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS (Cont.)^(6,7,8)
 (-40°C ≤ T_A ≤ +85°C) (V_{DD} = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, -5.5 V ≤ V_{BB} ≤ -4.5 V)

| SYM | PARAMETER | MKI4116-72 | | MKI4116-73 | | MKI4116-74 | | UNITS | NOTES |
|------------------|---------------------------|------------|-----|------------|-----|------------|-----|-------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t _{REF} | Refresh period | | 2 | | 2 | | 2 | ms | 19 |
| t _{WCS} | WRITE command set-up time | 0 | | 0 | | 0 | | ns | 16 |
| t _{CWD} | CAS to WRITE delay | 60 | | 80 | | 90 | | ns | 16 |
| t _{RWD} | RAS to WRITE delay | 110 | | 145 | | 175 | | ns | 16 |

CAPACITANCE

(-40°C ≤ T_A ≤ +85°C) (V_{DD} = 12.0 V ± 10%; V_{SS} = 0 V; -5.5 V ≤ V_{BB} ≤ -4.5 V)

| SYM | PARAMETER | TYP | MAX | UNITS | NOTES |
|-----------------|---|-----|-----|-------|-------|
| C _{I1} | Input Capacitance (A ₀ - A ₆), D _{IN} | 4 | 5 | pF | 17 |
| C _{I2} | Input Capacitance, RAS, CAS, WRITE | 8 | 10 | pF | 17 |
| C _O | Output Capacitance (D _{OUT}) | 5 | 7 | pF | 17,18 |

NOTES:

- T_A is specified here for operation at frequencies to t_{RC} ≥ t_{RC} (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
- All voltages referenced to V_{SS}.
- Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specifications is not guaranteed in this mode.
- I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.
- I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.
- Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- AC measurements assume t_r = 5 ns.
- V_{IHC}(min) or V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} or V_{IL}.
- The specifications for t_{RC} (min) t_{RMW} (min) are used only to indicate cycle which proper operation over the full temperature range (-40°C ≤ T_A ≤ 85°C) is assured.
- Assumes that t_{RCD} ≤ t_{RCD} (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RCD} will increase by the amount that t_{RCD} exceeds the value shown.
- Assumes that t_{RCD} ≥ t_{RCD} (max)
- Measured with a load equivalent to 2 TTL loads and 100pF.
- t_{OPJ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met t_{RCD} (max) is specified as a reference point only, if t_{RCP} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}
- These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
- t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If t_{WCS} ≤ t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If t_{CWD} ≤ t_{CWD} (min) and t_{RWD} ≤ t_{RWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- Effective capacitance calculated from the equation C = IΔt / ΔV with ΔV = 3 volts and power supplies at nominal levels.
- CAS = V_{IHC} to disable D_{OUT}.

DESCRIPTION (Continued)

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MKI4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely avail-

able automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.