

# MM54C941/MM74C941 Octal Buffers/Line Receivers/ Line Drivers with TRI-STATE® Outputs

## General Description

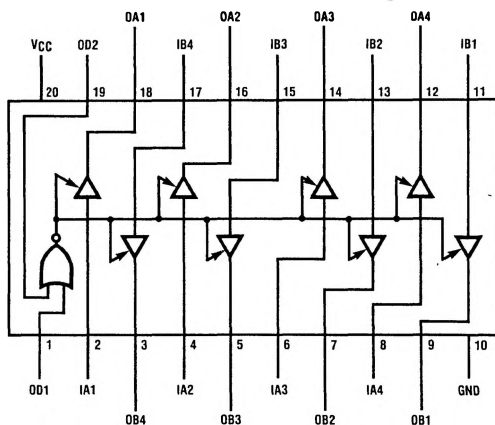
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. When  $V_{CC} = 5V$  inputs can accept true TTL high and low logic levels.

TRI-STATE is a registered trademark of National Semiconductor Corp.

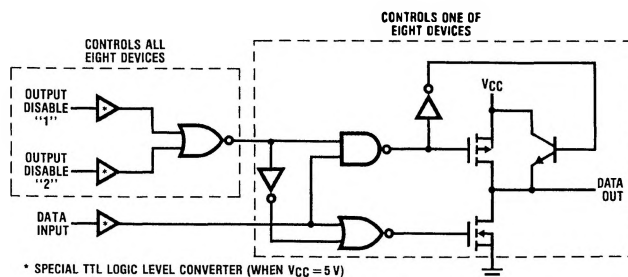
## Features

- Wide supply voltage range (3V to 15V)
- Low power consumption
- TTL compatibility (Improved on the inputs)
- High capacitive load
- TRI-STATE® outputs
- Input protection
- 20-pin dual-in-line package
- High output drive

## Connection Diagram



## Logic Diagram



**Absolute Maximum Ratings** (Note 1)

Voltage at Any Pin	0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C941	-55 °C to +125 °C
MM74C941	-40 °C to +85 °C
Storage Temperature Range	-65 °C to +150 °C
Package Dissipation	500mW
Operating $V_{CC}$ Range	3.0V to 15V
$V_{CC}$	18V
Lead Temperature (Soldering, 10 seconds)	300 °C

**DC Electrical Characteristics** Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
<b>CMOS to CMOS</b>					
$V_{IN(1)}$ Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.5 8.0			V V
$V_{IN(0)}$ Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			0.8 2.0	V V
$V_{OUT(1)}$ Logical "1" Output Voltage	$V_{CC} = 5.0V, I_O = -10\mu A$ $V_{CC} = 10V, I_O = -10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$ Logical "0" Output Voltage	$V_{CC} = 5.0V, I_O = +10\mu A$ $V_{CC} = 10V, I_O = +10\mu A$			0.5 1.0	V V
$I_{IN(1)}$ Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
$I_{IN(0)}$ Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
$I_{CC}$ Supply Current	$V_{CC} = 15V$		0.05	300	$\mu A$
Tristate Leakage	$V_{CC} = 15V, V_{OUT} = 0V$ or $15V$			$\pm 3.0$	$\mu A$
<b>CMOS/TTL Interface</b>					
$V_{IN(1)}$ Logical "1" Input Voltage	54C, $V_C = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 2.5$ $V_{CC} - 2.5$			V V
$V_{IN(0)}$ Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$ Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_O = -450\mu A$ 74C, $V_{CC} = 4.75V, I_O = -450\mu A$	$V_{CC} - 0.4$ $V_{CC} - 0.4$			V V
	54C, $V_{CC} = 4.5V, I_O = -2.2mA$ 74C, $V_{CC} = 4.75V, I_O = -2.2mA$	2.4 2.4			V V
$V_{OUT(0)}$ Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_O = +2.2mA$ 74C, $V_{CC} = 4.75V, I_O = +2.2mA$			0.4 0.4	V V
<b>Output Drive (See 54C/74C Family Characteristics Data Sheet)</b>					
$I_{SOURCE}$ Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-14.0	-30.0		mA
$I_{SOURCE}$ Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-36.0	-70.0		mA
$I_{SINK}$ Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	+12.0	+20.0		mA
$I_{SINK}$ Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	+48.0	+70.0		mA

**AC Electrical Characteristics**  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{pd1}$ , $t_{pd0}$ Propagation Delay (Data IN TO OUT)	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$		70	140	ns
	$V_{CC} = 10\text{ V}$ , $C_L = 50\text{ pF}$		35	70	ns
	$V_{CC} = 5.0\text{ V}$ , $C_L = 150\text{ pF}$		90	160	ns
	$V_{CC} = 10\text{ V}$ , $C_L = 150\text{ pF}$		45	90	ns
$t_{IH}$ , $t_{OH}$ Propagation Delay Output Disable to Logic Level (from High Impedance State) (from a Logic Level)	$R_L = 1\text{ k}\Omega$ , $C_L = 50\text{ pF}$				
	$V_{CC} = 5.0\text{ V}$		100	200	ns
	$V_{CC} = 10\text{ V}$		55	110	ns
$t_{H1}$ , $t_{H0}$ Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1\text{ k}\Omega$ , $C_L = 50\text{ pF}$				
	$V_{CC} = 5.0\text{ V}$		100	200	ns
	$V_{CC} = 10\text{ V}$		55	110	ns
$t_{THL}$ , $t_{TLH}$ Transition Time	$V_{CC} = 5.0\text{ V}$ , $C_L = 50\text{ pF}$		50	100	ns
	$V_{CC} = 10\text{ V}$ , $C_L = 50\text{ pF}$		30	60	ns
	$V_{CC} = 5.0\text{ V}$ , $C_L = 150\text{ pF}$		80	160	ns
	$V_{CC} = 10\text{ V}$ , $C_L = 150\text{ pF}$		50	100	ns
$C_{PD}$ Power Dissipation Capacitance (Output Enabled per Buffer) (Output Disabled per Buffer)	(See Note 3)				
			100		pF
$C_{IN}$ Input Capacitance (Any Input)	(See Note 2)				
	$V_{IN} = 0\text{ V}$ , $f = 1\text{ MHz}$ $T_A = 25^\circ\text{C}$		10		pF
$C_O$ (Output Capacitance) (Output Disabled)	$V_{IN} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $T_A = 25^\circ\text{C}$		10		pF

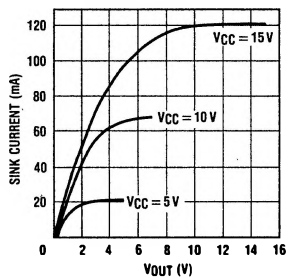
**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Truth Table**

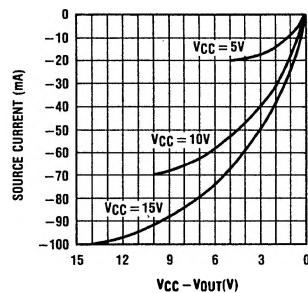
OD1	OD2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	Z
1	0	X	Z
1	1	X	Z

1 = High  
0 = Low  
X = Don't Care  
Z = TRI-STATE®

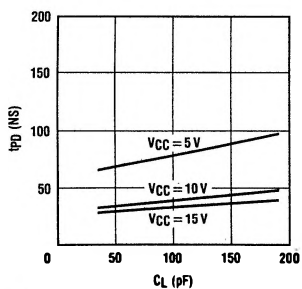
**N-Channel Output Drive  
@ 25°C**



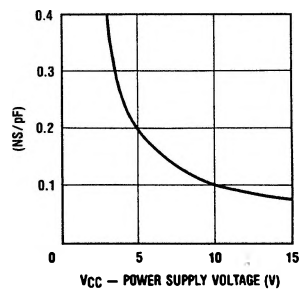
**P-Channel Output Drive  
@ 25°C**



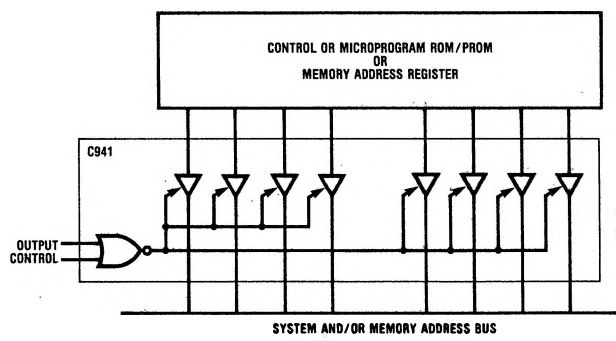
**Propagation Delay vs.  
Load Capacitance**



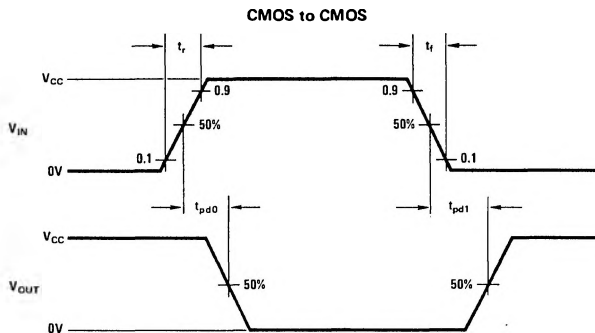
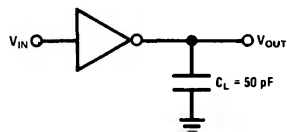
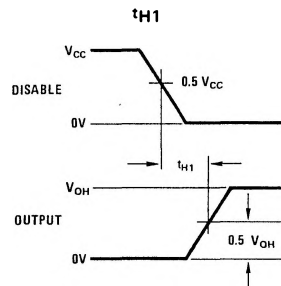
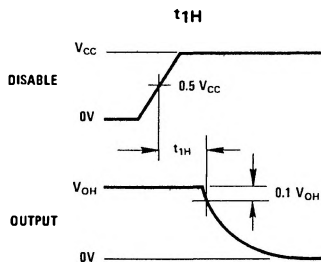
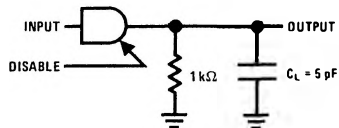
**Δt<sub>PD</sub> per pF of Load  
Capacitance**



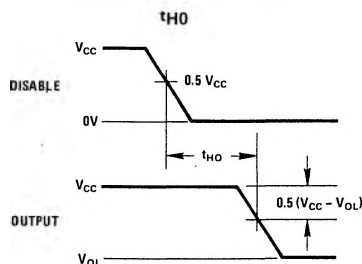
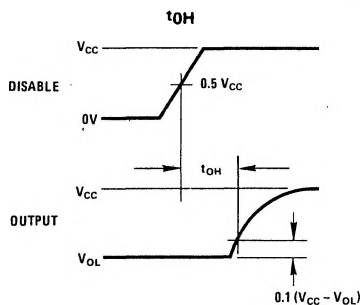
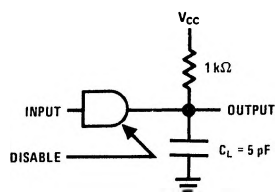
## Applications



## AC Test Circuits and Switching Time Waveforms

 $t_{pd0}$ ,  $t_{pd1}$  $t_{1H}$  and  $t_{1L}$ 

NOTE:  $V_{OH}$  IS DEFINED AS THE DC OUTPUT HIGH VOLTAGE WHEN THE DEVICE IS LOADED WITH A 1 kΩ RESISTOR TO GROUND.

 $t_{0H}$  and  $t_{0L}$ 

NOTE:  $V_{OL}$  IS DEFINED AS THE DC OUTPUT LOW VOLTAGE WHEN THE DEVICE IS LOADED WITH A 1 kΩ RESISTOR TO  $V_{CC}$ .

Note: Delays measured with input  $t_i$ ,  $t_i \leq 20$  ns