

DUAL J-K-MASTER-SLAVE FLIP-FLOP

S54107 N74107

S54107—A,F • N74107—A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S54107A/N74107A J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:
See S5473/N7473 waveform.

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

TRUTH TABLE

LOGIC

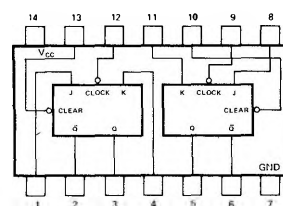
(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	\bar{Q}_n

NOTES:

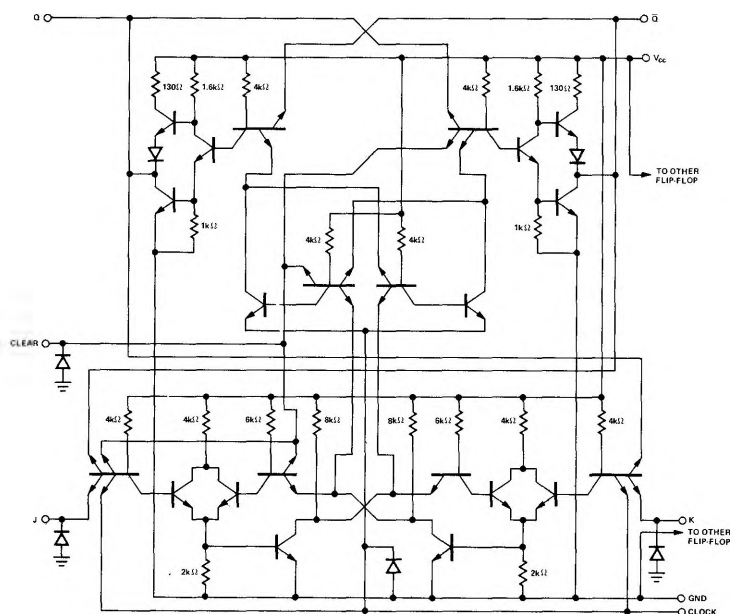
1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

PIN CONFIGURATIONS

A,F PACKAGE



SCHEMATIC (each flip-flop)



NOTE: Component values shown are nominal.

SIGNETICS DIGITAL 54/74 TTL SERIES - S54107 • N74107
RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S54107 Circuits	4.5	5	5.5	V
N74107 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A : S54107 Circuits	-55	25	125	°C
N74107 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N			10	
Width of Clock Pulse, $p(\text{clock})$	20			ns
Width of Clear Pulse, $t_{p(\text{clear})}$	25			ns
Input Setup Time, t_{setup}	$\geq t_{p(\text{clock})}$			
Input Hold Time, t_{hold}	0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}$, $I_{\text{load}} = -400\mu\text{A}$	2.4	3.5		V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}$, $I_{\text{sink}} = 16\text{mA}$		0.22	0.4	V
$I_{in(0)}$ Logical 0 level input current at J or K	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at clear or clock	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J or K	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$			40	μA
	$V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at clear or clock	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$			80	μA
	$V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			1	mA
I_{OS} Short circuit output current†	$V_{CC} = \text{MAX}$, $V_{in} = 0$	S54107 -20 N74107 -18		-57 -57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, $V_{in} = 5\text{V}$		20	40	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{clock} Maximum clock frequency	$C_L = 15\text{pF}$, $R_L = 400\Omega$	15	20		MHz
t_{pd1} Propagation delay time to logical 1 level from clear to output	$C_L = 15\text{pF}$, $R_L = 400\Omega$		16	25	ns
t_{pd0} Propagation delay time to logical 0 level from clear to output	$C_L = 15\text{pF}$, $R_L = 400\Omega$		25	40	ns
t_{pd1} Propagation delay time to logical 1 level from clock to output	$C_L = 15\text{pF}$, $R_L = 400\Omega$	10	16	25	ns
t_{pd0} Propagation delay time to logical 0 level from clock to output	$C_L = 15\text{pF}$, $R_L = 400\Omega$	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

† Not more than one output should be shorted at a time.