

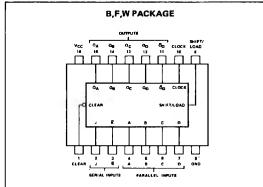
## 4-BIT PARALLEL-ACCESS | S54195 SHIFT REGISTER

S54195-B,F,W • N74195-B,F

# N74195

DIGITAL 54/74 TTL SERIES

#### PIN CONFIGURATIONS



#### DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear.

The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction  $\Omega_A$  toward  $\Omega_D$ ) Parallel loading is accomplished by applying the 4 bits of data and taking the shift/load control input low. The data are loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode are entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive require-ments to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The S54195 is characterized for operation over the full military temperature range of -55° C to 125° C; the N74195 is characterized for operation from 0°C to 70°C.

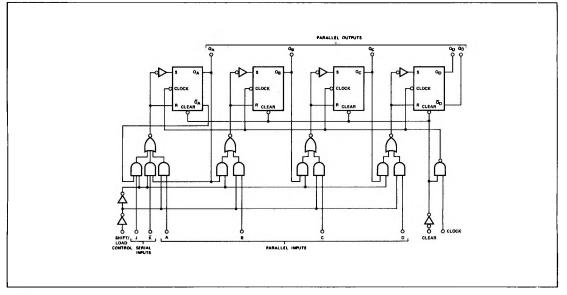
#### TRUTH TABLE

Input	s at t <sub>n</sub>	Outputs at t <sub>n+1</sub>					
J	ĸ	QA	QB	QC	٥ <sub>D</sub>	۵ <sub>۵</sub>	
L	н	Q <sub>An</sub>	Q <sub>An</sub>	0.Bn	O <sub>Cn</sub>	ācn	
L	L	î.	QAn	QBn	QCn	QCn	
н	н	н	QAn	QBn	QCn	Q <sub>Cn</sub>	
н	L	ā <sub>An</sub>	QAn	QBn	QCn	0 <sub>Cn</sub>	

H = High Level, L = Low Level NOTES A. t<sub>n</sub> = bit time before clock pulse B.  $t_{n+1}^{(i)}$  = bit time after clock pulse

C.  $Q_{An}$  = state of  $Q_A$  at  $t_n$ 

#### LOGIC DIAGRAM



#### **RECOMMENDED OPERATING CONDITIONS**

	\$54195		N74195				
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply Voltage V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	v
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Input Clock Frequency, fclock	0		30	0		30	MHz
Width of Clock Input Pulse, two clock)	16			16		1	ns
Width of Clear Input Pulse, tw(clear)	12			12			n
Setup Time, tsetup: Shift/load	25			25			
Serial and parallel data	15			15			n
Clear inactive-state	25			25			
Shift/Load Release Time, t <sub>release</sub>			10			10	ns
Serial and Parallel Data Hold Time, thold	0			0			ns
Operating Free-Air Temperature, TA	-55		125	0		70	°C

#### ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS •			MIN	ТҮР**	мах	UNIT
v <sub>iH</sub>	High-level input voltage				2			v
VIL	Low-level input voltage						0.8	v
4	Input clamp voltage	$V_{CC} = MIN$	I <sub>I</sub> = -12mA				-1.5	v
v <sub>он</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8V,	V <sub>IH</sub> = 2V, I <sub>OH</sub> = -800µА		2.4			v
V <sub>OL</sub>	Low-level output voltage	$V_{CC} = MIN,$ $V_{IL} = 0.8V,$	V <sub>IH</sub> = 2V, I <sub>OL</sub> = 16mA				0.4	v
4	Input current at maximum input voltage	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5V				1	mA
Чн	High-level input current	V <sub>CC</sub> = MAX, V <sub>CC</sub> = MAX,	V <sub>1</sub> = 2.4V				40	μΑ
Ψ <u>Γ</u>	Low-level input current	V <sub>CC</sub> = MAX,	Vi = 0.4V				-1.6	mA
los	Short-circuit output current <sup>†</sup>	V <sub>CC</sub> = MAX	•	S54195 N74195	-20 -18		-57 -57	mA
<sup>I</sup> cc	Supply current	V <sub>CC</sub> = MAX,	See Note			39	63	mA

### SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	ТҮР	MAX	UNIT
f <sub>max</sub>	Maximum input clock frequency			30	39		MHz
<sup>t</sup> PHL	Propagation delay time, high-to- low-level output from clear				19	30	ns
<sup>t</sup> ₽LH	Propagation delay time, low-to- high-level output from clock	C <sub>L</sub> = 15pF,	RL = 400Ω	6	14	22	ns
<sup>t</sup> PHL	Propagation delay time, high-to- low-level output from clock			7	17	26	ns

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

\*\* All typical values are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

1 Not more than one output should be shorted at a time.

NOTE With all outputs open, shift/load grounded, and 4.5V applied to the J,R, and data inputs, I<sub>CC</sub> is measured by applying a momentary ground, followed by 4.5V, to clear, and then applying a momentary ground, followed by 4.5V, to clock.