## DESCRIPTION

The 54/7426 Quad 2-Input NAND Gate features standard TTL inputs with high voltage ( 15 volts) open collector outputs for interface with MOS, lamps or relays.

SCHEMATIC (each gate)


PIN CONFIGURATION


## RECOMMENDED OPERATING CONDITIONS

|  | S5426 |  |  | N7426 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Output Voltage, $\mathrm{V}_{\mathrm{OH}}$ |  |  | 15 |  |  | 15 | $V$ |
| Low-Level Output Current, I OL |  |  | 16 |  |  | 16 | mA |
| Operating Free-Air Temperature Range, $\mathrm{T}_{\mathbf{A}}$ | -55 | 25 | 125 | 0 | 25 | 70 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

|  | PARAMETER | TEST CONDITIONS* | MIN | TYP** | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  | 2 |  |  | V |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}, \mathrm{V}_{\text {IL }}=0.8 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=1 \mathrm{~mA}$ | 15 |  |  | V |
| ${ }^{\mathrm{I}} \mathrm{OH}$ | High-level output current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}, \mathrm{V}_{\text {IL }}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{OH}}=12 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}, \mathrm{V}_{\text {IH }}=2 \mathrm{~V}, \mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA}$ |  |  | 0.4 | V |
|  | High-level input current | $\mathrm{V}_{C C}=\mathrm{MAX}, \mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 40 | $\mu \mathrm{A}$ |
| IH | (each input) | $V_{C C}=M A X, V_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $I_{\text {IL }}$ | Low-level input current (each input) | $V_{C C}=\mathrm{MAX}, \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -1.6 | mA |
| ${ }^{1} \mathrm{CCH}$ | Supply current, high-level output | $V_{C C}=M A X, V_{1}=0$ |  | 4 | 8 | mA |
| ${ }^{1} \mathrm{CCL}$ | Supply current, low-level output | $V_{C C}=M A X, V_{1}=5 V$ |  | 12 | 22 | mA |

SIGNETICS DIGITAL 54/74 TTL SERIES - S5426• N7426

| PARAMETER |  | TEST CONDITIONS |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {P PLH }}$ | Propagation delay time, low-to-high-level output | $C_{L}=15 \mathrm{pF}$, | $\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$ |  | 16 | 24 | ns |
| ${ }^{\text {tPHL }}$ | Propagation delay time high-to-low-level output | $C_{L}=15 \mathrm{pF}$, | $R_{L}=1 \mathrm{k} \Omega$ |  | 11 | 17 | ns |

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at $V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}$.

