# DUAL J-K MASTER-SLAVE FLIP-FLOP | \$5473

N7473

\$5473-A,F,W • N7473-A,F

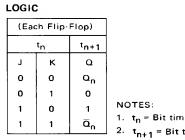
# DIGITAL 54/74 TTL SERIES

### DESCRIPTION

The S5473/N7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

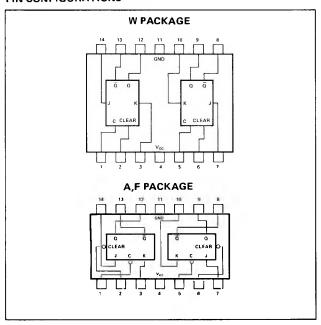
- 1. Isolate slave from master
- 2. Enter information from J and K inputs to master
- 3. Disable J and K inputs
- 4. Transfer information from master to slave.

#### **TRUTH TABLE**

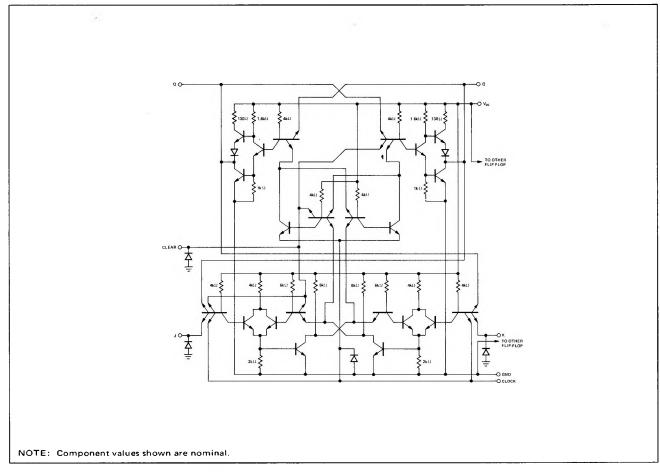


- 1.  $t_n = Bit time before clock pulse.$
- 2. t<sub>n+1</sub> = Bit time after clock pulse.

## PIN CONFIGURATIONS



#### SCHEMATIC (each flip-flop)



### RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V <sub>CC</sub> : S5473 Circuits	4.5	5	5.5	V
N7473 Circuits	4.75	5	5.25	l v
Operating Free-Air Temperature Range, T <sub>A</sub> : S5473 Circuits	-55	25	125	°c
N7473 Circuits	0	25	70	°c
Normalized Fan-Out from each Output, N			10	
Width of Clock Pulse, tp(clock)	20			ns
Width of Clear Pulse, total and the control of the	25			ns
Input Setup Time, t <sub>setup</sub>	≥tp(Clock)			
Input Hold Time, thold	0			

# ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	T	EST CONDITIONS*		MIN	TYP**	MAX	UNIT
V <sub>in(1)</sub>	Input voltage required to ensure logical 1 at any input terminal	V <sub>CC</sub> = MIN			2			V
V <sub>in(0)</sub>	Input voltage required to ensure logical 0 at any input terminal	V <sub>CC</sub> = MIN,			-		8.0	V
$V_{out(1)}$	Logical 1 output voltage	V <sub>CC</sub> = MIN,	$I_{load} = -400\mu A$		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V <sub>CC</sub> = MIN,	Isink = 16mA			0.22	0.4	V
<sup>1</sup> in(0)	Logical 0 level input current at J or K	V <sub>CC</sub> = MAX,	$V_{in} = 0.4V$				-1.6	mA
l <sub>in(0)</sub>	Logical 0 level input current at clear or clock	V <sub>CC</sub> = MAX,	$V_{in} = 0.4V$				-3.2	mA
lin(1)	Logical 1 level input current at J or K	V <sub>CC</sub> = MAX, V <sub>CC</sub> = MAX,	V <sub>in</sub> = 2.4V V <sub>in</sub> = 5.5V				40 1	μA mA
lin(1)	Logical 1 level input current at clear or clock	V <sub>CC</sub> = MAX, V <sub>CC</sub> = MAX,	V <sub>in</sub> = 2.4V V <sub>in</sub> = 5.5V				<b>80</b> 1	μA mA
los	Short circuit output current <sup>†</sup>	V <sub>CC</sub> = MAX,	V <sub>in</sub> = 0	S5473 N7473	-20 -18		-57 -57	mA
<sup>l</sup> cc	Supply current	V <sub>CC</sub> = MAX,	V <sub>in</sub> = 5V			20	40	mA

# SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
fclock	Maximum clock frequency	C <sub>L</sub> = 15pF,	R <sub>L</sub> = 400Ω	15	20		MHz
<sup>t</sup> pd1	Propagation delay time to logical 1 level from clear to output	C <sub>L</sub> = 15pF,	R <sub>L</sub> = 400Ω		16	25	ns
<sup>t</sup> pd0	Propagation delay time to logical 0 level from clear to output	C <sub>L</sub> = 15pF,	R <sub>L</sub> = 400Ω		25	40	ns
<sup>t</sup> pd1	Propagation delay time to logical 1 level from clock to output	C <sub>L</sub> = 15pF,	R <sub>L</sub> = 400Ω	10	16	25	ns
<sup>t</sup> pd0	Propagation delay time to logical 0 level from clock to output	C <sub>L</sub> = 15pF,	R <sub>L</sub> = 400Ω	10	25	40	ns

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
Not more than one output should be shorted at a time.