# DUAL J-K MASTER-SLAVE FLIP.FLOP <br> S5473-A,F,W • N7473-A,F 

DIGITAL 54/74 TTL SERIES
PIN CONFIGURATIONS


DESCRIPTION
The S5473/N7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from $J$ and $K$ inputs to master
3. Disable $J$ and $K$ inputs
4. Transfer information from master to slave.

## TRUTH TABLE

LOGIC

| (Each Flip- Flop) |  |  |
| :---: | :---: | :---: |
| $t_{n}$ |  | $t_{n+1}$ |
| $J$ | $K$ | $Q$ |
| 0 | 0 | $a_{n}$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\bar{o}_{n}$ |

NOTES:

1. $t_{n}=$ Bit time before clock pulse.
2. $t_{n+1}=$ Bit time after clock pulse.

SCHEMATIC (each flip-flop)


## RECOMMENDED OPERATING CONDITIONS

|  | MIN | NOM | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| Supply Voltage V CC : S5473 Circuits | 4.5 | 5 | 5.5 | V |
| N7473 Circuits | 4.75 | 5 | 5.25 | V |
| Operating Free-Air Temperature Range, $\mathbf{T A}_{\text {A }}$ : $\quad$ S5473 Circuits | -55 | 25 | 125 | ${ }^{\circ} \mathrm{C}$ |
| N7473 Circuits | 0 | 25 | 70 | ${ }^{\circ} \mathrm{C}$ |
| Normalized Fan-Out from each Output, N |  |  | 10 |  |
| Width of Clock Pulse, $\mathrm{t}_{\text {p(clock) }}$ | 20 |  |  | ns |
| Width of Clear Pulse, $t_{\text {piclear) }}$ | 25 |  |  | ns |
| Input Setup Time, $\mathrm{t}_{\text {setup }}$ | $\geqslant t_{\text {p }}$ (Clock) |  |  |  |
| Input Hold Time, ${ }_{\text {hold }}$ | 0 |  |  |  |

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS* |  |  | MIN | TYP** | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $v_{\text {in(1) }}$ | Input voltage required to ensure logical 1 at any input terminal | $V_{C C}=$ MIN |  |  | 2 |  |  | V |
| $V_{\text {in }}(0)$ | Input voltage required to ensure logical 0 at any input terminal | $V_{C C}=$ MIN, |  |  |  |  | 0.8 | V |
| $V_{\text {out (1) }}$ | Logical 1 output voltage | $V_{C C}=$ MIN, | $I_{\text {load }}=-400 \mu \mathrm{~A}$ |  | 2.4 | 3.5 |  | V |
| $\mathrm{V}_{\text {out (0) }}$ | Logical 0 output voltage | $V_{C C}=$ MIN | $I_{\text {sink }}=16 \mathrm{~mA}$ |  |  | 0.22 | 0.4 | $\checkmark$ |
| $1 \mathrm{in}(0)$ | Logical $O$ level input current at J or K | $V_{C C}=M A X$, | $V_{\text {in }}=0.4 \mathrm{~V}$ |  |  |  | -1.6 | mA |
| $I_{\text {in }}(0)$ | Logical $O$ level input current at clear or clock | $V_{C C}=M A X$, | $\mathrm{V}_{\text {in }}=0.4 \mathrm{~V}$ |  |  |  | -3.2 | mA |
| $1 \mathrm{in}(1)$ | Logical 1 level input current at J or K | $\begin{aligned} & V_{C C}=M A X, \\ & V_{C C}=M A X, \end{aligned}$ | $\begin{aligned} & V_{\text {in }}=2.4 \mathrm{~V} \\ & V_{\text {in }}=5.5 \mathrm{~V} \end{aligned}$ |  |  |  | $\begin{array}{r} 40 \\ 1 \end{array}$ | $\mu \mathrm{A}$ mA |
| $1 \mathrm{in}(1)$ | Logical 1 level input current at clear or clock | $\begin{aligned} & V_{C C}=M A X, \\ & V_{C C}=M A X, \end{aligned}$ | $\begin{aligned} & V_{\text {in }}=2.4 \mathrm{~V} \\ & V_{\text {in }}=5.5 \mathrm{~V} \end{aligned}$ |  |  |  | $80$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| ${ }^{\prime} \mathrm{OS}$ | Short circuit output current ${ }^{\dagger}$ | $V_{C C}=M A X$, | $V_{\text {in }}=0$ | $\begin{aligned} & \text { S5473 } \\ & \text { N7473 } \end{aligned}$ | $\begin{aligned} & -20 \\ & -18 \end{aligned}$ |  | $\begin{aligned} & -57 \\ & -57 \end{aligned}$ | mA |
| ${ }^{1} \mathrm{Cc}$ | Supply current | $V_{C C}=M A X$, | $\mathrm{V}_{\text {in }}=5 \mathrm{~V}$ |  |  | 20 | 40 | mA |

SWITCHING CHARACTERISTICS, $V_{C C}=5 V, T_{A}=25^{\circ} \mathrm{C}, \mathbf{N}=10$

| PARAMETER |  | TEST CONDITIONS |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {f clock }}$ | Maximum clock frequency | $C_{L}=15 \mathrm{pF}$, | $R_{L}=400 \Omega$ | 15 | 20 |  | MHz |
| ${ }^{\text {t }}$ pd1 | Propagation delay time to logical 1 level from clear to output | $C_{L}=15 \mathrm{pF}$, | $R_{L}=400 \Omega$ |  | 16 | 25 | ns |
| ${ }^{t} \mathrm{pdO}$ | Propagation delay time to logical 0 level from clear to output | $C_{L}=15 \mathrm{pF}$, | $R_{L}=400 \Omega$ |  | 25 | 40 | ns |
| ${ }^{t} \mathrm{pd} 1$ | Propagation delay time to logical 1 level from clock to output | $C_{L}=15 \mathrm{pF}$, | $R_{L}=400 \Omega$ | 10 | 16 | 25 | ns |
| ${ }^{\text {pdo }}$ | Propagation delay time to logical 0 level from clock to output | $C_{L}=15 p F$, | $R_{L}=400 \Omega$ | 10 | 25 | 40 | ns |

[^0]
[^0]:    * For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
    * All typical values are at $V_{C C}=5 V, T_{A}=25^{\circ} \mathrm{C}$.
    $t$ Not more than one output should be shorted at a time.

