

DIVIDE-BY-TWELVE COUNTER | \$5492 (DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

\$5492-A,F,W • N7492-A,F

N7492

DESCRIPTION

The S5492/N7492 is a high-speed monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flops outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

- 1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous division of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table.
- 2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously, frequency division of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

The S5492/N7492 is completely compatible with Series 54 and Series 74 logic families. Average power dissipation is 155mW.

OUTPUT

0 0 1

0 1 0 0

0 1 0 1

DC ΒA

0 0 0 0

0

TRUTH TABLE (See Notes 1 and 2)

COUNT

0

1

2 0 0 1 0

3 0 0 1 1

4

5



SCHEMATIC DIAGRAM



DIGITAL 54/74 TTL SERIES

PIN CONFIGURATIONS



1. Output A connected to input B.

2. To reset all outputs to logical 0,

both R0(1) and R0(2) inputs

must be at logical 1.

NOTES:

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	МАХ	UNIT
Supply Voltage V _{CC} : S5492 Circuits	4.5	5	5.5	v (
N7492 Circuits	4.75	5	5.25	V V
Operating Free-Air Temperature Range, TA: S5492 Circuits	-55	25	125	°C
N7492 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N			10	
Width of Input Count Pulse, to (in)	50			ns
Width of Reset Pulse, t _p (reset)	50			ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER Input voltage required to ensure logical 1 at any input terminal	т	TEST CONDITIONS *		MIN	TYP**	MAX	UNIT
V _{in(1)}		V _{CC} = MIN			2			Y
V _{in(0)}	Input voltage required to ensure logical 0 at any input terminal	V _{CC} = MIN					0.8	v
V _{out(1)}	Logical 1 output voltage	V _{CC} = MIN,	load = -400µA		2.4			v
V _{out} (0)	Logical 0 output voltage	V _{CC} = MIN,	I _{sink} = 16mA				0.4	v
lin(1)	Logical 1 level input current at $R_{O(1)}$ or $R_{O(2)}$ inputs	V _{CC} = MAX, V _{CC} = MAX,	V _{in} = 2.4V V _{in} = 5.5V				40 1	μA mA
lin(1)	Logical 1 level input current at input A	V _{CC} = MAX, V _{CC} = MAX,	V _{in} = 2.4V V _{in} = 5.5V				80 1	μA mA
lin(1)	Logical 1 level input current at input BC	V _{CC} = MAX, V _{CC} = MAX,	V _{in} = 2.4V V _{in} = 5.5V				160 1	μA mA
lin(0)	Logical O level input current at R _{O(1)} or R _{O(2)} inputs	$V_{CC} = MAX,$	V _{in} = 0.4V				-1.6	mA
lin(0)	Logical 0 level input current input A	V _{CC} = MAX,	V _{in} = 0.4V				-3.2	mA
¹ in(0)	Logical O level input current at input BC	∨ _{СС} - мах,	V _{in} = 0.4V				-6.4	mA
los	Short circuit output current †	V _{CC} = MAX,	V _{out} = 0	S5492 N7492	-20 -18		-57 -57	mA mA
'cc	Supply current	V _{CC} = MAX,	V _{in} = 4.5V	S5492 N7492		31 31	44 51	mA mA

SWITCHING CHARACTERISTICS, VCC = 5V, TA = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	түр	MAX	UNIT
i _{max}	Maximum frequency of input count pulses	C _L = 15pF,	R _L = 400Ω	10	18		MHz
^t pd 1	Propagation delay time to logical 1 level from input count pulse to output D	C _L = 15pF,	R լ - 400Ω		60	100	ns
^t pd0	Propagation delay time to logical 0 level from input count pulse to output D	C _L = 15pF,	א ן = 400 Ω		60	100	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC}^{-5} 5V, $T_A = 25^{\circ}C$. † Not more than one output should be shorted at a time.