DIGITAL 54/74 TTL SERIES

## PIN CONFIGURATIONS

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock puise also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of $J$ and $K$ inputs must not be allowed to change when the clock pulse is in a high state.

TRUTH TABLE

## LOGIC

| (Each Flip-Flop) |  |  |
| :---: | :---: | :---: |
| $t_{n}$ |  | $t_{n+1}$ |
| $J$ | $K$ | $Q$ |
| 0 | 0 | $Q_{n}$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $Z_{n}$ |

NOTES:

1. $t_{\mathbf{n}}=$ bit time before clock pulse
2. $t_{n+1}=$ bit time after clock pulse

## POSITIVE LOGIC

Low input to clear sets $\mathbf{Q}$ to logical 0
Clear is independent of clock


## CLOCK WAVEFORM



SCHEMATIC (each flip-flop)


NOTE: Component values shown are nominal.

## RECOMMENDED OPERATING CONDITIONS

|  | MIN | NOM | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| Supply Voltage $\mathrm{V}_{\text {CC }}$ : S54H73 Circuits | 4.5 | 5 | 5.5 | V |
| N74H73 Circuits | 4.75 | 5 | 5.25 | V |
| Operating Free-Air Temperature Range, $\mathrm{T}_{\mathrm{A}}$ : S 54 H 73 Circuits | -55 | 25 | 125 | ${ }^{\circ} \mathrm{C}$ |
| N74H73 Circuits | 0 | 25 | 70 | ${ }^{\circ} \mathrm{C}$ |
| Normalized Fan-Out from each Output, N |  |  | 10 |  |
| Width of Clock Pulse, $\mathrm{t}_{\text {p(clock) }}$ | 12 |  |  | ns |
| Width of Clear Pulse, $\mathrm{t}_{\text {p(clear) }}$ | 16 |  |  | ns |
| Input Setup Time, tsetup (See above) | $\geqslant t_{\mathrm{p}(\text { clock })}$ |  |  |  |
| Input Hold Time, thold | $0$ |  |  |  |

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS** |  | MIN | TYP ${ }^{\text {t }}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{i n}(1)$ | Input voltage required to ensure logical 1 at any input terminal | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | 2 |  |  | V |
| $V_{\text {in(0) }}$ | Input voltage required to ensure logical 0 at any input terminal | $V_{C C}=$ MIN |  |  |  | 0.8 | V |
| $V_{\text {out (1) }}$ | Logical 1 output voltage | $V_{\text {CC }}=$ MIN, | $I_{\text {load }}=-500 \mu \mathrm{~A}$ | 2.4 |  |  | $v$ |
| $V_{\text {out (0) }}$ | Logical 0 output voltage | $V_{C C}=$ MIN, | $I_{\text {sink }}=20 \mathrm{~mA}$ |  |  | 0.4 | $\checkmark$ |
| $\operatorname{lin}(0)$ | Logical 0 level input current at J, K, or clock | $V_{C C}=$ MAX , | $V_{\text {in }}=0.4 \mathrm{~V}$ |  |  | -2 | mA |
| I in (0) | Logical 0 level input current at clear | $V_{C C}=M A X$, | $\mathrm{V}_{\text {in }}=0.4 \mathrm{~V}$ |  |  | -4 | mA |
| $1 \mathrm{in}(1)$ | Logical 1 level input current at Jor K . | $\begin{aligned} & V_{C C}=M A X, \\ & V_{C C}=M A X, \end{aligned}$ | $\begin{aligned} & V_{i n}=2.4 \mathrm{~V} \\ & V_{i n}=5.5 \mathrm{~V} \end{aligned}$ |  |  | 50 1 | $\begin{aligned} & \mu A \\ & m A \end{aligned}$ |
| $\operatorname{lin}(1)$ | Logical 1 level input current at clock | $\begin{aligned} & V_{C C}=M A X, \\ & V_{C C}=M A X, \end{aligned}$ | $\begin{aligned} & V_{i n}=2.4 \mathrm{~V} \\ & V_{i n}=5.5 \mathrm{~V} \end{aligned}$ |  |  | 50 1 | $\mu \mathrm{A}$ mA |
| Iin(1) | Logical 1 level input current at clear | $\begin{aligned} & V_{C C}=M A X, \\ & V_{C C}=M A X, \end{aligned}$ | $\begin{aligned} & V_{i n}=2.4 \mathrm{~V} \\ & V_{i n}=5.5 \mathrm{~V} \end{aligned}$ |  |  | $\begin{array}{r} 100 \\ 1 \end{array}$ | $\begin{aligned} & \mu A \\ & m A \end{aligned}$ |
| ${ }^{1} \mathrm{OS}$ | Short circuit output current"* | $V_{\text {CC }}=$ MAX , | $v_{\text {in }}=0$ | -40 |  | -100 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 32 | 50 | mA |

SWITCHING CHARACTERISTICS, $V_{C C}=5 V, T_{A}=25^{\circ} \mathrm{C}, \mathrm{N}=10$

| PARAMETER |  | TEST CONDITIONS |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $f_{\text {clock }}$ | Maximum clock frequency | $C_{L}=25 p F$, | $R_{L}=280 \Omega$ | 25 | 30 |  | MHz |
| ${ }^{\text {tpd }} 1$ | Propagation delay time to logical 1 level from clear to output | $C_{L}=25 p F$, | $R_{L}=280 \Omega$ |  | 6 | 13 | ns |
| ${ }^{\text {tpdo }}$ | Propagation delay time to logical $O$ level from clear to output | $C_{L}=25 \mathrm{pF}$, | $R_{L}=280 \Omega$ |  | 12 | 24 | ns |
| ${ }^{\text {tpd }} \mathbf{1}$ | Propagation delay time to logical 1 level from clock to output | $C_{L}=25 p F$, | $\mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 16 | 21 | ns |
| ${ }^{\mathbf{t}} \mathrm{pdO}$ | Propagation delay time to logical 0 level from clock to output | $C_{L}=25 p F$, | $\mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 22 | 27 | ns |

[^0]
[^0]:    - For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
    * Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.
    t All typical values are at $V_{C C}=5 \mathrm{~V}, \mathrm{~T}_{A}=26^{\circ} \mathrm{C}$

