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December 2010

# NC7SV32 TinyLogic<sup>®</sup> ULP-A 2-Input OR Gate

### **Features**

- 0.9V to 3.6V V<sub>CC</sub> Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at Vcc from 0.9V to 3.6V
- Extremely High Speed t<sub>PD</sub>
  - 1.0ns: Typical for 2.7V to 3.6V V<sub>CC</sub>
  - 1.2ns: Typical for 2.3V to 2.7V V<sub>CC</sub>
  - 2.0ns: Typical for 1.65V to 1.95V V<sub>CC</sub>
  - 3.2ns: Typical for 1.4V to 1.6V V<sub>CC</sub>
  - 6.0ns: Typical for 1.1V to 1.3V V<sub>CC</sub>
  - 13.0ns: Typical for 0.9V V<sub>CC</sub>
- Power-Off High-Impedance Inputs and Outputs
- High Static Drive (I<sub>OH</sub>/I<sub>OL</sub>)
  - ±24mA at 3.00V V<sub>CC</sub>
  - ±18mA at 2.30V V<sub>CC</sub>
  - ±6mA at 1.65V V<sub>CC</sub>
  - ±4mA at 1.4V V<sub>CC</sub>
  - $\pm 2$ mA at 1.1V V<sub>CC</sub>
  - $\pm 0.1$ mA at 0.9V V<sub>CC</sub>
- Uses Proprietary Quiet Series<sup>™</sup> Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak<sup>™</sup> Packages
- Ultra-Low Dynamic Power

### Description

The NC7SV32 is a single two-input OR gate from Fairchild's Ultra-Low Power (ULP-A) Series of TinyLogic $^{\circ}$ . ULP-A is ideal for applications that require extreme high speed, high drive, and low power. This product is designed for a wide low-voltage operating range (0.9V to 3.6V V $_{\rm CC}$ ) and applications that require more drive and speed than the TinyLogic $^{\circ}$  ULP series, but still offer best-in-class, low-power operation.

The NC7SV32 is uniquely designed for optimized power and speed and is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

### **Ordering Information**

Part Number	Top Mark	Package	Packing Method
NC7SV32P5X	V32	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SV32L6X	G6	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7SV32FHX	G6	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

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MicroPak™ and Quiet Series™ are trademarks of Fairchild Semiconductor Corporation.

### **Battery Life**

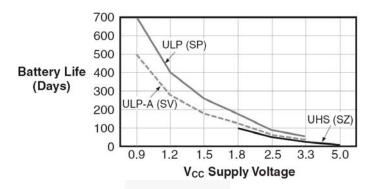
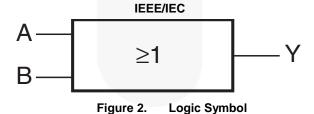


Figure 1. Battery Life vs. V<sub>CC</sub> Supply Voltage

#### Notes:

- TinyLogic<sup>®</sup> ULP and ULP-A with up to 50% less power consumption can extend battery life significantly. Battery Life = (V<sub>battery</sub>•I<sub>battery</sub>•.9)/(P<sub>device</sub>)/24hrs/day where, P<sub>device</sub> = (I<sub>CC</sub>• V<sub>CC</sub>) + (C<sub>PD</sub>+ C<sub>L</sub>) • V<sub>CC2</sub>• f.
- 2. Assumes ideal 3.6V Lithium lon battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with  $C_L$  = 15pF load.

### **Connection Diagram**



### **Pin Configurations**

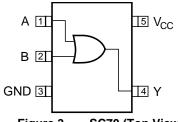


Figure 3. SC70 (Top View)

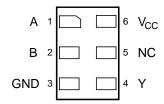


Figure 4. MicroPak™ (Top Through View)

### **Pin Definitions**

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	A	Input
2	2	В	Input
3	3	GND	Ground
4	4	Υ	Output
	5	NC	No Connect
5	6	Vcc	Supply Voltage

### **Function Table**

Inp	outs	Output
Α	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	Н

H = HIGH Logic Level

L = LOW Logic Level

### **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Para	ımeter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	DC Input Voltage		-0.5	4.6	V
\/	DC Output Valtage	HIGH or LOW State <sup>(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	W
V <sub>OUT</sub>	DC Output Voltage	V <sub>CC</sub> =0V	-0.5	4.6	V
I <sub>IK</sub>	DC Input Diode Current	$V_{IN} < 0V$		-50	mA
	D0.0 + + D1. + O	V <sub>OUT</sub> < 0V		-50	
l <sub>OK</sub>	DC Output Diode Current	$V_{OUT} > V_{CC}$		+50	mA
I <sub>OH</sub> /I <sub>OL</sub>	DC Output Source/Sink Curren	t		±50	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current per	Supply Pin		±50	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
TJ	Junction Temperature Under B	ias	\(	+150	°C
TL	Junction Lead Temperature, So	oldering 10 Seconds		+260	°C
		SC70-5		150	
$P_{D}$	Power Dissipation at +85°C	MicroPak™-6		130	mW
		MicroPak2™-6		120	
FCD	Human Body Model, JEDEC:JE	SD22-A114		4000	\/
ESD	Charge Device Model, JEDEC:JESD22-C1			2000	V

#### Note:

3. IO absolute maximum rating must be observed.

### **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
V <sub>CC</sub>	Supply Voltage		0.9	3.6	V	
V <sub>IN</sub>	Input Voltage		0	3.6	V	
Vout	Output Voltage	V <sub>CC</sub> =0V	0	3.6	V	
VOUT	Output Voltage	HIGH or LOW State	0	V <sub>cc</sub>	V	
		V <sub>CC</sub> =3.0V to 3.6V		±24		
		V <sub>CC</sub> =2.3V to 3.6V		±18		
1 /1	Output Current in 1 //	V <sub>CC</sub> =1.65V to 1.95V		±6	mA	
I <sub>OH</sub> /I <sub>OL</sub>	Output Current in I <sub>OH</sub> /I <sub>OL</sub>	V <sub>CC</sub> =1.4V to 1.6V		±4		
		V <sub>CC</sub> =1.1V to 1.3V		±2		
		V <sub>CC</sub> =0.9V		±0.1		
$T_A$	Operating Temperature, Free Air		-40	+85	°C	
Δt/ΔV	Minimum Input Edge Rate	V <sub>IN</sub> =0.8V to 2.0, V <sub>CC</sub> =3.0V		10	ns/V	
		SC70-5		425		
$\theta_{JA}$	Thermal Resistance	MicroPak™-6		500	°C/W	
		MicroPak2™-6		560		

#### Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

### **DC Electrical Characteristics**

0		.,	0 1111	T <sub>A</sub> =2	5°C	T <sub>A</sub> =-40	to 85°C	
Symbol	Parameter	V <sub>cc</sub>	Conditions	Min.	Max.	Min.	Max.	Units
		0.90		.65 x V <sub>CC</sub>		.65 x V <sub>CC</sub>		
		$1.10 \le V_{CC} \le 1.30$		.65 x V <sub>CC</sub>		.65 x V <sub>CC</sub>		
\ /	HIGH Level Input	$1.40 \le V_{CC} \le 1.60$		.65 x V <sub>CC</sub>		.65 x V <sub>CC</sub>		.,
$V_{IH}$	Voltage	$1.65 \le V_{CC} \le 1.95$		.65 x V <sub>CC</sub>		.65 x V <sub>CC</sub>		V
		$2.30 \leq V_{CC} \leq 2.70$		1.6		1.6		
		$2.70 \leq V_{CC} \leq 3.60$		2.0		2.0		
		0.90			.35 x V <sub>CC</sub>		.35 x V <sub>CC</sub>	
		$1.10 \le V_{CC} \le 1.30$			.35 x V <sub>CC</sub>		.35 x V <sub>CC</sub>	
\ /	LOW Level Input	$1.40 \leq V_{CC} \leq 1.60$			.35 x V <sub>CC</sub>		.35 x V <sub>CC</sub>	V
$V_{IL}$	Voltage	$1.65 \leq V_{CC} \leq 1.95$			.35 x V <sub>CC</sub>		.35 x V <sub>CC</sub>	V
		$2.30 \leq V_{CC} \leq 2.70$			0.7		0.7	
		$2.70 \leq V_{CC} \leq 3.60$			0.8		0.8	
7/		0.90		V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		
		$1.10 \le V_{CC} \le 1.30$		V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1		
- /-		$1.40 \le V_{CC} \le 1.60$	100	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
		$1.65 \le V_{CC} \le 1.95$	I <sub>OH</sub> =-100μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
		$2.30 \leq V_{CC} \leq 2.70$		V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
		$2.70 \leq V_{CC} \leq 3.60$		V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
		$1.10 \le V_{CC} \le 1.30$	I <sub>OH</sub> =-2mA	.75 x V <sub>CC</sub>		.75 x V <sub>CC</sub>		
$V_{OH}$	HIGH Level Output Voltage	$1.40 \leq V_{CC} \leq 1.60$	I <sub>OH</sub> =-4mA	.75 x V <sub>CC</sub>		.75 x V <sub>CC</sub>		V
	Voltage	$1.65 \le V_{CC} \le 1.95$	I <sub>OH</sub> =-6mA	1.25		1.25		
		$2.30 \leq V_{CC} \leq 2.70$	IOH=-OITIA	2.00		2.00		
		$2.30 \leq V_{CC} \leq 2.70$	- 12mΛ	1.8		1.8		
		2.70≤ V <sub>CC</sub> ≤ 3.60	I <sub>OH</sub> =-12mA	2.2		2.2		
		$2.30 \leq V_{CC} \leq 2.70$	1 40m A	1.7		1.7		
		$2.70 \leq V_{CC} \leq 3.60$	I <sub>OH</sub> =-18mA	2.4		2.4		
		$2.70 \leq V_{CC} \leq 3.60$	I <sub>OH</sub> =-24mA	2.2	7	2.2		1

Continued on following page...

### DC Electrical Characteristics (Continued)

		.,	0	T <sub>A</sub> =	25°C	T <sub>A</sub> =-40	) to 85°C	
Symbol	Parameter	V <sub>CC</sub>	Conditions	Min.	Max.	Min.	Max.	Units
		0.90			0.1		0.1	
		$1.10 \leq V_{CC} \leq 1.30$			0.1		0.1	
		$1.40 \le V_{CC} \le 1.60$	1.004		0.2		0.2	
		$1.65 \leq V_{CC} \leq 1.95$	I <sub>OL</sub> =100μA		0.2		0.2	
		$2.30 \leq V_{CC} \leq 2.70$			0.2		0.2	
		$2.70 \leq V_{CC} \leq 3.60$			0.2		0.2	
	LOW Level	$1.10 \leq V_{CC} \leq 1.30$	I <sub>OL</sub> =2mA		0.25 x V <sub>CC</sub>		0.25 x V <sub>CC</sub>	V
V <sub>OL</sub>	Output Voltage	$1.40 \le V_{CC} \le 1.60$	I <sub>OL</sub> =4mA		0.25 x V <sub>CC</sub>		0.25 x V <sub>CC</sub>	V
		$1.65 \le V_{CC} \le 1.95$	I <sub>OL</sub> =6mA		0.3		0.3	
		$2.30 \leq V_{CC} \leq 2.70$	I <sub>OI</sub> =12mA		0.4		0.4	
		$2.70 \leq V_{CC} \leq 3.60$	I <sub>OL</sub> =12IIIA		0.4		0.4	
		$2.30 {\leq V_{CC}} {\leq 2.70}$	I <sub>OL</sub> =18mA		0.6		0.6	
4		$2.70 \leq V_{CC} \leq 3.60$	IOL=TOTIA		0.4		0.4	
		$2.70 \leq V_{CC} \leq 3.60$	I <sub>OL</sub> =24mA		0.55		0.55	
I <sub>IN</sub>	Input Leakage Current	0.90 to 3.60	$0 \leq V_{IN} \leq 3.60$		±0.1		±0.5	μΑ
I <sub>OFF</sub>	Power Off Leakage Current	0	$0 \le (V_{IN}, v_O) \le 3.60$		0.5		0.5	μΑ
la a	Quiescent	0.90 to 3.60	V <sub>IN</sub> =V <sub>CC</sub> , or GND		0.9		0.9	
Icc	Supply Current	0.90 (0 3.60	$V_{CC} \leq V_{IN} \leq 3.6 V$				±0.9	μA

### **AC Electrical Characteristics**

Cumbal	Doromotor	V	Conditions		T <sub>A</sub> =25°	С	T <sub>A</sub> =-40	to 85°C	l lnito	Figure
Symbol	Parameter	V <sub>CC</sub>	Conditions	Min.	Тур.	Max.	Min.	Max.	Units	Figure
		0.90	$C_L=15pF, R_L=1M\Omega$		13					
		$1.10 \le V_{CC} \le 1.30$	C 45°E D 2kO	3.0	6.0	15.8	1.0	18.6	7	
<b>+ +</b>	Propagation	$1.40 \le V_{CC} \le 1.60$	$C_L=15pF, R_L=2k\Omega$	1.0	3.2	8.7	1.0	9.7	ns	Figure 5 Figure 6
t <sub>PHL</sub> , t <sub>PLH</sub>	Delay	$1.65 \leq V_{CC} \leq 1.95$		1.0	2.0	6.0	1.0	6.8		
		$2.30 \leq V_{CC} \leq 2.70$	$C_L$ =30pF, $R_L$ =500 $\Omega$	0.8	1.2	4.1	0.7	4.7		
		$2.70 \leq V_{CC} \leq 3.60$		0.7	1.0	3.3	0.6	4.0		
C <sub>IN</sub>	Input Capacitance	0			2				pF	5
C <sub>PD</sub>	Power Dissipation Capacitance	0.90 to 3.60	V <sub>IN</sub> =0V or V <sub>CC</sub> , f=10MHz		8				pF	3/

### **AC Loadings and Waveforms**

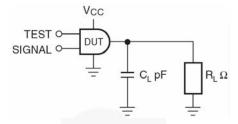
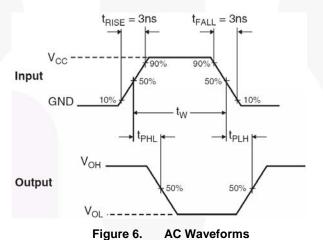


Figure 5. AC Test Circuit



Symbol	V <sub>cc</sub>								
Symbol	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V	1.5V ± 0.1V	1.2V ± 0.1V	0.9V			
$V_{mi}$	1.5V	V <sub>CC</sub> /2							
$V_{mo}$	1.5V	V <sub>CC</sub> /2							

### **Physical Dimensions**

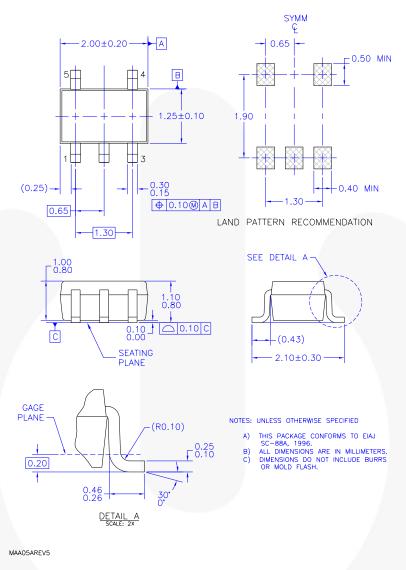


Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

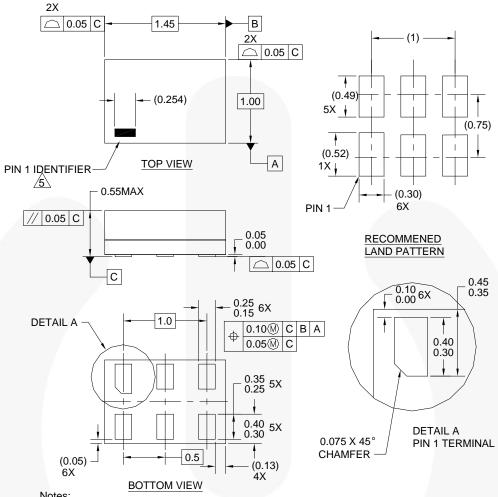
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.

### **Tape and Reel Specification**

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: <a href="http://www.fairchildsemi.com/products/analog/pdf/sc70-5">http://www.fairchildsemi.com/products/analog/pdf/sc70-5</a> tr.pdf.

Package Designator	ackage Designator Tape Section		Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

### **Physical Dimensions**



- Notes:
- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994
- 4. FILENAME AND REVISION: MAC06AREV4
- 5 PIN ONE IDENTIFIER IS 2X LENGTH OF ANY

OTHER LINE IN THE MARK CODE LAYOUT.

Figure 8. 6-Lead, MicroPak™, 1.0mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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### **Tape and Reel Specification**

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: <a href="http://www.fairchildsemi.com/products/logic/pdf/micropak\_tr.pdf">http://www.fairchildsemi.com/products/logic/pdf/micropak\_tr.pdf</a>.

Package Designator Tape Section		<b>Cavity Number</b>	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
L6X	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

#### **Physical Dimensions** 0.89 0.35 ○ 0.05 C 1.00 2X 5X 0.40 PIN 1 0.66 MIN 250uM 1.00 1X 0.45 6X 0.19 ○ 0.05 C TOP VIEW RECOMMENDED LAND PATTERN 2X FOR SPACE CONSTRAINED PCB 0.90 // 0.05 C 0.55MAX С 5X 0.52 SIDE VIEW 0.73 (0.08) 4X -1X 0.57 0.09 0.19 6X DETAIL A 3 - 0.20 6X ALTERNATIVE LAND PATTERN FOR UNIVERSAL APPLICATION (0.05) 6X5X 0.35 0.25 0.60 0.10M C B A 0.35 $\Phi$ 0.40 (0.08).05 C 0.30 4X **BOTTOM VIEW** NOTES: A. COMPLIES TO JEDEC MO-252 STANDARD B. DIMENSIONS ARE IN MILLIMETERS. 0.075X45° C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

Figure 9. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

DETAIL A

PIN 1 LEAD SCALE: 2X

CHAMFER

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D. LANDPATTERN RECOMMENDATION IS BASED ON FSC

E. DRAWING FILENAME AND REVISION: MGF06AREV3

#### **Tape and Reel Specification**

DESIGN.

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/packaging/MicroPAK2\_6L\_tr.pdf.

Package Designator Tape Section		<b>Cavity Number</b>	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
FHX	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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DEUXPEED<sup>6</sup>

Dual Cool™

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FastvCore™

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F-PESTM

FREET

MICROCOUPLER" OptoHiT™ OPTOLOGIC® OPTOPLANAR® PDP SPM™

Power-SPM™

PowerTrench<sup>6</sup> PowerXS\*\* Programmable Active Droop™ OFFT

QSTM Ouiet Series™ RapidConfigure™

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