

June 2001 Revised September 2004

NC7SZ386

TinyLogic® UHS 3-Input Exclusive-OR Gate

General Description

The NC7SZ386 is a single 3-Input Exclusive-OR Gate from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad $V_{\rm CC}$ operating range. The device is specified to operate over the 1.65V to 5.5V $V_{\rm CC}$ range. The inputs and output are high impedance when $V_{\rm CC}$ is 0V. Inputs tolerate voltages up to 7V independent of $V_{\rm CC}$ operating voltage.

Features

- Space saving SC70 6-lead package
- Ultra small MicroPak™ leadless package
- Ultra High Speed; t_{PD} 2.9 ns typ into 50 pF at 5V V_{CC}
- High Output Drive; ± 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

	Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As		
ī	NC7SZ386P6X	MAA06A	386	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel		
1	NC7SZ386L6X	MAC06A	F4	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel		

Logic Symbol



Pin Descriptions

Pin Names	Description
A, B, C	Input
Y	Output

Function Table

 $Y = A \oplus B \oplus C$

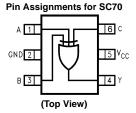
		Output		
-	4	В	С	Υ
L	-	L	L	L
L	-	L	Н	Н
L	-	Н	L	Н
L	_	Н	Н	L
F	1	L	L	Н
F	1	L	Н	L
F	1	Н	L	L
I +	1	н	н	н

H = HIGH Logic Level

L = LOW Logic Level

 $\label{eq:total_cond} \mbox{TinyLogic@ is a registered trademark of Fairchild Semiconductor Corporation.} \\ \mbox{MicroPak}^{\mbox{\tiny TM}} \mbox{ is a trademark of Fairchild Semiconductor Corporation.} \\$

Connection Diagrams

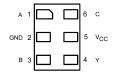


Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code **Note:** Orientation of Top Mark determines Pin One location. Read the Top Product Code Mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Through View)

Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Voltage (V _{IN})	-0.5V to +7.0V
DC Output Voltage (V _{OUT})	-0.5V to +7.0V
DC Input Diode Current (I _{IK})	
$@V_{INI} < -0.5V$	−50 mA

 $@V_{IN} < -0.5V$ -50 mA $@V_{IN} > 6V$ +20 mA

DC Output Diode Current (I_{OK})

Junction Temperature under Bias (T_J)

Junction Lead Temperature (T_L) ;

(Soldering, 10 seconds) 260°C

Power Dissipation (PD) @ +85°C

SC70-5 150 mW

Recommended Operating Conditions (Note 2)

Input Rise and Fall Time $(t_r, \, t_f)$

$$\begin{split} & \text{V}_{\text{CC}} = 1.8\text{V}, \, 2.5\text{V} \pm 0.2\text{V} & \text{0 ns/V to 20 ns/V} \\ & \text{V}_{\text{CC}} = 3.3\text{V} \pm 0.3\text{V} & \text{0 ns/V to 10 ns/V} \\ & \text{V}_{\text{CC}} = 5.0\text{V} \pm 0.5\text{V} & \text{0 ns/V to 5 ns/V} \end{split}$$

Thermal Resistance (θ_{JA})

SC70-5 425°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}		T _A = +25°C	;	T _A = -40°0	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Conditions	
Syllibol	Farameter	(V)	Min	Тур	Max	Min	Max	Units	Condi	tions
V _{IH}	HIGH Level Input Voltage	1.8 ± 0.15	0.75 V _{CC}			0.75 V _{CC}		V		
		2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		l v		
V _{IL}	LOW Level Input Voltage	1.8 ± 0.15			0.25 V _{CC}		0.25 V _{CC}	V		
		2.3 to 5.5			$0.3~\mathrm{V}_{\mathrm{CC}}$		$0.3~V_{\rm CC}$	l *		
V _{OH}	HIGH Level Output Voltage	1.65	1.55	1.65		1.55				
		2.3	2.2	2.3		2.2			$V_{IN} = V_{IH}, V_{II}$	$I_{OH} = -100 \mu A$
		3.0	2.9	3.0		2.9			VIN - VIH, VIL	
		4.5	4.4	4.5		4.4				
		1.65	1.29	1.52		1.29		V		$I_{OH} = -4 \text{ mA}$
		2.3	1.9	2.15		1.9				$I_{OH} = -8 \text{ mA}$
		3.0	2.4	2.80		2.4				$I_{OH} = -16 \text{ mA}$
		3.0	2.3	2.68		2.3				$I_{OH} = -24 \text{ mA}$
		4.5	3.8	4.20		3.8				$I_{OH} = -32 \text{ mA}$
V _{OL}	LOW Level Output Voltage	1.65		0.0	0.1		0.1			
		2.3		0.0	0.1		0.1		$V_{IN} = V_{IH}$ or V_{II}	I 100 !! A
		3.0		0.0	0.1		0.1		VIN - VIH OI VIL	10L = 100 μΑ
		4.5		0.0	0.1		0.1			
		1.65		0.08	0.24		0.24	V		$I_{OL} = 4 \text{ mA}$
		2.3		0.10	0.3		0.3			$I_{OL} = 8 \text{ mA}$
		3.0		0.15	0.4		0.4			$I_{OL} = 16 \text{ mA}$
		3.0		0.22	0.55		0.55			$I_{OL} = 24 \text{ mA}$
		4.5		0.22	0.55		0.55			$I_{OL} = 32 \text{ mA}$
I _{IN}	Input Leakage Current	0 to 5.5			±1		±10	μΑ	$V_{IN} = 5.5V$, GND)
I _{OFF}	Power Off Leakage Current	0.0			1		10	μΑ	V _{IN} or V _{OUT} = 5.5V	
I _{CC}	Quiescent Supply Current	1.65 to 5.5			2.0		20	μΑ	$V_{IN} = 5.5V$, GND)

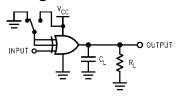
150°C

AC Electrical Characteristics

Symbol	Parameter	V_{CC} $T_A = +25^{\circ}C$			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Figure	
Cymbol		(V)	Min	Тур	Max	Min	Max	Omico		Number
t _{PLH} ,	Propagation Delay	1.8 ± 0.15	2.0	14.0	22.5	2.0	23.0			
t_{PHL}		2.5 ± 0.2	0.8	8.0	12.5	0.8	13.0	ns	$C_{L} = 15 \text{ pF},$	Figures
		3.3 ± 0.3	0.5	6.0	9.2	0.5	9.5	113	$R_L = 1 M\Omega$	1, 3
		5.0 ± 0.5	0.5	4.3	5.7	0.5	6.1			
t _{PLH} ,	Propagation Delay	3.3 ± 0.3	1.5	6.1	9.5	1.5	9.8	ns	$C_L = 50 \text{ pF},$	Figures
t_{PHL}		5.0 ± 0.5	0.8	4.8	6.5	1.0	6.9	113	$R_L = 500\Omega$	
C _{IN}	Input Capacitance	0		4				pF		
C _{PD}	Power Dissipation Capacitance	3.3		25				pF	(Note 3)	Figure 2
		5.0		31				ы	(Note 3)	i iguie z

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{\parallel N}) + (I_{CC}static)$.

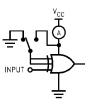
AC Loading and Waveforms



 $\mathbf{C}_{\mathbf{L}}$ includes load and stray capacitance

Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; $t_r = t_f = 1.8 \text{ ns};$

PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

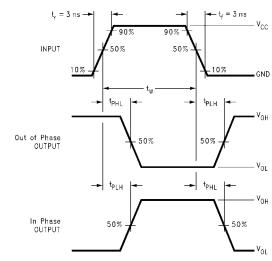


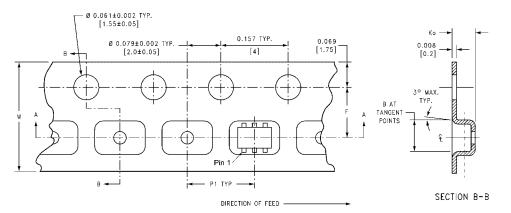
FIGURE 3. AC Waveforms

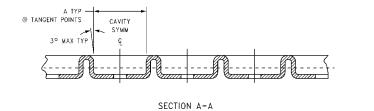
Tape and Reel Specification

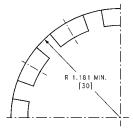
TAPE FORMAT for SC70

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Package	Tape	Number	Cavity	Cover Tape						
Designator	Section	Cavities	Status	Status						
	Leader (Start End)	125 (typ)	Empty	Sealed						
P6X	Carrier	3000	Filled	Sealed						
	Trailer (Hub End)	75 (typ)	Empty	Sealed						

TAPE DIMENSIONS inches (millimeters)



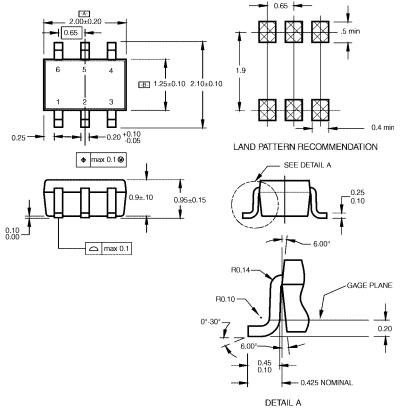




BEND RADIUS NOT TO SCALE

Package	Tape Size	DIM A	DIM B	DIM F	DIM K _o	DIM P1	DIM W
SC70-6	8 mm	0.093	0.096	0.138 ± 0.004	0.053 ± 0.004	0.157	0.315 ± 0.004
3070-0		(2.35)	(2.45)	(3.5 ± 0.10)	(1.35 ± 0.10)	(4)	(8 ± 0.1)

Tape and Reel Specification (Continued) TAPE FORMAT for MicroPak Package Tape Number Cavity Cover Tape Designator Section Cavities Status Status Leader (Start End) 125 (typ) Empty Sealed L6X Carrier 5000 Filled Sealed Trailer (Hub End) 75 (typ) **Empty** Sealed 2.00-1.75±0.10 В 8.00 ^{+0.30} -0.10 3.50±0.05 1.15±0.05 **-** → В◄ -ø 0.50 ±0.05 SECTION B-B DIRECTION OF FEED SCALE:10X 0.254±0.020 Г 0.70±0.05 SECTION A-A SCALE:10X **REEL DIMENSIONS** inches (millimeters) TAPE SLOT DETAIL X DETAIL X SCALE: 3X W1 W2 W3 Tape В С D Ν Α Size W1 + 0.078/-0.039 0.331 + 0.059/-0.000 0.567 7.0 0.059 0.512 0.795 2.165 8 mm (177.8)(1.50)(13.00)(20.20)(55.00)(8.40 + 1.50 / -0.00)(W1 + 2.00/-1.00)(14.40)



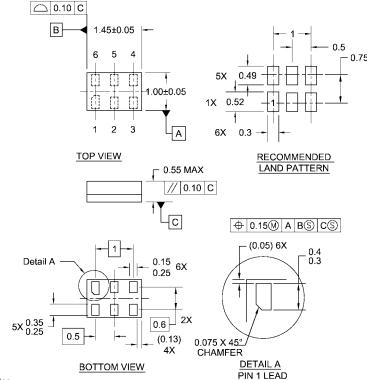
NOTES:

- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

6-Lead SC70, EIAJ SC88, 1.25mm Wide Package Number MAA06A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

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