Advance Information Full Featured Voltage Mode PWM Controller

The NCP1560 PWM controller contains all of the features and flexibility needed to implement voltage-mode control for modern high performance power converters. This device cost effectively reduces system part count with the inclusion of a high-voltage start-up regulator that operates over a wide input range of 33 V to 150 V. The NCP1560 provides two control outputs, OUT1 which controls the main PWM switch and OUT2 with adjustable over-lap delay, which can control a synchronous rectifier. Other distinctive features include: two mode over-current protection, line under/over voltage lockout, fast line feed-forward, soft-start and a maximum duty cycle clamp.

Features

- Internal High Voltage Start-up Regulator
- Dual Control Outputs with Adjustable Over-Lap Delay
- Single Resistor Oscillator Frequency Setting
- Fast Line Feed–Forward
- Line Under/Over Voltage Lockout
- Dual Mode Over-Current Protection
- Programmable Maximum Duty Cycle Control
- Maximum Duty Cycle Proportional to Line Voltage
- Programmable Soft-Start
- Precision Reference

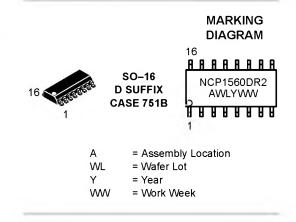
Typical Applications

- Telecommunication Power Converters
- Industrial Power Converters
- High Voltage Power Modules
- +42 V Automotive Systems
- Control Driven Synchronous Rectifier Power Converters



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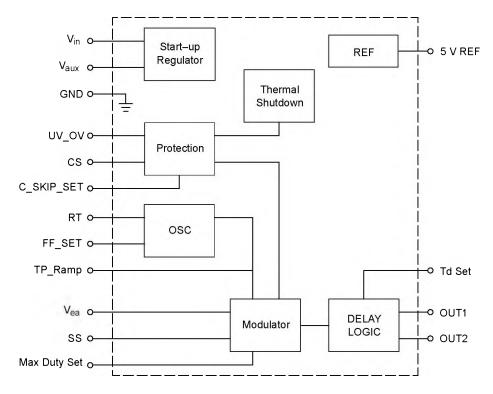


ORDERING INFORMATION

| Device | Package | Shipping |
|------------|---------|-----------------|
| NCP1560DR2 | SO–16 | 2500 Units/Reel |

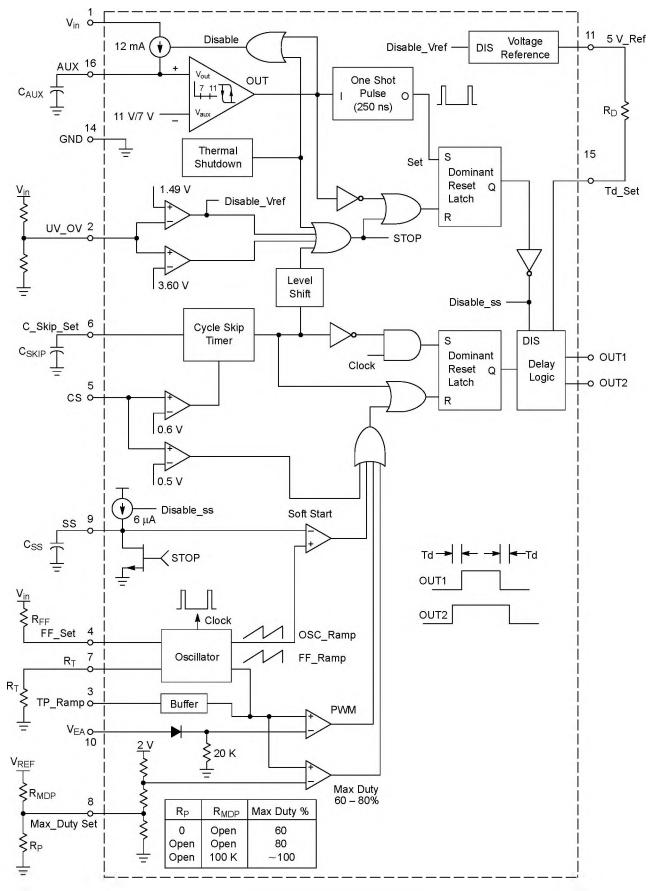
This document contains information on a new product. Specifications and information herein are subject to change without notice.

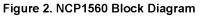
NCP1560





NCP1560





PIN DESCRIPTION

| Pin Name | | Description | Application Information | | | |
|----------|--------------|---|---|--|--|--|
| 1 | Vin | Source Input Voltage | Input range: 33 V to 150 V. | | | |
| 2 | UV_OV | Input Undervoltage and Overvoltage shutdown. | An external divider from the power converter source input must be scaled >1.49 volts and < 3.60 volts over the operational range. | | | |
| 3 | TP_Ramp | Test point provided for the Feed Forward Ramp signal. | Internally this signal is compared to Vea. | | | |
| 4 | FF_SET | An external resistor between Vin and this pin adjusts the amplitude of the FF_Ramp in proportion to Vin and R. | By varying the PWM ramp amplitude in proportion to the line voltage changes in loop bandwidth resulting from line voltage changes are eliminated. | | | |
| 5 | CS | Current Sense input | If CS exceeds 0.5 volt the outputs will go into a Cycle by Cycle current limit. If CS exceeds 0.6 volts the outputs will be disabled for a period determined by the Current Sense Fault Timer. A softstart will follow at the conclusion of the fault timer. | | | |
| 6 | C_SKIP_SET | An external capacitor sets the shutdown period after 0.6 V CS event. | An external capacitor sets the shutdown period. Range: 68 pF = 12 μs, 6800 pF = 1.2 ms | | | |
| 7 | RT | A single external resistor between this pin and GND sets the fixed oscillator frequency. | Resistance Range 68 K = 500 KHz 390 K = 100 KHz | | | |
| 8 | MAX_DUTY_SET | An external resistor between this pin and GND sets the maximum allowable Duty cycle. | Resistance Range 0 Ohms = 60% Open = 80% given the FF_Ramp of 2.0 V peak (low line). | | | |
| 9 | SS | Softstart control | An external capacitor and the internal 6.0 μ A current source, set the softstart ramp. The capacitor voltage sets a maximum duty cycle clamp from 0 to 2.0 volts (0 to 100% Duty). | | | |
| 10 | Vea | Input from an external error amplifier. | There is no error amplifier included within this controller. The error amplifier is typically secondary side referenced while the controller is primary side referenced. | | | |
| 11 | 5.0 V_REF | Precision 5.0 volt reference output. | Maximum output current: 10 mA. | | | |
| 12 | Td_Set | An external resistor between Vref and this pin sets the leading edge and trailing edge time delay between OUT1 and OUT2. | Time delay (Td) Rd open = 250 nS (Max Delay) Rd (60 K) = 25 nS (Min Delay) | | | |
| 13 | OUT2 | Output of the PWM controller with leading edge and a trailing edge time delay of (Td). | OUT2 can be used to drive a synchronous rectifier. | | | |
| 14 | GND | Return | | | | |
| 15 | OUT1 | Output of the PWM controller. | OUT1 main PWM output. | | | |
| 16 | AUX | Auxiliary bias power. Upon turn–on an internal current source supplies bias power. An external slave winding then continues supplying bias power. | An internal current source supplies 12 mA until Vaux reaches 11 volts. An external capacitor is required to holdup Vaux above 7.0 volts while the converter starts. Typically an external slave winding then provides power to the control circuits. | | | |

MAXIMUM RATINGS (Notes 1 & 2)

| Rating | Symbol | Value | Unit |
|--|------------------|-------------|------|
| Vin to GND | V _{in} | 150 | V |
| Vaux to GND | V _{aux} | 16 | V |
| All Other Inputs to GND | - | - | V |
| 5.0 V Reference Output Current | I _{REF} | 10 | mA |
| OUT1, OUT2 Output Current | IOUT1, IOUT2 | 20 | mA |
| Operating Junction Temperature | TJ | -40 to +140 | °C |
| Storage Temperature Range | T _{stg} | –55 to +150 | °C |
| Power Dissipation at $T_A = 25^{\circ}C$ | PD | 0.88 | W |
| Thermal Resistance, Junction to Case | $R_{	heta JA}$ | 130 | °C/W |

 Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
This device series contains ESD protection and exceeds the following tests:

 This device series contains ESD protection and exceeds the following test Human Body Model 2000 V per MIL–STD–883, Method 3015. Machine Model Method 200 V.

ELECTRICAL CHARACTERISTICS ($T_A = T_{low}$ to T_{high} , $V_{in} = 48$ V, $V_{aux} = 12$ V, $R_T = 100$ K, $C_{ft} = 6800$ pF, $R_d = 60$ K, $R_{FF} = 464$ K)

| Characteristic | Symbol | Conditions | Min | Тур | Max | Unit |
|--|------------------|--|------|------|------|------|
| Reference | • | | | | | |
| REF Output Voltage | V _{REF} | I _{ref} = 0 mA | 4.9 | 5.0 | 5.1 | V |
| REF Voltage Regulation | | I _{ref} = 0 to 10 mA | - | 50 | - | mV |
| Vaux Supply | • | • | - | | | |
| Vaux Current Source | | Vaux < 11 V* | 11 | 12 | - | mA |
| Vaux Current Source Disable | | | - | 11 | - | V |
| Vaux Undervoltage Lockout Voltage | | | - | 7.0 | - | V |
| Startup Regulator Leakage | | T _A = 25°C, V _{in} = 150 V | - | - | 50 | μΑ |
| Supply Current (laux) | | Vea = 0 V | - | - | 5.0 | mA |
| Shutdown Current (laux) | | Vuv/ov = 0 V | - | _ | 2.5 | mA |
| Input UV/OV Shutdown | | • | | | • | |
| Undervoltage Shutdown (increasing) | | | 1.43 | 1.49 | 1.55 | V |
| Undervoltage Shutdown Hysteresis | | | - | 0.16 | - | V |
| Overvoltage Shutdown (increasing) | | | 3.46 | 3.60 | 3.74 | V |
| Overvoltage Shutdown Hysteresis | | | - | 0.16 | - | V |
| Current Limit | | • | | | | |
| ILIM Delay to Output (T _A = 25°C) | | | - | - | 150 | nS |
| Cycle-by-Cycle Threshold Voltage | | | 0.47 | 0.5 | 0.53 | V |
| Cycle Skip Threshold Voltage | | | 0.57 | 0.6 | 0.63 | V |
| Cycle Skip Program | • | | | • | • | • |
| Time Delay | | | _ | 1.2 | - | mS |

*Non-continuous rating. Vaux current source will supply 12 mA over the input voltage range of 33 V to 150 V. However package thermal restrictions apply.

NCP1560

ELECTRICAL CHARACTERISTICS (continued) ($T_A = T_{low}$ to T_{high} , $V_{in} = 48$ V, $V_{aux} = 12$ V, $R_T = 100$ K, $C_{ft} = 6800$ pF, $R_d = 60$ K, $R_{FF} = 464$ K)

| Characteristic | Symbol | Conditions | Min | Тур | Max | Unit |
|---|---------|-------------------------------------|-----|------|-----|------|
| Softstart | | • | | | | |
| Charge Current | | | 5.0 | 6.0 | 7.0 | μΑ |
| Discharge Current | | | - | 10 | - | mA |
| Oscillator | | • | - | - | | |
| Frequency | | | 285 | 300 | 315 | KHz |
| PWM Comparator | | · | | | | |
| Input Bias Current | | | - | 1.0 | - | nA |
| Delay to Output (T _A = 25°C) | | | - | - | 200 | nS |
| Feedforward | | | | | | |
| FF Ramp Amplitude | | | - | 2.7 | - | V |
| Max Duty Program | | • | | | | |
| Max Duty 60% | | Rp = 0 Ohms, V _{in} = 36 V | 57 | 60 | 63 | % |
| Max Duty 80% | | Rp = open, V _{in} = 36 V | 76 | 80 | 84 | % |
| Output Section | | | | | | |
| Output High Saturation | | I _{out} = 10 mA | - | 11.4 | - | V |
| Output Low Saturation | | I _{out} = –10 mA | - | 0.25 | - | V |
| Rise Time | | C _L = 100 pF | - | 20 | - | nS |
| Fall Time | | C _L = 100 pF | - | 12 | - | nS |
| Time Delay Set | | - | | | | |
| Time Delay Max | Td(max) | Rd = open, T _A = 25°C | 225 | 250 | 275 | nS |
| Time Delay Min | Td(min) | Rd = 60 K, T _A = 25°C | 20 | 25 | 30 | nS |
| Thermal Shutdown | | | | | | |
| Thermal Shutdown Temperature | Tsd | | - | 150 | - | °C |

DETAILED OPERATING DESCRIPTION

The NCP1560 PWM controller contains all of the features and flexibility needed for implementation of voltage-mode control for modern high performance power converters. This device cost effectively reduces system part count with the inclusion of a high-voltage start-up regulator. The NCP1560 provides two control outputs, OUT1 which controls the main PWM switch and OUT2 with adjustable over-lap delay, which can control a synchronous rectifier switch. Other distinctive features include: two mode over-current protection, line under/over voltage lockout, fast line feed-forward, soft-start and a maximum duty cycle clamp. The Functional Block Diagram is shown in Figure 1.

The NCP1560 is designed for Voltage–Mode Control converters. The features included in the NCP1560 enable all of the advantages of Current–Mode Control, fast line feed–forward, and cycle by cycle current limit. It eliminates the disadvantages of low power jitter, slope compensation and noise susceptibility. Finally the dual outputs of the NCP1560 allow for optimum control of a synchronous rectifier switch.

High Voltage Start-up Regulator

The NCP1560 contains an internal high voltage current source. This current source is set to 12 mA. When the line voltage is in range, the current source is enabled and sources current into an external capacitor connected to the Vaux pin. When the voltage on the Vaux pin reaches 11 V the controller outputs are enabled and the internal current source is disabled. The Vaux voltage will then transition to the converter self bias voltage. The start-up regulator will remain off until the Vaux voltage falls below 7.0 V. At that time the outputs will be disabled until the Vaux pin again reaches 11 V. The external Vaux capacitor must be sized such that the self-bias will maintain a Vaux voltage greater than 7.0 V during initial start-up. During a fault mode when the converter self bias is inactive, external current draw on the Vaux line should be limited as to not exceed the maximum power dissipation of the controller.

Input Under/Over Voltage Shutdown

The NCP1560 contains a line under/over voltage shut down circuit. An external voltage divider sets the operational range of the converter. The divider must be set for a voltage at the under/over voltage pin to be greater than 1.49 V and less than 3.60 V. If the Under voltage threshold is not met, all functions of the controller are disabled except the bias (Vaux) regulator and the controller will be in a low power state, < 500 μ A. If the Over voltage threshold is exceeded, OUT1 and OUT2 will be disabled and the softstart capacitor will be discharged.

The under/over voltage pin can also be used to implement a remote enable/disable function. By shorting the over/under pin to ground, the converter can be disabled. The internal bias regulator will continue to operate varying between 7.0 and 11 volts. All other functions will be disabled.

Reference

The NCP1560 provides a precision reference output of 5 volts. This output should be locally bypassed with a 0.1 μ F ceramic capacitor. The maximum current available from this output is 10 mA.

Current Limit

The NCP1560 contains two levels of over current protection. If the voltage on the CS pin exceeds 0.5 volt the present cycle is terminated and the outputs are disabled. If the voltage on the CS pin exceeds 0.6 volts, the controller will disable the outputs, enable the Cycle Skip Timer and discharge the softstart capacitor. The outputs will remain disabled until the Cycle Skip Timer completes, then a softstart will commence. The duration of the Current Sense Fault Timer is set by an external capacitor. The range of capacitor (time set) is 68 pF (12 μ s) to 6800 pF (1.2 mS). A complete softstart will commence after the current sense fault timer completes.

Oscillator and Ramp Feed–Forward

The NCP1560 oscillator is set by a single external resistor connected between the RT pin and return. Internally there are two ramp voltages generated by the oscillator. The OSC_Ramp is a fixed amplitude ramp of 0 to 1.5 volts. This ramp is used for the softstart comparator and as a basis for the Feed Forward ramp (FF_Ramp). The amplitude of the FF ramp varies in proportion to the voltage on the FF_SET pin. The FF_Ramp is used for the PWM comparator and the Max Duty Cycle comparator. The amplitude of the FF_Ramp is normally set to vary from 1.5 to 3.0 volts for a corresponding 2:1 change in line voltage. An external resistor between the FF_SET pin and the line sets the proportion to which the ramp amplitude changes with line voltage.

Maximum Duty Cycle

A dedicated internal comparator limits the maximum output duty cycle. The Feedforward ramp is compared to a fixed voltage configured by the Max Duty Cycle pin. Since the amplitude of the Feedforward ramp increases with increasing line voltage the maximum duty cycle will then decrease with increasing line voltage, which is a desirable feature. If the Max Duty Cycle pin is left open the voltage present at the Max Duty Cycle comparator will be 1.6 volts. which will correspond to a maximum duty cycle of 80% when the FF Ramp amplitude is at 2.0 volts. If the Max Duty Cycle pin is shorted to return the voltage present at the Max Duty Cycle comparator will be 1.2 volts, which will correspond to a maximum duty cycle of 60% when the FF Ramp amplitude is 2.0 volts. If the Max Duty Cycle pin is connected to Vref, the maximum duty cycle feature will be disabled and the maximum duty cycle will approach 100%. If the FF Ramp amplitude increases to 4.0 volts as a result of the line increasing the maximum duty cycle will then decrease to 40% or 30%, respectively, depending upon the Maximum Duty Set pin configuration.

PWM Comparator

The PWM comparator compares the Feedforward ramp to the voltage presented at the Vea pin. There is a 0.65 V (diode) offset between the Vea pin and the PWM comparator. The output of an external error amplifier generally drives the Vea pin. The comparator polarity is such that 0.65 volts or less on the Vea pin will cause a Zero duty cycle.

Softstart

The softstart feature allows the converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. Upon power on, a 6.0 μ A current is sourced out of the softstart pin into an external capacitor. The capacitor voltage will begin to ramp up. The voltage on the softstart pin is compared to a 2.0 V Oscillator Ramp signal and will act to reduce the maximum duty cycle until the capacitor voltage or current cycle skip, the softstart pin will discharge the external capacitor and disable the output drivers. When the fault condition is no longer present a softstart will be exercised again.

OUT1, OUT2 and Time Delay

The NCP1560 provides two in-phase outputs, OUT1 and OUT2. However, OUT2 always precedes OUT1 at any low to high transition and OUT1 always precedes OUT2 at any high to low transition. The leading and trailing time delays are equal and set by the Time Delay pin. An open circuit on the Time Delay pin will cause the maximum delay of 500 nS. A 60 K resistor between the Time Delay pin and 5.0 V_REF will cause the minimum delay of 50 nS. Generally, OUT1 controls the main switching element. OUT2 once inverted can drive the free-wheeling synchronous rectifier switching element.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 150 degrees Celsius, the controller is forced into a low power reset state, disabling the output drivers and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.