

NDS351AN

N-Channel, Logic Level, PowerTrench^o MOSFET

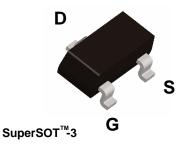
General Description

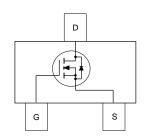
These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.4 A, 30 V. $R_{DS(ON)} = 160 \text{ m}\Omega$ @ $V_{GS} = 10 \text{ V}$ $R_{DS(ON)} = 250 \text{ m}\Omega$ @ $V_{GS} = 4.5 \text{ V}$
- · Ultra-Low gate charge
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT[™]-3 design for superior thermal and electrical capabilities
- High performance trench technology for extremely low R_{DS(ON)}





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		30	V
V _{GSS}	Gate-Source Voltage		± 20	V
I _D	Drain Current - Continuous	(Note 1a)	1.4	А
	- Pulsed		10	
P _D	Power Dissipation for Single Operation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
351A	NDS351AN	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics				•	l
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = 250 \mu\text{A}$	30			V
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A,Referenced to 25°C		26		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, \qquad V_{GS} = 0 \text{ V}$			1	μА
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10	μА
I _{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			±100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	0.8	2.1	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$, Referenced to $25^{\circ}C$		-4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$\begin{aligned} &V_{GS} = 10 \text{ V}, &I_{D} = 1.4 \text{ A} \\ &V_{GS} = 4.5 \text{ V}, &I_{D} = 1.2 \text{ A} \\ &V_{GS} = 10 \text{ V}, I_{D} = 1.4 \text{ A}, T_{J} = 125 ^{\circ}\text{C} \end{aligned}$		92 120 114	160 250 214	mΩ
I _{D(on)}	On-State Drain Current	$V_{GS} = 4.5V$, $V_{DS} = 5 V$	3.5			Α
G FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 1.4 \text{ A}$		4		S
Dynamic	Characteristics			•		•
C _{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		145		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		35		pF
C _{rss}	Reverse Transfer Capacitance	7		15		pF
R _G	Gate Resistance	$V_{GS} = 15 \text{ mV}, f = 1.0 \text{ MHz}$		1.6		Ω
Switchin	ng Characteristics (Note 2)	•				
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, \qquad I_{D} = 1 \text{ A},$		3	6	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		8	16	ns
t _{d(off)}	Turn-Off Delay Time			16	29	ns
t _f	Turn-Off Fall Time			2	4	ns
Qg	Total Gate Charge	$V_{DS} = 15 \text{ V}, \qquad I_{D} = 1.4 \text{ A},$		1.3	1.8	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = 4.5 \text{ V}$		0.5		nC
Q_{gd}	Gate-Drain Charge			0.5		nC
Drain-Se	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source	Diode Forward Current			0.42	Α
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 0.42 \text{ A} \text{(Note 2)}$		0.8	1.2	V
t _{rr}	Diode Reverse Recovery Time	$I_F = 1.4 \text{ A}, \qquad d_{iF}/d_t = 100 \text{ A/}\mu\text{s}$		11		nS
Q _{rr}	Diode Reverse Recovery Charge			4		nC

Notes:

 R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.



b) 270°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%

Typical Characteristics

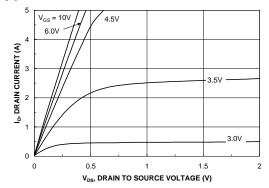


Figure 1. On-Region Characteristics.

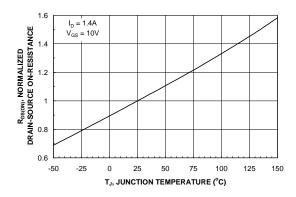


Figure 3. On-Resistance Variation with Temperature.

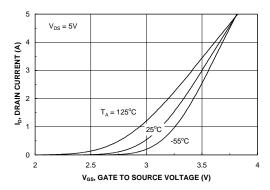


Figure 5. Transfer Characteristics.

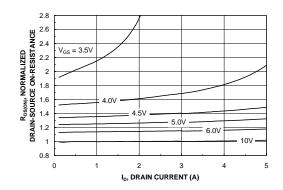


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

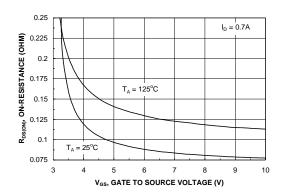


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

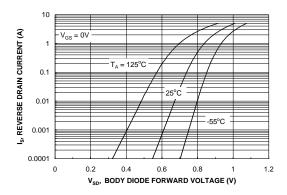
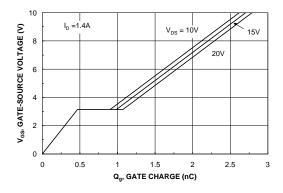


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



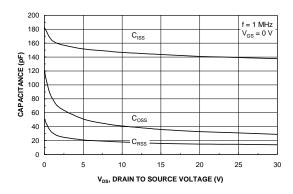


Figure 7. Gate Charge Characteristics.

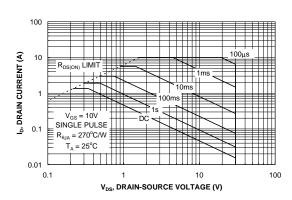


Figure 8. Capacitance Characteristics.

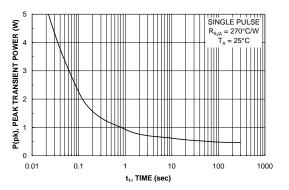


Figure 9. Maximum Safe Operating Area.



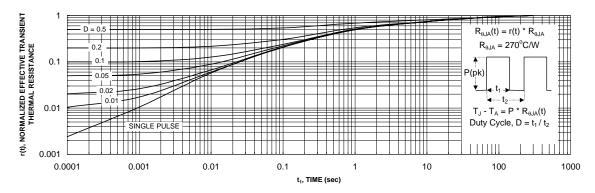


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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