

ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has 8 open collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin molded or cerdip package.

The NE591 has 8 open emitter Darlington outputs which source current to an external load from a common collector line, V_S . This V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18-pin molded or cerdip package.

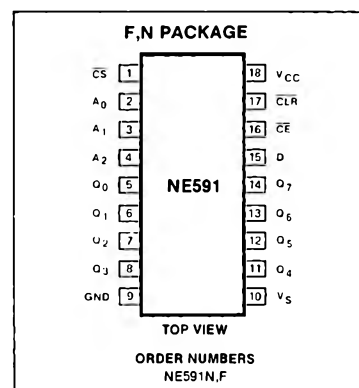
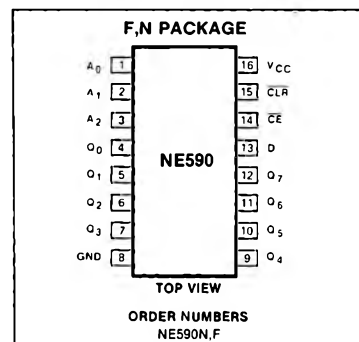
FEATURES

- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- NE590 will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- NE590 is pin compatible with 54/74LS259

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

PIN CONFIGURATION



PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0 - A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0 - Q_7	The 8 device outputs. The NE590 has open collector Darlington outputs. The NE591 has open emitter follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	16	$\overline{CE}$	Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output. The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
—	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
—	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

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TRUTH TABLE (NE590)

INPUTS							OUTPUTS								MODE		
CL _R	CE	D	A ₀	A ₁	A ₂		Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇			
L	H	X	X	X	X		H	H	H	H	H	H	H	H	Clear		
L	L	L	L	L	L		H	H	H	H	H	H	H	H	Demultiplex		
L	L	H	L	L	L		L	H	H	H	H	H	H	H			
L	L	L	H	L	L		H	H	H	H	H	H	H	H			
L	L	H	H	L	L		H	L	H	H	H	H	H	H			
L	L	L	H	H	H		H	H	H	H	H	H	H	H			
L	L	H	H	H	H		H	H	H	H	H	H	H	L			
H	H	X	X	X	X		Q _{N-1} →								Memory		
H	L	L	L	L	L		H	Q _{N-1} →								Addressable Latch	
H	L	H	L	L	L		L	Q _{N-1} →									
H	L	L	H	L	L		Q _{N-1}	H	Q _{N-1} →								
H	L	L	H	L	L		Q _{N-1}	L	Q _{N-1} →								
H	L	L	H	H	H		Q _{N-1}	→ H									
H	L	H	H	H	H		Q _{N-1}	→ L									

X = Don't care condition

Q_{N-1} = Previous output state

L = Low voltage level/"ON" output state

H = High voltage level/"OFF" output state

(NE591)

INPUTS							OUTPUTS								MODE
CLR	CE	CS	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q _{N-1} →								Memory
H	H	L	X	X	X	X	Q _{N-1} →								
H	L	H	X	X	X	X	Q _{N-1} →								
H	L	L	L	L	L	L	L Q _{N-1} →								Addressable Latch
H	L	L	L	L	L	L	H Q _{N-1} →								
H	L	L	L	H	L	L	Q _{N-1} L Q _{N-1} →								
H	L	L	H	H	L	L	Q _{N-1} H Q _{N-1} →								
H	L	L	L	H	H	H	Q _{N-1} → L								
H	L	L	H	H	H	H	Q _{N-1} → H								

X = Don't care

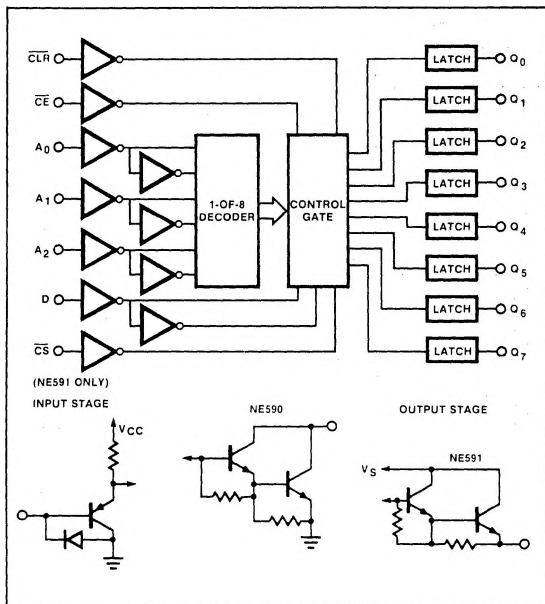
Q_{N-1} = Previous output state

L = Low voltage level/"OFF" output state

H = High voltage level/"ON" output state

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ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
V_{CC} Supply voltage	-0.5 to +7	V
V_{IN} Input voltage	-0.5 to +15	V
V_{OUT} Output voltage	V	
NE590	0 to +7	
NE591	0 to V_{CC}	
V_S Source bus voltage	V	
NE591 only	-0.5 to +7	
$V_S - V_{CC}$ Source/supply differential voltage	V	
NE591 only	-5 to +2	
I_{OUT} Output current	mA	
Each output	300	
All outputs	1000	
P_D Power dissipation ¹	1	W
Temperature range	$^\circ\text{C}$	
T_A Ambient	0 to +70	
T_J Junction	165	
T_{STG} Storage	-65 to +150	
T_{solder} Lead soldering temperature (10sec max)	300	$^\circ\text{C}$

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 4.75$ to 5.25V , $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ unless otherwise specified.^{2,3}

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IH} Input voltage High		2.0			V
V_{IL} Input voltage Low				0.8	V
V_{OL} Output voltage Low (NE590 only)	$I_{OL} = 250\text{mA}$, $T_A = 25^\circ\text{C}$		1.0	1.3	V
V_{OH} Output voltage High (NE591 only)	Over temperature $I_{OH} = -250\text{mA}$, $V_{CC} = V_S = 5\text{V}$	2.9		1.5	V
I_{IH} Input current High	$V_{in} = V_{CC}$		0.1	10	μA
I_{IL} Input current Low	$V_{in} = 0\text{V}$		-25	-60	μA
I_{CE} CE input			-15	-50	μA
I_{OH} Leakage current	$V_{OUT} = 5.25\text{V}$		10	250	μA
I_{CCL} Supply current ⁴ All outputs low	$V_S = V_{CC} = 5\text{V}$				mA
NE590			33	50	
NE591			15	50	
I_{CCH} Supply current ⁴ All outputs high					
NE590			15	50	
NE591			30	50	

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature:

NE590N at 9.3 mW/ $^\circ\text{C}$ above 85°C

NE590F at 7.5 mW/ $^\circ\text{C}$ above 65°C

NE591N at 11.5 mW/ $^\circ\text{C}$ above 100°C

NE591F at 10.7 mW/ $^\circ\text{C}$ above 72°C

2. All typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.

3. For the NE591, $V_S = V_{CC}$ in all tests.

4. Supply current for the NE591 is measured with no output load.

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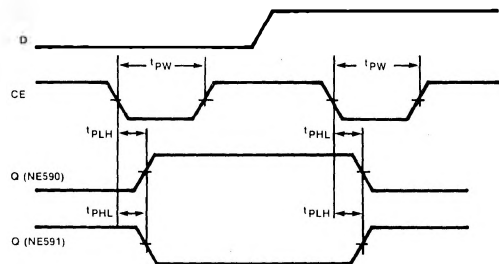
SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER	TO	FROM	NE590			NE591			UNIT
			Min	Typ	Max	Min	Typ	Max	
Propagation delay time t_{PLH} Low to high ⁵ t_{PHL} High to low ⁵	Output	$\overline{CE}$		65 115	150 230		50 70	80 120	ns
t_{PLH} Low to high ⁶ t_{PHL} High to low ⁶	Output	Data		65 120	130 240		45 65	70 100	
t_{PLH} Low to high ⁷ t_{PHL} High to low ⁷	Output	Address		100 130	200 260		45 75	80 140	
t_{PLH} Low to high ⁸ t_{PHL} High to low ⁸	Output	$\overline{CLR}$		65	130		45	140	
t_{PLH} Low to high ⁵ t_{PHL} High to low ⁵	Output	$\overline{CS}$					40 70	80 120	
SWITCHING SET-UP REQUIREMENTS									
$t_{s(H)}^9$ $t_{s(L)}^9$	Chip enable	High data Low data	210 210	60 105		50 80	15 60		ns ns
$t_{s(A)}^{10}$	Chip enable	Address	+ 20	- 5		+ 20	- 20		ns
$t_{h(H)}^9$ $t_{h(L)}^9$	Chip enable	High data Low data	- 20 - 20	60 60		0 + 10	- 60 - 15		ns ns
$t_{s(CS)}^9$	Chip enable	Low chip select				80	50		ns
$t_{pw(E)}$ Chip enable pulse width ⁵			300	140		100	50		ns

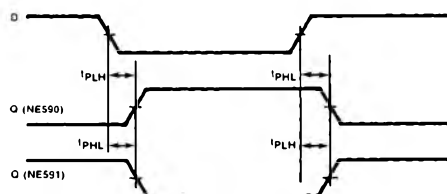
NOTES

- 5 See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
6 See Turn-On and Turn-Off Delays, Data to Output timing diagram.
7 See Turn-On and Turn-Off Delays, Address to Output timing diagram.
8 See Turn-Off Delay, Clear to Output timing diagram.
9 See Setup and Hold Time, Data to Enable timing diagram.
10 See Setup Time, Address to Enable timing diagram.

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH

Other Inputs: $\overline{CLR}$ H, A Stable, $\overline{CS}$ L

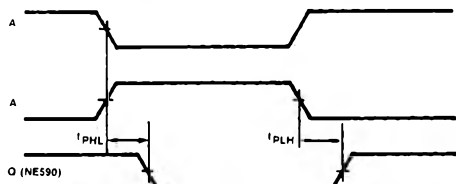
TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT

Other Inputs: $\overline{CE}$ $\overline{CS}$ L, $\overline{CLR}$ H, A = Stable

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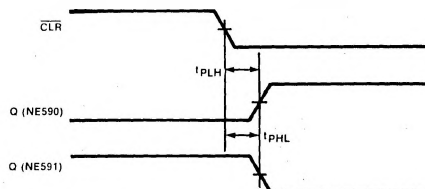
NE590/NE591

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



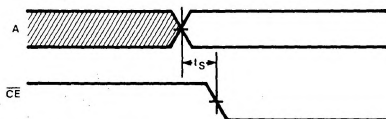
Other Inputs: $\overline{CE} = L$, $\overline{CLR} = L$, $D = H$

TURN-OFF DELAY, CLEAR TO OUTPUT



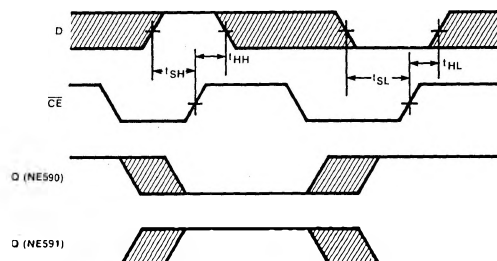
Other Inputs: $\overline{CE} = H$, $\overline{CS} = H$

SETUP TIME, ADDRESS TO ENABLE



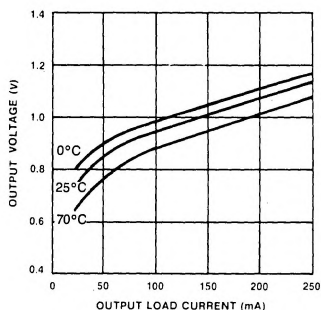
Other Inputs: $\overline{CLR} = H$, $\overline{CS} = L$

SETUP AND HOLD TIME, DATA TO ENABLE

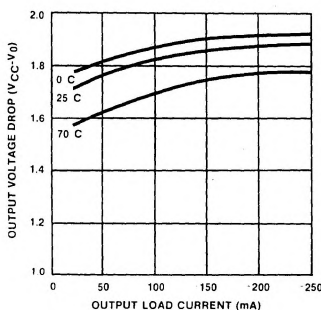


Other Inputs: $\overline{CLR} = H$, $A = \text{Stable}$, $\overline{CS} = L$

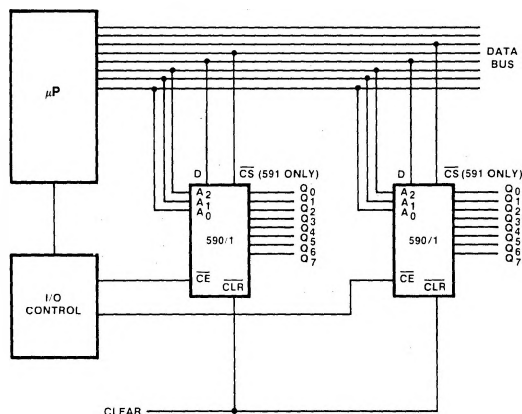
OUTPUT VOLTAGE VS LOAD CURRENT (NE590)



OUTPUT VOLTAGE DROP VS LOAD CURRENT (NE591)



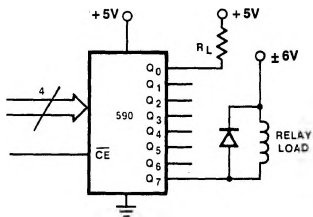
INTERFACING THE 590/591 WITH A MICROPROCESSOR SYSTEM



A0, A1, A2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

TYPICAL APPLICATIONS (Cont'd)

NE590 DRIVING SIMPLE LOADS



NE590 OPERATING IN DEMULTIPLEX MODE

