

NFVA35065L32

ASPM 27 Series

3-Phase 650 V, 50 A Automotive Smart Power Module

Description

NFVA35065L32 is an advanced Automotive SPM[®] module providing a fully-featured, high-performance inverter output stage for hybrid and electric vehicles. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring of drive IC, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

- Automotive SPM in 27 pin DIP package
- Automotive qualified grade (AEC-Q100, 101 & LV 324)
- 650 V/50 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protections
- 175°C guaranteed Short-Circuit Rated FS Trench IGBTs with stable EMI performance
- Outstanding Thermal Resistance using AIN DBC Substrate
- Separated Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply
- LVIC Temperature-Sensing Built-In for Temperature Monitoring
- Isolation Rating: 2500 V_{rms}/1 min.
- Pb-Free and RoHS compliant

Applications

- Automotive high voltage auxiliary motors
 - ◆ Climate e-Compressors
 - ◆ Oil/Water Pumps
 - ◆ Super/Turbo Chargers
 - ◆ Variety Fans

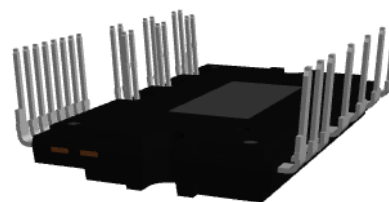
Related Resources

- [AN-9088](#) – Motion SPM 3 V6 Series Users Guide
- [AN-9086](#) – SPM 3 Package Motion Guide



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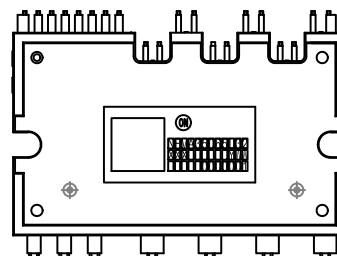
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3D Package Drawing
(Click to Activate 3D Content)

ASPM27-CCA
CASE MODFJ

MARKING DIAGRAM



ON	= ON Semiconductor Logo
NFVA35065L32	= Specific Device Code
XXX	= Lot Number
Y	= Year
WW	= Work Week
0000001	= Serial Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

General Description

Integrated Power Functions

- 650 V–50 A IGBT inverter for three–phase DC/AC power conversion (Refer to Figure 2)

Integrated Drive, Protection and System Control Functions

- For inverter high–side IGBTs: gate drive circuit, high–voltage isolated high–speed level shifting control circuit Under–Voltage Lock–Out Protection (UVLO)
- For inverter high–side IGBTs: gate drive circuit, Short–Circuit Protection (SCP) control supply circuit Under–Voltage Lock–Out Protection (UVLO)
- Fault signaling: corresponding to UVLO (low–side supply) and SC faults
- Input interface: active–HIGH interface, works with 3.3/5 V logic, Schmitt–trigger input

PIN CONFIGURATION

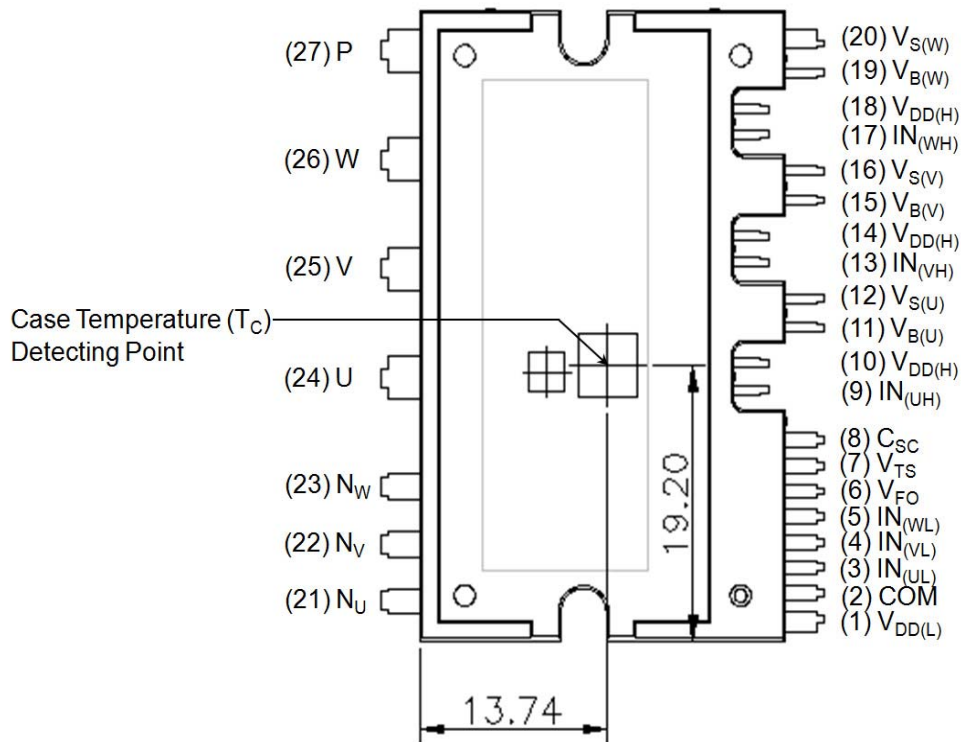


Figure 1. Top View

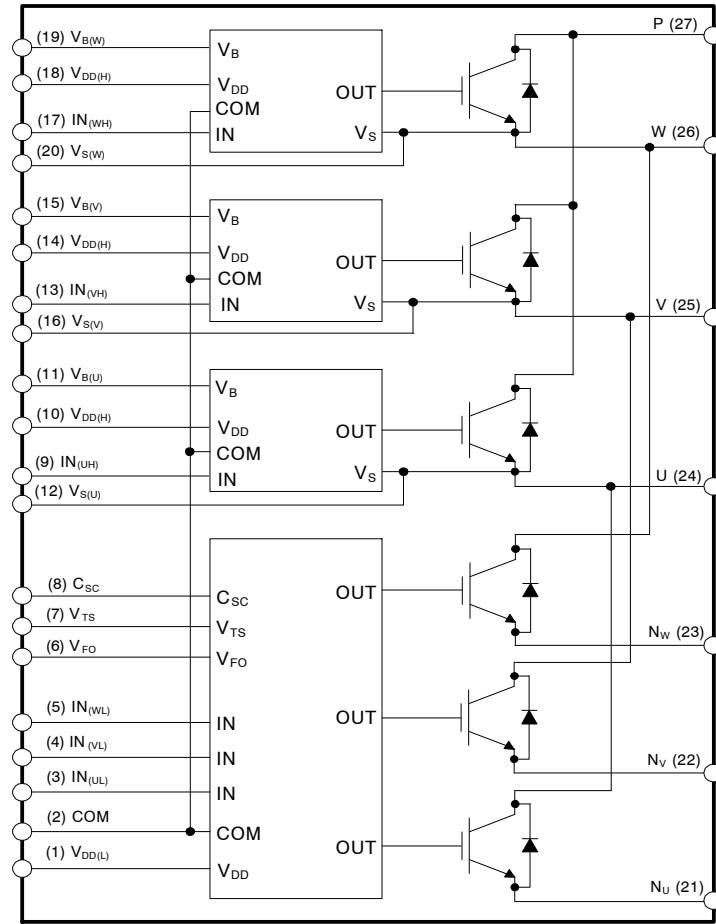
NFVA35065L32

PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	V _{DD(L)}	Low-Side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	IN _(UL)	Signal Input for Low-Side U-Phase
4	IN _(VL)	Signal Input for Low-Side V-Phase
5	IN _(WL)	Signal Input for Low-Side W-Phase
6	V _{FO}	Fault Output
7	V _{TS}	Output for LVIC Temperature Sensing Voltage Output
8	C _{SC}	Shut Down Input for Short-Circuit Current Detection Input
9	IN _(UH)	Signal Input for High-Side V-Phase
10	V _{DD(H)}	High-Side Common Bias Voltage for IC and IGBTs Driving
11	V _{B(U)}	High-Side Bias Voltage for U-Phase IGBT Driving
12	V _{S(U)}	High-Side Bias Voltage Ground for U-Phase IGBT Driving
13	IN _(VH)	Signal Input for High-Side V-Phase
14	V _{DD(H)}	High-Side Common Bias Voltage for IC and IGBTs Driving
15	V _{B(V)}	High-Side Bias Voltage for V-Phase IGBT Driving
16	V _{S(V)}	High-Side Bias Voltage Ground for V-Phase IGBT Driving
17	IN _(WH)	Signal Input for High-Side W-Phase
18	V _{DD(H)}	High-Side Common Bias Voltage for IC and IGBTs Driving
19	V _{B(W)}	High-Side Bias Voltage for W-Phase IGBT Driving
20	V _{S(W)}	High-Side Bias Voltage Ground for W-Phase IGBT Driving
21	N _U	Negative DC-Link Input for U-Phase
22	N _V	Negative DC-Link Input for V-Phase
23	N _W	Negative DC-Link Input for W-Phase
24	U	Output for U-Phase
25	V	Output for V-Phase
26	W	Output for W-Phase
27	P	Positive DC-Link Input

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INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



NOTES:

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT, and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs, freewheeling diodes, and three drive ICs for each IGBT.

Figure 2. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions	Rating	Unit
V_{PN}	Supply Voltage	Applied between P–N _U , N _V , N _W	500	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P–N _U , N _V , N _W	550	V
V_{CES}	Collector–Emitter Voltage		650	V
$\pm I_C$	Each IGBT Collector Current	$T_C = 100^\circ\text{C}$, $V_{DD} \leq 15\text{ V}$, $T_J \leq 175^\circ\text{C}$ (Note 4)	50	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25^\circ\text{C}$, $T_J \leq 175^\circ\text{C}$, Under 1 ms Pulse Width (Note 4)	100	A
P_C	Collector Dissipation	$T_C = 25^\circ\text{C}$ per One Chip (Note 4)	405	W
T_J	Operating Junction Temperature	IGBT and Diode	–40~175	$^\circ\text{C}$
		Driver IC	–40~150	

CONTROL PART

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$ –COM	20	V
V_{BS}	High–Side Control Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ –COM	–0.3– $V_{DD}+0.3$	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} –COM	–0.3– $V_{DD}+0.3$	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} –COM	–0.3– $V_{DD}+0.3$	V

TOTAL SYSTEM

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(\text{PROT})}$	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{DD} = V_{BS} = 13.5 \sim 16.5\text{ V}$, $T_J = 150^\circ\text{C}$, Non–repetitive, < 2 μs	400	V
T_{STG}	Storage Temperature		–55~175	$^\circ\text{C}$
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate	2500	V_{rms}

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance	Inverter IGBT part (per 1/6 module)	–	–	0.37	$^\circ\text{C/W}$
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	–	–	1.02	$^\circ\text{C/W}$
L_σ	Package Stray Inductance	P to N _U , N _V , N _W (Note 5)	–	24	–	nH

4. These values had been made an acquisition by the calculation considered to design factor.

5. Stray inductance per phase measured per IEC 60747–15.

ELECTRICAL CHARACTERISTICS – INVERTER PART (T_J as specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$	Collector – Emitter Saturation Voltage	$V_{DD} = V_{BS} = 15\text{ V}$, $V_{IN} = 5\text{ V}$, $I_C = 50\text{ A}$, $T_J = 25^\circ\text{C}$	–	1.75	2.25	V
		$V_{DD} = V_{BS} = 15\text{ V}$, $V_{IN} = 5\text{ V}$, $I_C = 50\text{ A}$, $T_J = 175^\circ\text{C}$		2.15	2.75	V
V_F	FWDi Forward Voltage	$V_{IN} = 0\text{ V}$, $I_F = 50\text{ A}$, $T_J = 25^\circ\text{C}$	–	1.90	2.50	V
		$V_{IN} = 0\text{ V}$, $I_F = 50\text{ A}$, $T_J = 175^\circ\text{C}$		1.95	2.55	V
HS	t_{ON}	$V_{PN} = 300\text{ V}$, $V_{DD} = 15\text{ V}$, $I_C = 50\text{ A}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \Leftrightarrow 5\text{ V}$, Inductive Load See Figure 4 (Note 6)	0.80	1.20	1.80	μs
	$t_{C(ON)}$		–	0.30	0.75	μs
	t_{OFF}		–	1.25	1.75	μs
	$t_{C(OFF)}$		–	0.15	0.60	μs
	t_{rr}		–	0.15	–	μs
LS	t_{ON}	$V_{PN} = 300\text{ V}$, $V_{DD} = 15\text{ V}$, $I_C = 50\text{ A}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \Leftrightarrow 5\text{ V}$, Inductive Load See Figure 4 (Note 6)	0.65	1.05	1.65	μs
	$t_{C(ON)}$		–	0.30	0.75	μs
	t_{OFF}		–	1.30	1.80	μs
	$t_{C(OFF)}$		–	0.25	0.60	μs
	t_{rr}		–	0.15	–	μs
I_{CES}	Collector–Emitter Leakage Current	$T_J = 25^\circ\text{C}$, $V_{CE} = V_{CES}$	–	–	3	mA

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping
NFVA35065L32	NFVA35065L32	ASPM27–CCA	10 Units/Tube

6. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information see Figure 3.

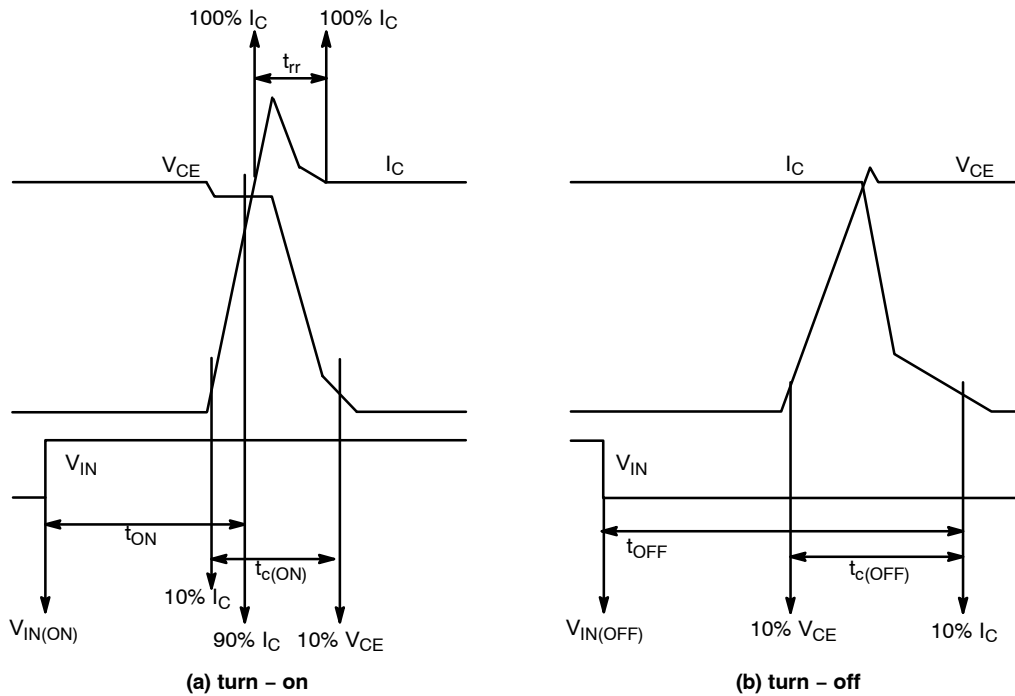


Figure 3. Switching Time Definition

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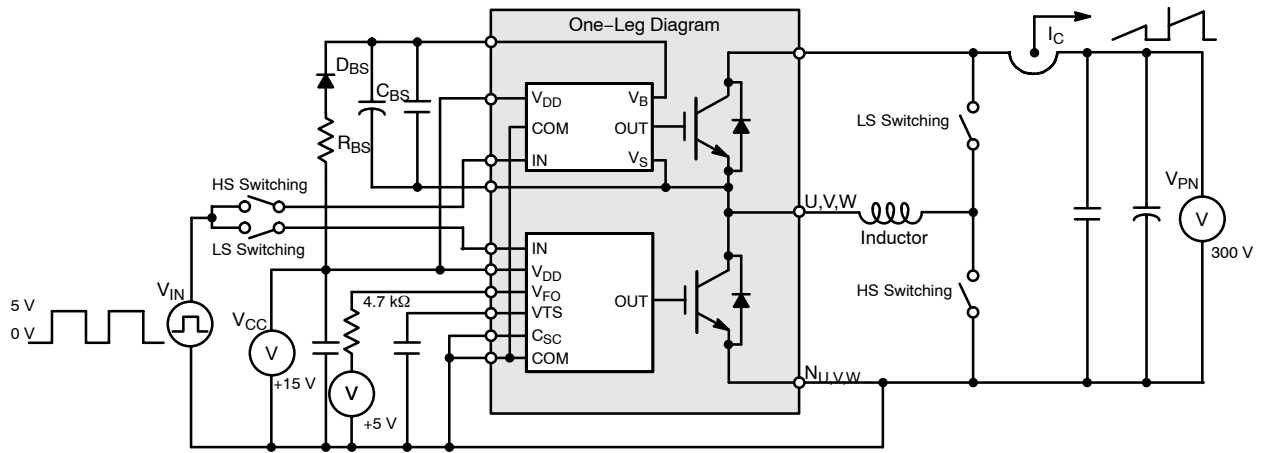


Figure 4. Example Circuit for Switching Test

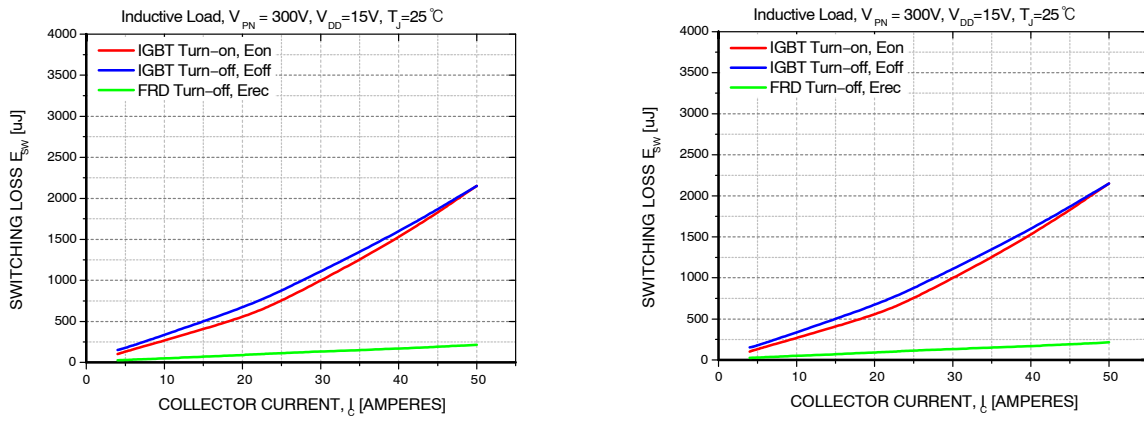


Figure 5. Switching Loss Characteristics

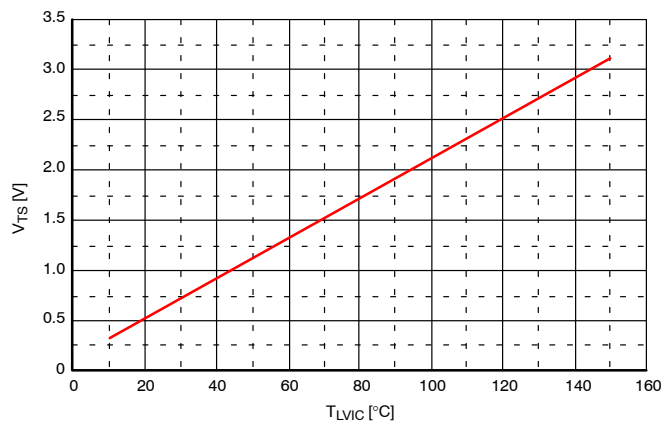


Figure 6. Temperature Profile of V_{TS} (Typical)

CONTROL PART ($T_J = 25^\circ\text{C}$)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I _{QDDH}	Quiescent V _{DD} Supply Current	V _{DD(H)} = 15 V, I _{N(UH,VH.WH)} = 0 V	V _{DD(H)} – COM	–	–	0.40	mA
I _{QDDL}		V _{DD(L)} = 15 V, I _{N(UH,VH.WH)} = 0 V	V _{DD(L)} – COM	–	–	4.80	mA
I _{PDDH}	Operating V _{DD} Supply Current	V _{DD(H)} = 15 V, f _{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High– Side	V _{DD(H)} – COM	–	–	0.48	mA
I _{PDDL}		V _{DD(L)} = 15 V, f _{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for Low– Side	V _{DD(L)} – COM	–	–	8.80	mA
I _{QBS}	Quiescent V _{BS} Supply Current	V _{BS} = 15 V, I _{N(UH,VH.WH)} = 0 V	V _{B(U)} – V _{S(U)} , V _{B(V)} – V _{S(V)} , V _{B(W)} – V _{S(W)} ,	–	–	0.24	mA
I _{PBS}	Operating V _{BS} Supply Current	V _{DD} = V _{BS} = 15 V, f _{PWM} = 20 kHz, duty = 50%, applied to one PWM signal input for High–Side	V _{B(U)} – V _{S(U)} , V _{B(V)} – V _{S(V)} , V _{B(W)} – V _{S(W)} ,	–	–	4.40	mA
V _{FOH}	Fault Output Voltage	V _{DD} = 15 V, V _{SC} = 0 V, V _{FO} Circuit: 4.7 kΩ to 5 V Pull–up		4.5	–	–	V
V _{FOL}		V _{DD} = 15 V, V _{SC} = 1 V, V _{FO} Circuit: 4.7 kΩ to 5 V Pull–up		–	–	0.50	V
V _{SC(ref)}	Short Circuit Trip Level	V _{DD} = 15 V (Note 7)	C _{SC} – COM _(L)	0.45	0.50	0.55	V
UV _{DDD}	Supply Circuit Under–Voltage Protection	Detection Level		9.80	–	13.3	V
UV _{DDR}		Reset Level		10.3	–	13.8	V
UV _{BSD}		Detection Level		9.00	–	12.5	V
UV _{BSR}		Reset Level		9.50	–	13.0	V
t _{FOD}	Fault–Out Pulse Width			50	–	–	μs
V _{TS}	LVIC Temperature Sensing Voltage Output	V _{DD(L)} = 15 V, T _{LVIC} = 25°C (Note 8) See Figure 6		540	640	740	mV
V _{IN(ON)}	ON Threshold Voltage	Applied between I _{N(UH,VH.WH)} – COM I _{N(UL,VL.WL)} – COM		–	–	2.60	V
V _{IN(OFF)}	OFF Threshold Voltage			0.80	–	–	V

7. Short–circuit current protection os functioning only at the low–sides.

8. T_{LVIC} is the temperature of LVIC itself. V_{TS} is only for sensing temperature of LVIC and can not shutdown IGBTs automatically.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P – N_U , N_V , N_W	–	300	400	V
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$ – COM, $V_{DD(L)}$ – COM	14.0	15	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	13.0	15	18.5	V
dV_{DD}/dt , dV_{BS}/dt	Control Supply Variation		–1	–	1	V/ μ s
t_{dead}	Blanking Time for Preventing Arm-Short	For Each Input Signal	2.0	–	–	μ s
f_{PWM}	PWM Input Signal	$-40^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$	–	–	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U , N_V , N_W – COM (Including Surge Voltage)	–5	–	5	V
$PW_{IN(ON)}$	Minimum Input Pulse Width	$V_{DD} = V_{BS} = 15\text{ V}$, $I_C \leq 50\text{ A}$, Wiring Inductance between $N_{U,V,W}$ and DC Link N < 10 nH (Note 9)	2.0	–	–	μ s
$PW_{IN(OFF)}$			2.0	–	–	
$PW_{IN(ON)}$		$V_{DD} = V_{BS} = 15\text{ V}$, $50\text{ A} \leq I_C \leq 100\text{ A}$, Wiring Inductance between $N_{U,V,W}$ and DC Link N < 10 nH (Note 9)	2.5	–	–	μ s
$PW_{IN(OFF)}$			2.5	–	–	
T_J	Junction Temperature		–40	–	150	$^{\circ}\text{C}$

9. This product might not make response if input pulse width is less than the recommended value.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions	Value			Unit
		Min.	Typ.	Max.	
Device Flatness	See Figure 7	0	–	+150	μm
Mounting Torque	Mounting Screw: M3 See Figure 8	0.6	0.7	0.8	N•m
		6.2	7.1	8.1	kg•cm
Terminal Pulling Strength	Load 19.8 N	10	–	–	s
Terminal Bending Strength	Load 9.8 N 90 deg. bend	2	–	–	times
Weight		–	15	–	g

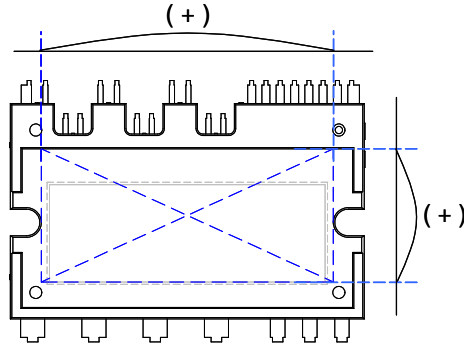


Figure 7. Flatness Measurement Position

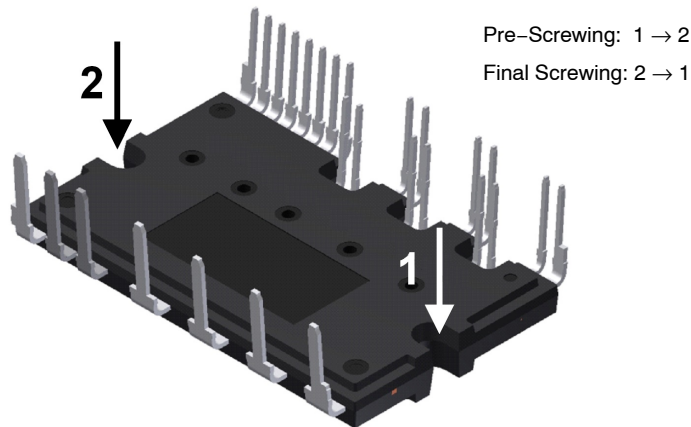
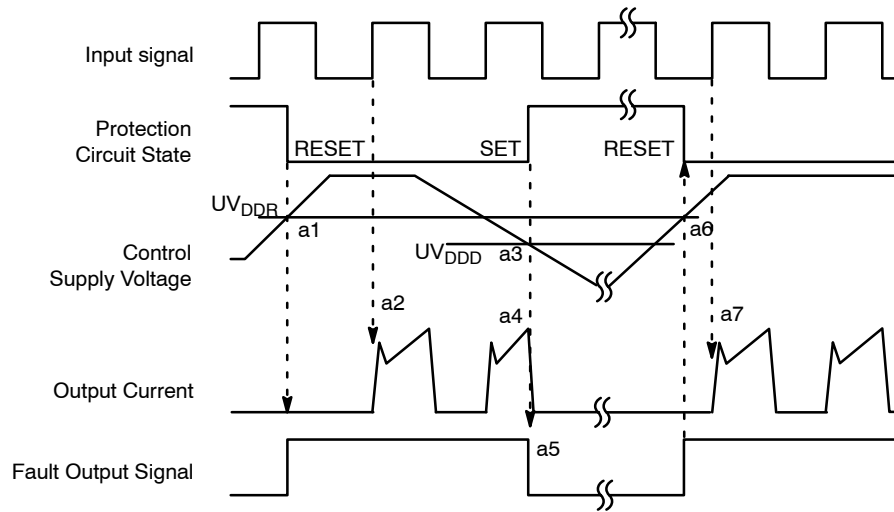


Figure 8. Mounting Screws Torque Order

NOTES:

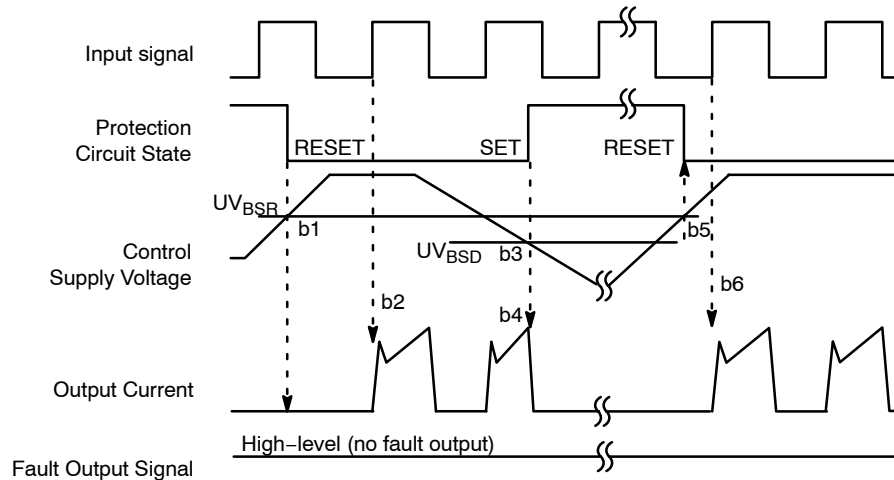
10. Do not make over torque when mounting screws. Much mounting torque may cause DBC cracks, as well as bolts and Al heat-sink destruction
11. Avoid one-sided tightening stress. Figure 8 shows the recommended torque order for mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre-screwing torque is set to 20 ~ 30% of maximum torque rating.

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- a1: Control supply voltage rises: After the voltage rises UV_{DDR} , the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under voltage detection (UV_{DD}).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts with a fixed pulse width.
- a6: Under voltage reset (UV_{DDR}).
- a7: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

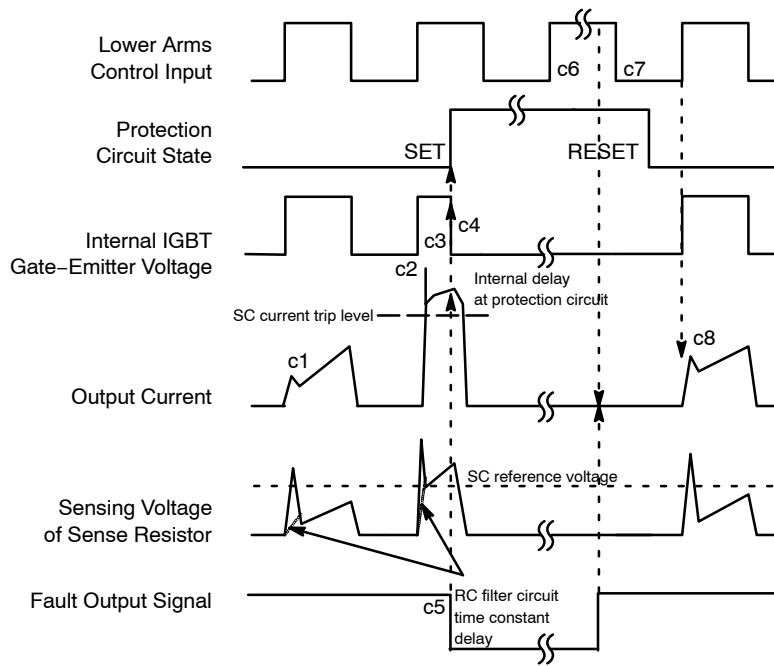
Figure 9. Under-Voltage Protection (Low-Side)



- b1: Control supply voltage rises: After the voltage rises UV_{BSR} , the circuits start to operate when next input is applied.
- b2: Normal operation: IGBT ON and carrying current.
- b3: Under voltage detection (UV_{BS}).
- b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5: Under voltage reset (UV_{BSR}).
- b6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

Figure 10. Under-Voltage Protection (High-Side)

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(with the external sense resistance and RC filter connection)

c1: Normal operation: IGBT ON and carrying current.

c2: Short circuit current detection (SC trigger).

c3: All low-side IGBT's gate are hard interrupted.

c4: All low-side IGBTs turn OFF.

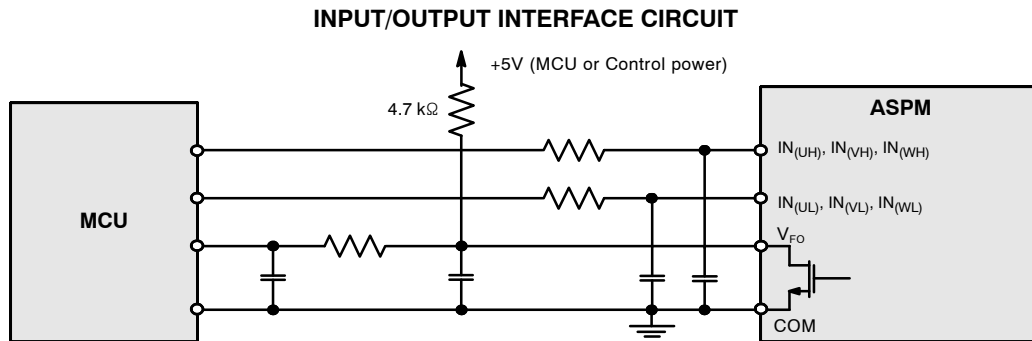
c5: Fault output operation starts with a fixed pulse width.

c6: Input HIGH: IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c7: Fault output operation finishes, but IGBT doesn't turn on until triggering next signal from LOW to HIGH.

c8: Normal operation: IGBT ON and carrying current.

Figure 11. Short-Circuit Current Protection (Low-Side Operation Only)



NOTE:

12. RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the ASPM27 product integrates 5kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Figure 12. Recommended CPU I/O Interface Circuit

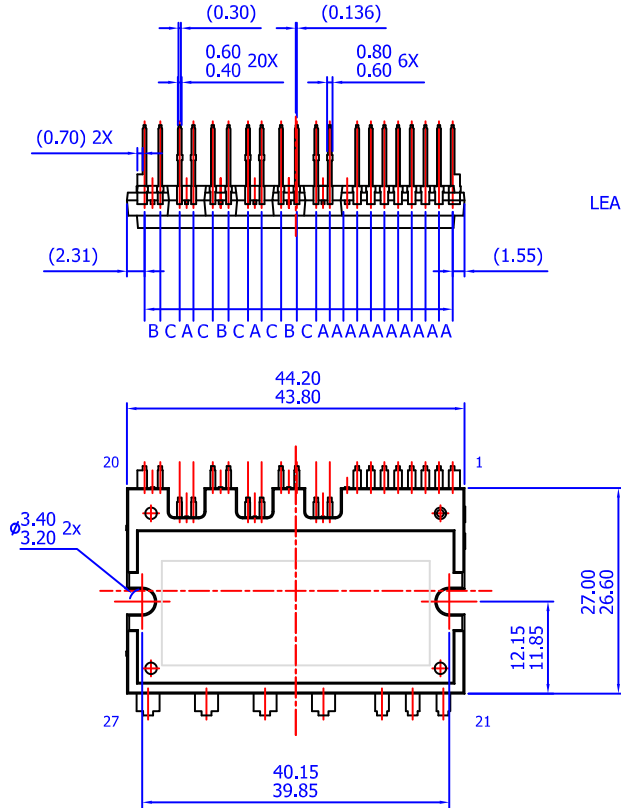
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24. Choose the electrolytic capacitor with good temperature characteristic in C₃. Also choose 0.1–0.2 μF R-category ceramic capacitors with good temperature and frequency characteristics in C₄.

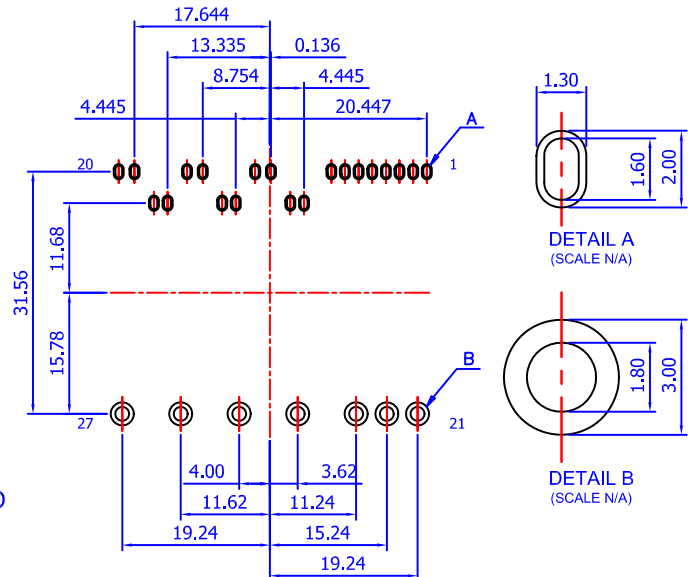
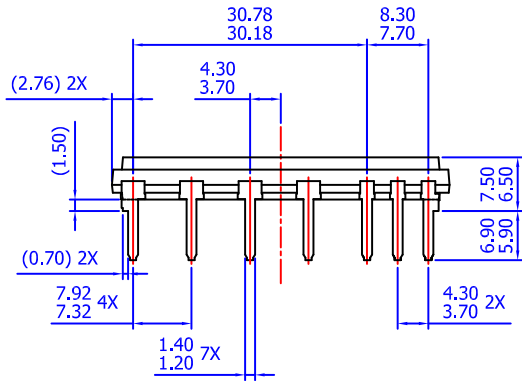
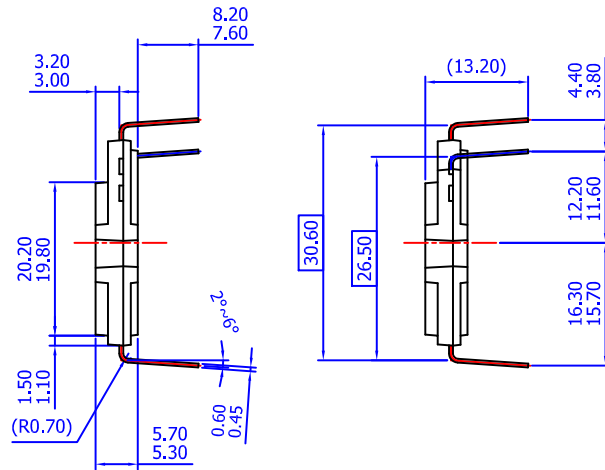
PACKAGE DIMENSIONS

SPMCA-027 / PDD STD, SPM27-CA, DBC TYPE
CASE MODFJ
ISSUE O




LEAD PITCH (TOLERANCE : ± 0.30)

A : 1.778
B : 2.050
C : 2.531



- NOTES: UNLESS OTHERWISE SPECIFIED
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B) ALL DIMENSIONS ARE IN MILLIMETERS
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