Ignition IGBT 20 A, 450 V, N-Channel D²PAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Overvoltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil-on-Plug and Driver-on-Coil Applications
- D²PAK Package Offers Smaller Footprint for Increased Board Space
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Low Threshold Voltage for Interfacing Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- This is a Pb-Free Device

Applications

• Ignition Systems

MAXIMUM RATINGS (T_{.1} = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CES}	500	V
Collector-Gate Voltage	V _{CER}	500	V
Gate-Emitter Voltage	V _{GE}	±15	V
Collector Current-Continuous @ T _C = 25°C - Pulsed	I _C	20 50	A _{DC} A _{AC}
Continuous Gate Current	I _G	1.0	mA
Transient Gate Current $(t \le 2 \text{ ms}, f \le 100 \text{ Hz})$	I _G	20	mA
ESD (Charged-Device Model)	ESD	2.0	kV
ESD (Human Body Model) R = 1500 Ω , C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω , C = 200 pF	ESD	500	V
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	150 1.0	W W/°C
Operating & Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

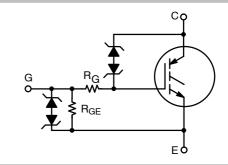
1



ON Semiconductor®

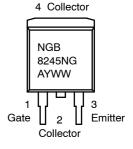
http://onsemi.com

20 A, 450 V $V_{CE(on)} \le 1.24 \text{ V } @$ $I_C = 15 \text{ A}, V_{GE} \ge 4.0 \text{ V}$



MARKING DIAGRAM

D²PAK CASE 418B STYLE 4



NGB8245N = Device Code

A = Assembly Location

Y = Year WW = Work Week G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
NGB8245NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

UNCLAMPED COLLECTOR-TO-EMITTER AVALANCHE CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Single Pulse Collector–to–Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I _L = 9.5 A, R _G = 1 k Ω , L = 3.5 mH, Starting T _C = 150°C	E _{AS}	158	mJ
THERMAL CHARACTERISTICS			
Thermal Resistance, Junction-to-Case	$R_{ heta JC}$	1.0	°C/W
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{ heta JA}$	62.5	°C/W

 T_L

°C

275

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
OFF CHARACTERISTICS (Note 3)					•		
Collector-Emitter Clamp Voltage	BV _{CES}	I _C = 2.0 mA	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	430	450	470	V
		I _C = 10 mA	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	450	475	500	
		I_C = 12 A, L = 3.5 mH, R_G = 1 k Ω (Note 4)	$T_{J} = -40^{\circ}\text{C to } 175^{\circ}\text{C}$	420	450	480	
Collector-Emitter Leakage Current	I _{CES}	V _{CE} = 15 V, V _{GE} = 0 V	T _J = 25°C		0.002	1.0	μΑ
		V_{CE} = 250 V, R_G = 1 k Ω	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	0.5	2.0	100	
Reverse Collector-Emitter Clamp	B _{VCES(R)}		T _J = 25°C	30	33	39	V
Voltage		$I_C = -75 \text{ mA}$	T _J = 175°C	31	35	40	1
			T _J = -40°C	30	31	37	
Reverse Collector-Emitter Leakage	I _{CES(R)}	V _{CE} = -24 V	T _J = 25°C	-	0.4	1.0	mA
Current			T _J = 175°C	-	20	35	
			T _J = -40°C	-	0.04	0.2	
Gate-Emitter Clamp Voltage	BV _{GES}	$I_G = \pm 5.0 \text{ mA}$	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	12	12.5	14	V
Gate-Emitter Leakage Current	I _{GES}	$V_{GE} = \pm 5.0 \text{ V}$	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	200	316	350	μΑ
Gate Resistor	R _G		$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$		70		Ω
Gate-Emitter Resistor	R _{GE}		$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	14.25	16	25	kΩ
ON CHARACTERISTICS (Note 3)				•	•		•
Gate Threshold Voltage	V _{GE(th)}		T _J = 25°C	1.5	1.8	2.1	V
		I _C = 1.0 mA, V _{GE} = V _{CE}	T _J = 175°C	0.7	1.0	1.3	1
			T _J = -40°C	1.7	2.0	2.3	
Threshold Temperature Coefficient (Negative)				4.0	4.6	5.2	mV/°C
Collector-to-Emitter On-Voltage	V _{CE(on)}	I _C = 10 A, V _{GE} = 3.7 V	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	0.8	1.11	1.97	V
		I _C = 10 A, V _{GE} = 4.0 V	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	0.8	1.10	1.85	
		I _C = 15 A, V _{GE} = 4.0 V	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	0.8	1.24	2.00	
Forward Transconductance	gfs	I _C = 6.0 A, V _{CE} = 5.0 V	T _J = 25°C	10	19	25	Mhos
DYNAMIC CHARACTERISTICS (Note	∋ 3)						
Input Capacitance	C _{ISS}			1100	1400	1600	pF
Output Capacitance	C _{OSS}	$f = 10 \text{ kHz}, V_{CE} = 25 \text{ V}$	T _J = 25°C	50	65	80	
Transfer Capacitance	C _{RSS}			15	20	25	1

Maximum Temperature for Soldering Purposes, 1/8" from case for 5 seconds (Note 2)

1. When surface mounted to an FR4 board using the minimum recommended pad size.

When surface mounted to an FR4 board using the minimum recommended pad size.
 For further details, see Soldering and Mounting Techniques Reference Manual: SOLDERRM/D.

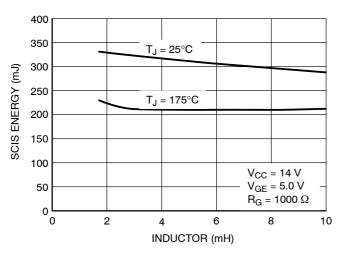
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Тур	Max	Unit
SWITCHING CHARACTERISTICS (Note 3)							
Turn-On Delay Time (Resistive) 10% V _{GE} to 10% I _C	t _{d(on)} R	V_{CC} = 14 V, R_L = 1.0 Ω , R_G = 1.0 k Ω , V_{GE} = 5.0 V	$T_{J} = -40^{\circ}\text{C to } 175^{\circ}\text{C}$	0.1	1.0	2.0	μs
Rise Time (Resistive) 10% I _C to 90% I _C	t _{rR}		$T_{J} = -40^{\circ}\text{C to } 175^{\circ}\text{C}$	1.0	3.4	6.0	
Turn-Off Delay Time (Resistive) 90% V _{GE} to 90% I _C	t _{d(off)R}	V _{CC} = 14 V, R _I = 1.0 Ω,	$T_{J} = -40^{\circ}\text{C to } 175^{\circ}\text{C}$	2.0	4.5	8.0	μs
Fall Time (Resistive) 90% I _C to 10% I _C	t _{fR}	$R_{G} = 1.0 \text{ k}\Omega, V_{GE} = 5.0 \text{ V}$	$T_{J} = -40^{\circ}\text{C to } 175^{\circ}\text{C}$	3.0	8.0	12	
Turn-Off Delay Time (Inductive) 90% V _{GE} to 90% I _C	t _{d(off)L}	V _{CE} = BV _{CES} , L = 0.5mH,	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	6.5	9.7	12.5	μs
Fall Time (Inductive) 90% I _C to 10% I _C	t _{fL}	R_G = 1.0 kΩ, I_C = 10 A, V_{GE} = 5.0 V	$T_J = -40^{\circ}\text{C} \text{ to } 175^{\circ}\text{C}$	6.0	8.3	11	

Electrical Characteristics at temperature other than 25°C, Dynamic and Switching characteristics are not subject to production testing.
 Not subject to production testing.

TYPICAL ELECTRICAL CHARACTERISTICS

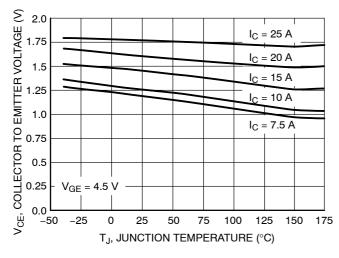
30



V_{CC} = 14 V V_{GE} = 5.0 V IA, AVALANCHE CURRENT (A) 25 $R_G = 1000 \Omega$ L = 1.8 mH20 L = 3.0 mH15 10 L = 10 mH5 0 -50 -25 0 25 50 75 100 125 150 175 T_J, JUNCTION TEMPERATURE (°C)

Figure 1. Self Clamped Inductive Switching

Figure 2. Open Secondary Avalanche Current vs. Temperature



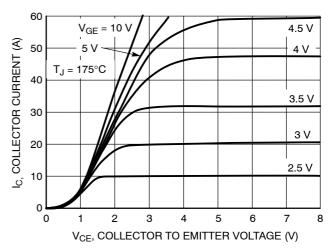
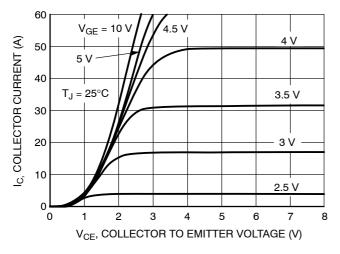


Figure 3. Collector-to-Emitter Voltage vs.
Junction Temperature

Figure 4. Collector Current vs. Collector-to-Emitter Voltage



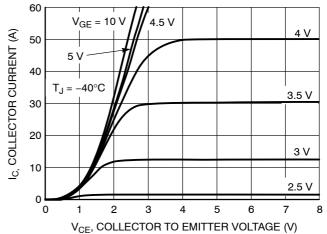


Figure 5. Collector Current vs. Collector-to-Emitter Voltage

Figure 6. Collector Current vs. Collector-to-Emitter Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

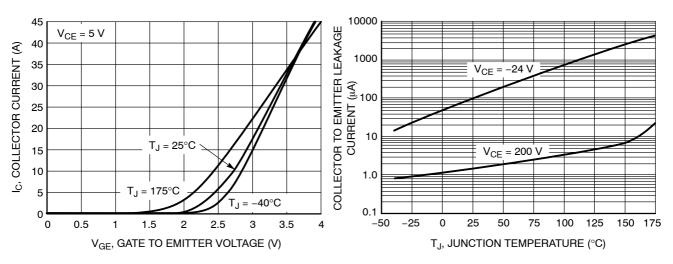


Figure 7. Transfer Characteristics

Figure 8. Collector-to-Emitter Leakage Current vs. Temperature

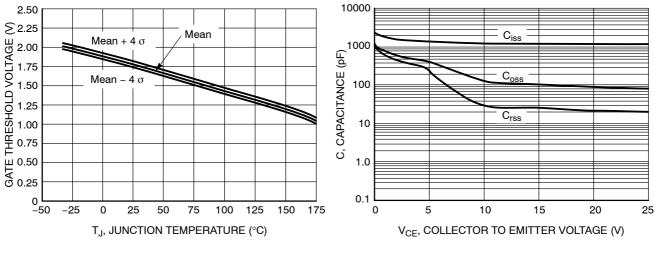


Figure 9. Gate Threshold Voltage vs.
Temperature

12 10 SWITCHING TIME (µs) t_{delay} V_{CC} = 300 V $V_{GE} = 5.0 \text{ V}$ $R_G = 1000 \Omega$ I_C = 9.0 A 2 $R_L = 33 \Omega$ 25 125 150 175 100 T_J, JUNCTION TEMPERATURE (°C)

Figure 11. Resistive Switching Fall Time vs. Temperature

Figure 10. Capacitance vs. Collector-to-Emitter Voltage

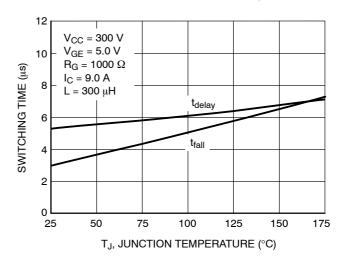


Figure 12. Inductive Switching Fall Time vs. Temperature

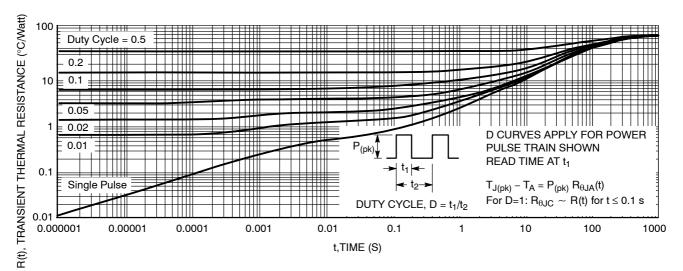


Figure 13. Minimum Pad Transient Thermal Resistance (Non-normalized Junction-to-Ambient)

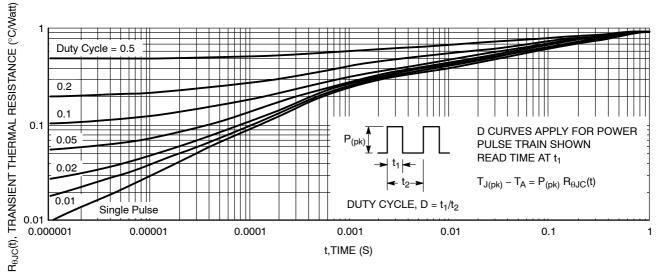
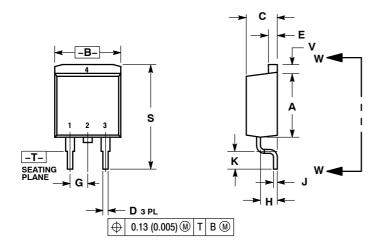


Figure 14. Best Case Transient Thermal Resistance (Non-normalized Junction-to-Case Mounted on Cold Plate)

PACKAGE DIMENSIONS

D²PAK 3 CASE 418B-04 **ISSUE K**

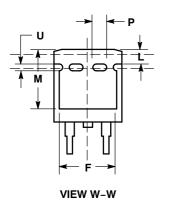


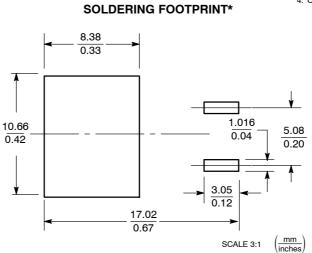
- NOTES:
 1. DIMENSIONING AND TOLERANCING
- PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.340	0.380	8.64	9.65	
В	0.380	0.405	9.65	10.29	
С	0.160	0.190	4.06	4.83	
D	0.020	0.035	0.51	0.89	
E	0.045	0.055	1.14	1.40	
F	0.310	0.350	7.87	8.89	
G	0.100	BSC	2.54 BSC		
Н	0.080	0.110	2.03	2.79	
J	0.018	0.025	0.46	0.64	
K	0.090	0.110	2.29	2.79	
L	0.052	0.072	1.32	1.83	
М	0.280	0.320	7.11	8.13	
N	0.197	REF	5.00 REF		
P	0.079	REF	2.00 REF		
R	0.039	REF	0.99 REF		
S	0.575	0.625	14.60	15.88	
V	0.045	0.055	1.14	1.40	

STYLE 4:

- PIN 1. GATE 2. COLLECTOR
 - 3. EMITTER
 - 4. COLLECTOR





*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and was are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking, ited. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910 Japan Customer Focus Center

Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative