National Semiconductor

NM59C11 1024-Bit Serial EEPROM 64 x 16-Bit or 128 x 8-Bit Configurable with Programming Status

General Description

The NM59C11 is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or as 128 8-bit registers. The organization is determined by the status of the ORG input. This memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM59C11 is available in an SO package for small space considerations.

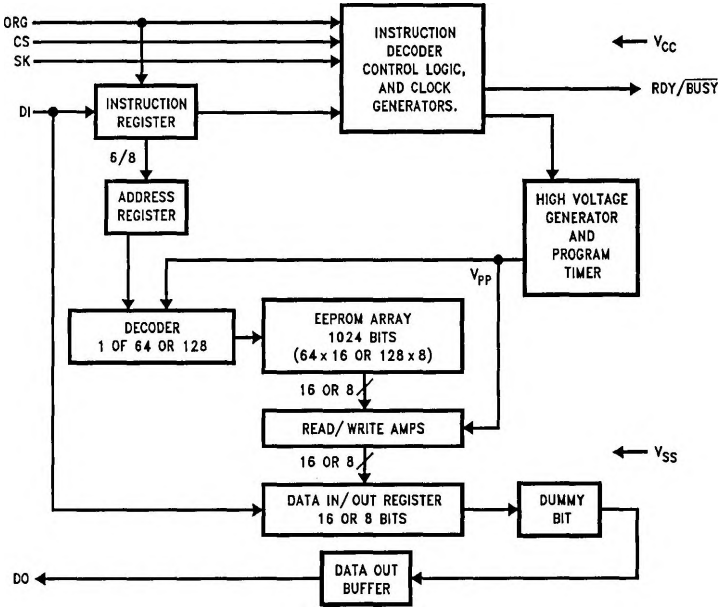
The interface that controls the EEPROM is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 6 instructions that operate the NM59C11: Read, Erase/Write Enable, Write, Erase/Write Disable, Write All, and Erase All. The device programming status is output on the RDY/$\overline{\text{BUSY}}$ output.

The NM59C11 has programming status in adddition to the functions found in the NM93C46A.

Features

- Device status during programming mode
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct Write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes (also available with 3.0V to 5.5V)
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

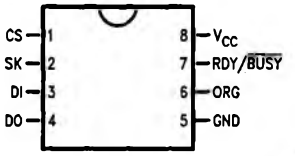
Block Diagram



TL/D/11051–1

Connection Diagram

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/11051-2

Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization
RDY/$\overline{BUSY}$	Programming Status

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM59C11N
NM59C11M8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM59C11EN
NM59C11EM8

Military Temp. Range (−55°C to +125°C)

Order Number
NM59C11MN
NM59C11MM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM59C11	0°C to +70°C
NM59C11E	−40°C to +85°C
NM59C11M	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified)

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM59C11 NM59C11E MN59C11M	CS = V_{IH}, SK = 1 MHz SK = 1.0 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM59C11 NM59C11E MN59C11M	CS = V_{IH}, SK = 1 MHz SK = 1.0 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM59C11 NM59C11E NM59C11M	CS = 0V		50 100 100	μA
I_{IL}	Input Leakage	NM59C11 NM59C11E NM59C11M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NM59C11 NM59C11E NM59C11M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM59C11 NM59C11E NM59C11M	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NM59C11 NM59C11E NM59C11M		0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM59C11 NM59C11E NM59C11M	(Note 2) (Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM59C11 NM59C11E NM59C11M	(Note 2) (Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup Time	NM59C11 NM59C11E NM59C11M	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM59C11 NM59C11E NM59C11M	(Note 4) (Note 4) (Note 5)	250 250 500		ns
t_{CSS}	CS Setup Time	NM59C11 NM59C11E NM59C11M	Relative to SK	50 50 100		ns

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DH}	DO Hold Time		Relative to SK	10		ns
t_{DIS}	DI Setup Time	NM59C11A NM59C11AE NM59C11AM	Relative to SK	100 100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		
t_{PD1}	Output Delay to "1"	NM59C11A NM59C11AE NM59C11AM	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM5911A NM59C11AE NM59C11AM	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM59C11A NM59C11AE NM59C11AM	AC Test CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specfication is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in a SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SLK} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the mimimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM59C11 has 6 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8/9 bits carry the op code and the 6/7-bit address for register selection.

Read (READ)

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into an 8- or 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 8- or 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN)

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

RDY/BUSY

The NM59C11 has a separate output that indicates if the device is in the programming mode. It enters the programming mode when the last data bit is clocked in. When it enters the programming mode, the NM59C11 drives the RDY/BUSY output low. After it completes the programming mode, it drives the RDY/BUSY output high. The RDY/BUSY output remains at a high level at all times except while the device is in the programming mode.

Program (PROGRAM)

The program instruction is used to write data into an 8- or 16-bit register at the specified address. When the last data bit is clocked in, the NM59C11 automatically enters the programming mode. While the device is in the programming mode it cannot accept any other instructions and the RDY/BUSY output is driven low to indicate BUSY. When the device has completed the internally timed programming cycle, the RDY/BUSY output is driven high to indicate it is ready to accept the next instruction.

The Chip Select (CS) input does not need to be driven low to initiate the programming cycle, but it must be driven low for the minimum CS low timer (t_{CS} = 250 μs) before a new cycle can be initiated.

Erase All (ERAL)

The ERAL instruction will erase all memory registers simultaneously (all bits set to a logical "1"). To initiate the internal programming mode, an 8- or 16-bit data field must be clocked in, although the contents of the data field are "don't care" in this instruction. The internally timed programming cycle will be initiated when the last data bit is clocked in. As with the Program mode, the RDY/BUSY line will indicate when the device is able to accept the next instruction.

The Chip Select (CS) input does not need to be driven low to initiate the internal programming cycle, but it must be driven low for the minimum chip select low time (t_{CS} = 250 ns) before a new cycle can be initiated.

Write All (WRAL)

The WRAL instruction will write the same data into all memory registers simultaneously. The address field is "don't care" in this instruction, although must be clocked in. The internal programming cycle is initiated when the last data bit is clocked in. As with the Program mode, the RDY/BUSY output indicates when the device is ready to accept the next instruction.

The Chip Select (CS) input does not need to be driven low to initiate the internal programming cycle, but it must be driven low for the minimum chip select low time (t_{CS} = 250 ns) before a new cycle can be initiated.

Erase/Write Disable (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

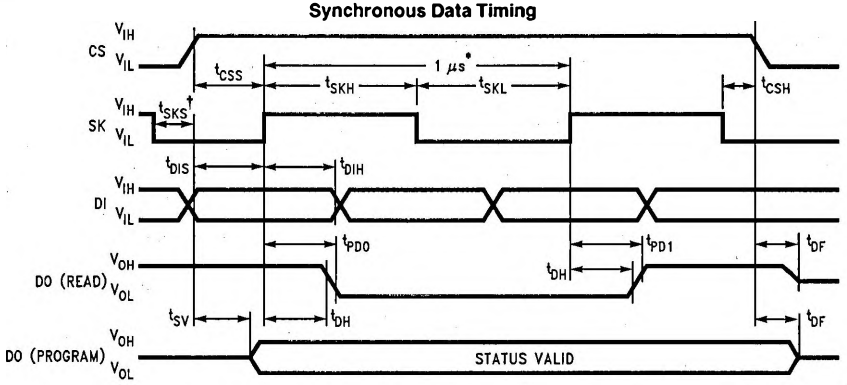
Instruction Set

Instruction	Start Bit	Opcode	Address*		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A6–A0	A5–A0			Read Address AN–A0
PROGRAM	1	0100	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0011	XXXXXXX	XXXXXX			Program Enable
EWDS	1	0000	XXXXXXX	XXXXXX			Program Disable
ERAL	1	0010	XXXXXXX	XXXXXX			Erase All Addresses
WRAL	1	0001	XXXXXXX	XXXXXX	D7–D0	D15–D0	Program All Addresses

*It is necessary to clock in the "Don't Care" address bits.

Timing Diagrams

Synchronous Data Timing

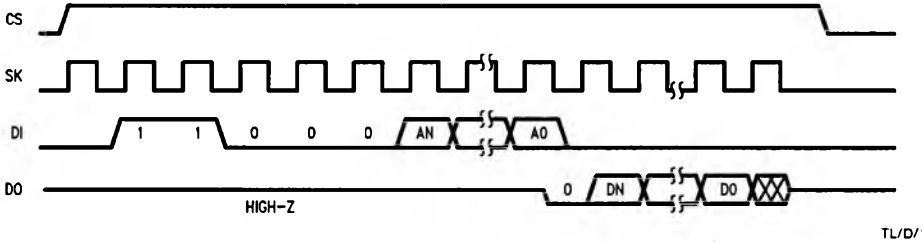


TL/D/11051–13

*This is the minimum SK period (Note 2).

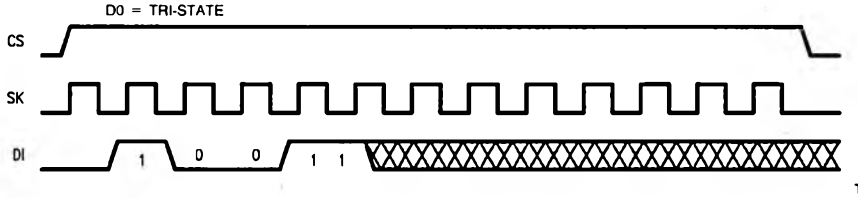
†t_{SKS} is not needed if D1 = V_{IL} when CS is going active (HIGH).

READ



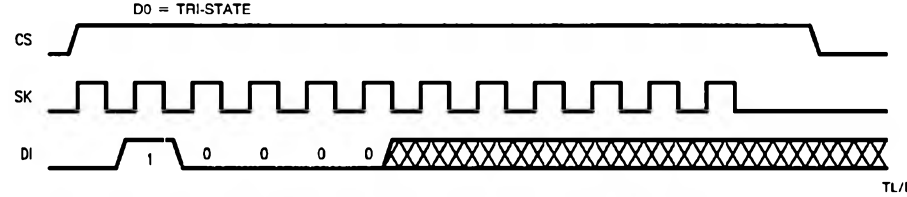
TL/D/11051–4

EWEN



TL/D/11051–5

EWDS†

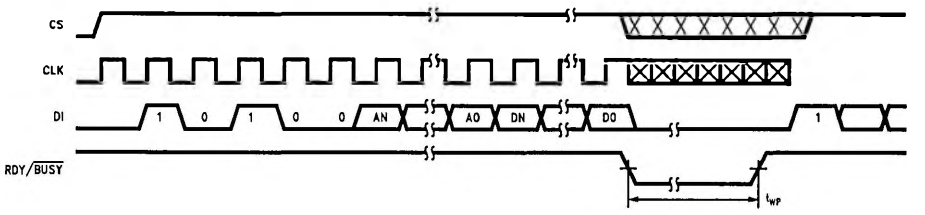


TL/D/11051–6

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a number of clock cycles after the last bit of opcode is clocked in. In the 64 x 16 configuration, 6 additional clock cycles are required. In the 128 x 8 configuration, 7 additional clock cycles are required.

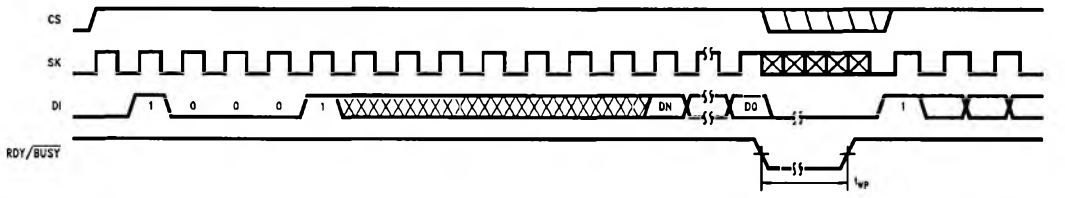
Timing Diagrams (Continued)

WRITE



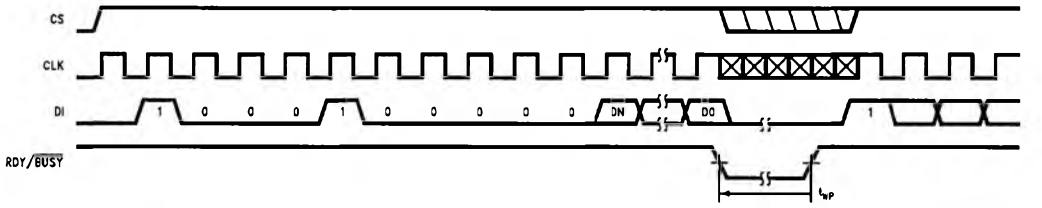
TL/D/11051–7

WRAL (128 x 8 Organization)



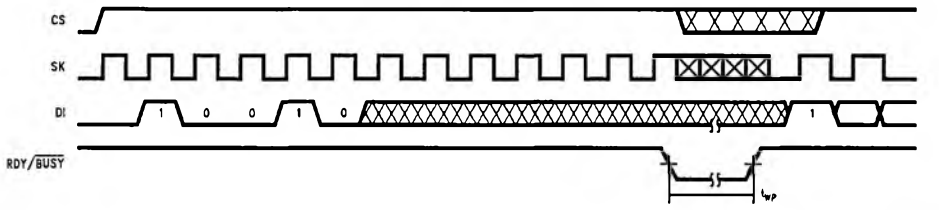
TL/D/11051–8

WRAL (64 x 16 Organization)



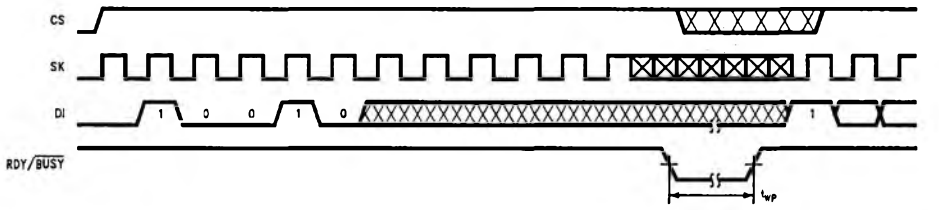
TL/D/11051–9

ERAL† (128 x 8 Organization)



TL/D/11051–11

ERAL† (64 x 16 Organization)



TL/D/11051–12

†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a number of clock cycles after the last bit of opcode is clocked in. In the 64 x 16 configuration, 6 additional clock cycles are required. In the 128 x 8 configuration, 7 additional clock cycles are required.