# **Power MOSFET**

# 30 V, 18 A, Single N-Channel, SO-8

#### **Features**

- Ultra Low R<sub>DS(on)</sub> (at 4.5 V<sub>GS</sub>), Low Gate Resistance and Low Q<sub>G</sub>
- Optimized for Low Side Synchronous Applications
- High Speed Switching Capability
- Pb-Free Package is Available

### **Applications**

- Notebook Computer Vcore Applications
- Network Applications
- DC-DC Converters

#### **MAXIMUM RATINGS** (T<sub>J</sub> = 25°C unless otherwise noted)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	30	V
Gate-to-Source Voltage			$V_{GS}$	±20	V
Continuous Drain	Steady	T <sub>A</sub> = 25°C	I <sub>D</sub>	15	Α
Current (Note 1)	State T <sub>A</sub> = 85°C			11	
	t ≤10 s	T <sub>A</sub> = 25°C		18	
Power Dissipation (Note 1)	Steady State T <sub>A</sub> = 25°C		P <sub>D</sub>	1.67	W
	t ≤10 s			2.5	
Continuous Drain	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	11	Α
Current (Note 2)		T <sub>A</sub> = 85°C		8.0	
Power Dissipation (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	0.93	W
Pulsed Drain Current	t <sub>p</sub> = 10 μs		I <sub>DM</sub>	56	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Continuous Source Current (Body Diode)			IS	3.0	Α
Single Pulse Drain–to–Source Avalanche Energy (V $_{DD}$ = 30 V, V $_{GS}$ = 10 V, I $_{PK}$ = 32 A, L = 1 mH, R $_{G}$ = 25 $\Omega$ )		E <sub>AS</sub>	512	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

### THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	75	°C/W
Junction-to-Ambient – $t \le 10 s$ (Note 1)	$R_{\theta JA}$	50	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	135	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

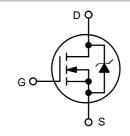
- Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [1 oz] including traces).
- Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412" sq.).



## ON Semiconductor®

#### http://onsemi.com

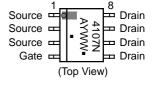
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
30 V	3.4 mΩ @ 10 V	18 A
30 V	4.7 mΩ @ 4.5 V	107



#### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8 CASE 751 STYLE 12



4107N = Specific Device Code A = Assembly Location

Y = Year WW = Work Week ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTMS4107NR2	SO-8	2500/Tape & Reel
NTMS4107NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	-			-		<u>-</u>	<u>-</u>
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				21		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	.,	T <sub>J</sub> = 25°C			1.0	μΑ
		$V_{GS} = 0 \text{ V}, V_{DS} = 24 \text{ V}$	T <sub>J</sub> = 125°C			10	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} =$				±100	nA
ON CHARACTERISTICS (Note 3)					-		
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 2$	250 μΑ	1.0		2.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				7.4		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> =	= 14 A		4.7	5.5	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> =	: 15 A		3.4	4.5	
Forward Transconductance	9FS	V <sub>DS</sub> = 15 V, I <sub>D</sub> =	: 18 A		25		S
CHARGES, CAPACITANCES AND GATE R	ESISTANCE				•		•
Input Capacitance	C <sub>ISS</sub>				6000		pF
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz	, V <sub>DS</sub> = 15 V		1030		1
Reverse Transfer Capacitance	C <sub>RSS</sub>				550		
Total Gate Charge	Q <sub>G(TOT)</sub>				45		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V}, I_{D} = 18 \text{ A}$			6.5		1
Gate-to-Source Charge	$Q_{GS}$				16.3		1
Gate-to-Drain Charge	$Q_{GD}$				19.3		
Gate Resistance	$R_{G}$				0.60		Ω
SWITCHING CHARACTERISTICS (Note 4)	•						
Turn-On Delay Time	t <sub>d(ON)</sub>				9.0		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> =	= 15 V		10		
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$I_D = 1.0 \text{ A}, R_G = 6.0 \Omega$			94		1
Fall Time	t <sub>f</sub>				38		
DRAIN-SOURCE DIODE CHARACTERISTI	cs				•		
Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3.0 A	T <sub>J</sub> = 25°C		0.8	1.1	V
			T <sub>J</sub> = 125°C		0.6		1
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } d_{IS}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 3.0 \text{ A}$			41		ns
Charge Time	t <sub>a</sub>				20		1
Discharge Time	t <sub>b</sub>				21		1
Reverse Recovery Charge	Q <sub>RR</sub>				48		nC

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

#### TYPICAL PERFORMANCE CURVES

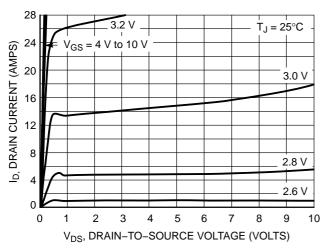
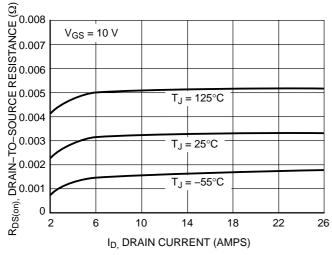


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



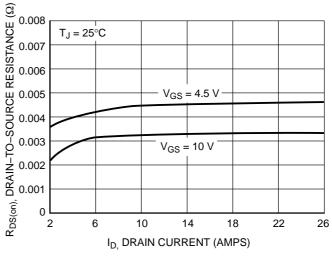
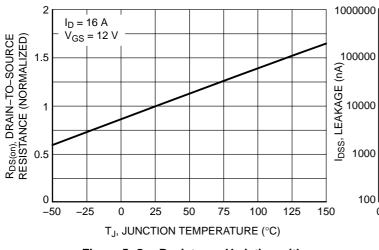


Figure 3. On–Resistance vs. Drain Current and Temperature

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



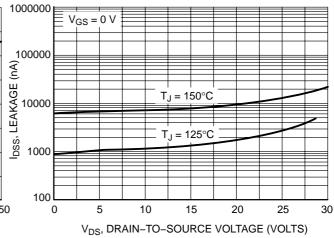
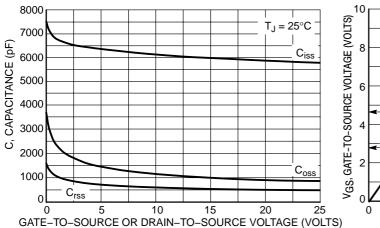


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

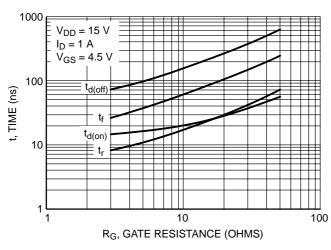
#### TYPICAL PERFORMANCE CURVES



10 V<sub>GS</sub>
V<sub></sub>

Figure 7. Capacitance Variation

Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge



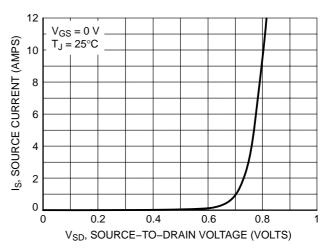


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

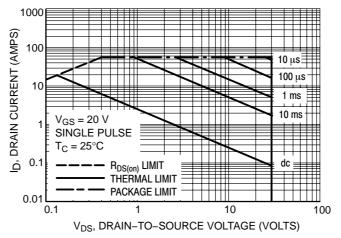
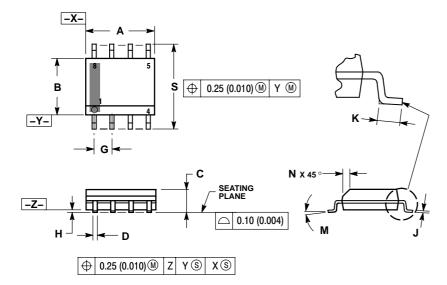


Figure 11. Maximum Rated Forward Biased Safe Operating Area

#### PACKAGE DIMENSIONS

SO-8 CASE 751-07 **ISSUE AG** 



#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER

- DIMENSIONING AND TOLERANCING PER ANSI Y14-5M, 1982.
  CONTROLLING DIMENSION: MILLIMETER. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- PER SIDE.

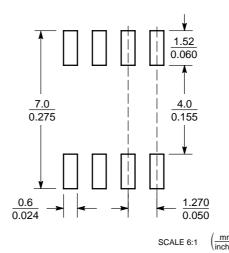
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

	MILLIMETERS		INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	4.80	5.00	0.189	0.197		
В	3.80	4.00	0.150	0.157		
C	1.35	1.75	0.053	0.069		
D	0.33	0.51	0.013	0.020		
O	1.27 BSC		0.05	.050 BSC		
Н	0.10	0.25	0.004	0.010		
J	0.19	0.25	0.007	0.010		
K	0.40	1.27	0.016	0.050		
М	0 °	8 °	0 °	8 °		
Ν	0.25	0.50	0.010	0.020		
s	5.80	6.20	0.228	0.244		

- STYLE 12: PIN 1. SOURCE
  - 2. SOURCE
  - SOURCE GATE 3.
  - 4. 5. DRAIN
  - DRAIN
  - DRAIN
  - 8. DRAIN

## **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use a components in systems intended for surgical implant into the body, or other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082–1312 USA Phone: 480–829–7710 or 800–344–3860 Toll Free USA/Canada Fax: 480–829–7709 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center 2–9–1 Kamimeguro, Meguro–ku, Tokyo, Japan 153–0051 Phone: 81–3–5773–3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.