Power MOSFET

30V, 7 m Ω , 89A, Single N-Channel SO8FL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified
- These are Pb-Free Devices

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	30	V
Gate-to-Source Voltage	Gate-to-Source Voltage		V _{GS}	±20	V
Continuous Drain Cur-		T _{mb} = 25°C	I _D	89	Α
rent R $_{\Psi J-mb}$ (Notes 1, 2, 3, 4)	Steady	T _{mb} = 100°C		63	
Power Dissipation	State	T _{mb} = 25°C	P_{D}	112	W
R _{ΨJ-mb} (Notes 1, 2, 3)		$T_{mb} = 100^{\circ}C$		56	
Continuous Drain Current R _{B.IA} (Notes 1 &		T _A = 25°C	I _D	16	Α
3, 4)	Steady	T _A = 100°C		11	
Power Dissipation	State	T _A = 25°C	P_{D}	3.7	W
R _{θJA} (Notes 1, 3)		T _A = 100°C		1.8	
Pulsed Drain Current	$T_A = 25^{\circ}C, t_p = 10 \mu s$		I _{DM}	336	Α
Current limited by package T _A = 25°C (Note 4)		I _{DmaxPkg}	80	Α	
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 175	°C
Source Current (Body Diode)			I _S	51	Α
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, V _{DD} = 24 V, V _{GS} = 10 V, $I_{L(pk)}$ = 19 A, L = 1.0 mH, R_G = 25 Ω)		E _{AS}	180	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

		-	
Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) - Steady State (Note 2, 3)	$R_{\Psi J-mb}$	1.3	°C/W
Junction-to-Ambient - Steady State (Note 3)	Rela	41	1

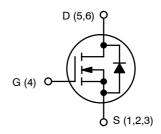
- 1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
- 3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- 4. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



ON Semiconductor®

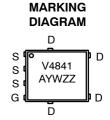
http://onsemi.com

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
30 V	7.0 mΩ @ 10 V	00.4
30 V	11.4 mΩ @ 4.5 V	89 A



N-CHANNEL MOSFET





Α = Assembly Location

= Year W = Work Week 77 = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NVMFS4841NT1G	SO-8FL (Pb-Free)	1500 / Tape & Reel
NVMFS4841NT3G	SO-8FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•					1	•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				25		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25 °C			1	
		V _{DS} = 30 V	T _J = 125°C			10	μΑ
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 V, V_{GS}$	= ±20 V			±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		1.5		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.6		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A		4.7	7.0	
		V _{GS} = 4.5 V	I _D = 30 A		9.2	11.4	mΩ
Forward Transconductance	9FS	V _{DS} = 15 V, I _E	₎ = 15 A		16		S
CHARGES AND CAPACITANCES	•					•	
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 12 V			1436		pF
Output Capacitance	C _{OSS}				348		
Reverse Transfer Capacitance	C _{RSS}				177		
Total Gate Charge	Q _{G(TOT)}				11.5	17	
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V}; I_D = 30 \text{ A}$			2.0		nC
Gate-to-Source Charge	Q _{GS}				5.0		
Gate-to-Drain Charge	Q_{GD}				5.1		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 30 A			25.4		nC
SWITCHING CHARACTERISTICS (Note 6)				•	•	•	
Turn-On Delay Time	t _{d(ON)}				13.5		
Rise Time	t _r	V _{GS} = 4.5 V, V _{DS} = 1	5 V. In = 15 A.		66.5		1
Turn-Off Delay Time	t _{d(OFF)}	$R_{\rm G} = 3.0 \Omega$			15.5		ns
Fall Time	t _f				7.5		
DRAIN-SOURCE DIODE CHARACTERISTIC	s	•		•	•		
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 30 A	T _J = 25°C		0.9	1.2	
			T _J = 125°C		0.8		_ v
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 30 \text{ A}$			20.5		
Charge Time	t _a				11.6		ns
Discharge Time	t _b				8.9		1
Reverse Recovery Charge	Q _{RR}				10.7		nC

^{5.} Pulse Test: pulse width \leq 300 μ s, duty cycle \leq 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

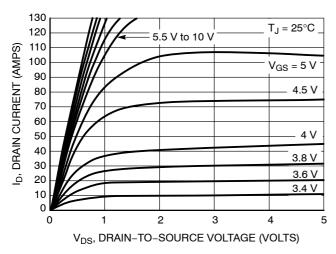


Figure 1. On-Region Characteristics

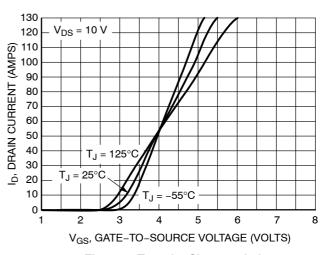


Figure 2. Transfer Characteristics

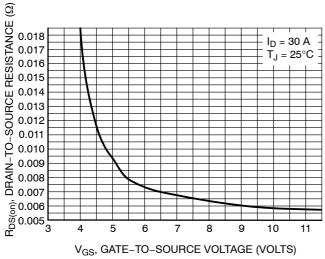


Figure 3. On-Resistance vs. Gate-to-Source Voltage

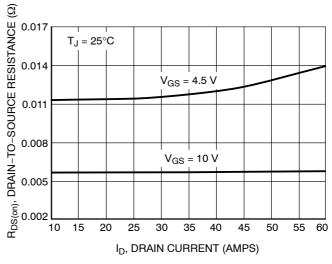


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

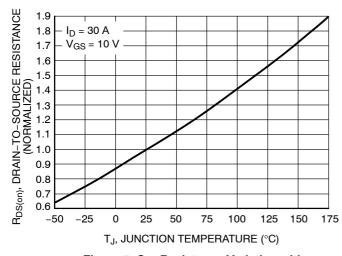


Figure 5. On–Resistance Variation with Temperature

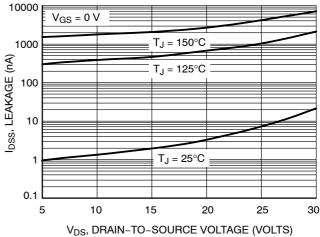
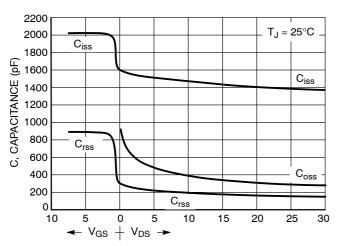


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

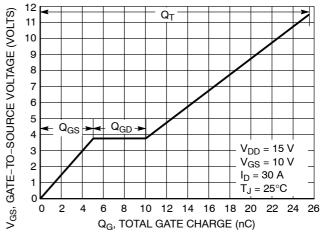


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge



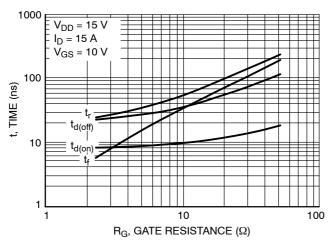


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

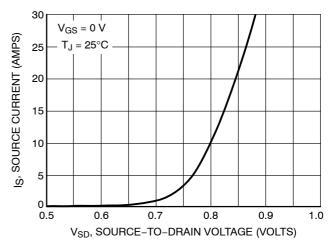


Figure 10. Diode Forward Voltage vs. Current

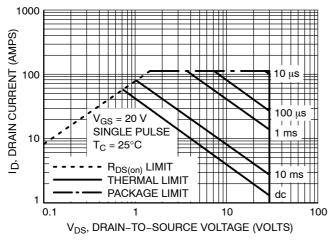


Figure 11. Maximum Rated Forward Biased Safe Operating Area

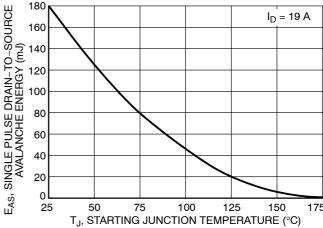


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL PERFORMANCE CURVES

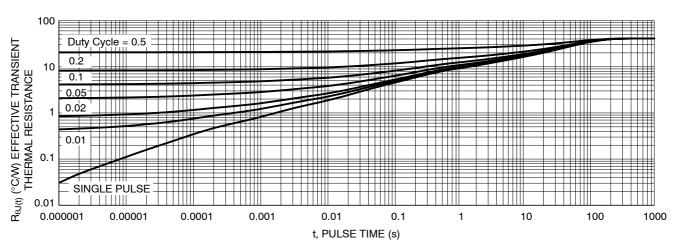
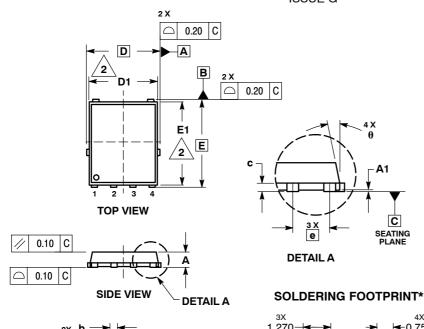


Figure 13. FET Thermal Response

PACKAGE DIMENSIONS



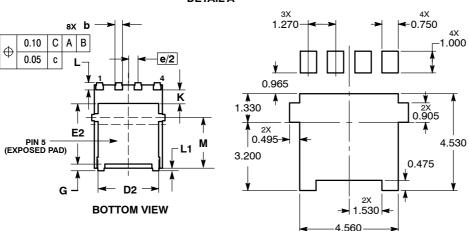


NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			
DIM	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
A1	0.00		0.05	
b	0.33	0.41	0.51	
С	0.23	0.28	0.33	
D	5.15 BSC			
D1	4.50	4.90	5.10	
D2	3.50		4.22	
E	6.15 BSC			
E1	5.50	5.80	6.10	
E2	3.45		4.30	
е	1.27 BSC			
G	0.51	0.61	0.71	
K	1.20	1.35	1.50	
L	0.51	0.61	0.71	
L1	0.05	0.17	0.20	
M	3.00	3.40	3.80	
θ	0 °		12 °	

- STYLE 1: PIN 1. SOURCE
 - 2. SOURCE
 - 3. SOURCE
 - GATE DRAIN



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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