National Semiconductor

PRELIMINARY
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PC87550
PicoPower North Bridge—PCI System Controller

General Description

A high-performance, highly integrated system controller for Microsoft® Windows®-compatible computers, the PC87550 significantly improves upon the performance offered by current system-logic solutions. The PCI-based system controller is optimized for portable multimedia systems with critical form-factor and power consumption requirements.

The PC87550 supports full PCI, DRAM, CPU, and L2-cache concurrency. It achieves a more effective utilization of the CPU bus by allowing the CPU execution to continue while the PCI Master is accessing the DRAM.

The presence of two independent write buffers improves performance by allowing PCI memory writes and DRAM memory writes/reads to occur concurrently. The PC87550 also supports the concurrent operation of an external PCI Master and a Pentium processor.

The PC87550 supports sustained PCI bursting of up to 120 Mbytes per second. It can achieve a sustained burst rate of x-1-1-1-1.... for both CPU-to-PCI and PCI Master-to-DRAM accesses.

The PC87550 system controller integrates the following functions in a single 388-pin BGA package:

- CPU-to-PCI bus interface controller/arbiter
- L2-cache controller
- DRAM controller
- Power management controller
- Data path controller
- SmartDock™ and SmartDock-II hot-docking interface

The level-2 cache controller supports synchronous burst, and pipelined synchronous SRAM.

It supports cache sizes ranging from 256 Kbytes to 512 Kbytes. Additionally, buffered write-through cache update schemes allow further performance gains by not stalling the CPU on L1 writeback cycles.

A sophisticated DRAM controller supports leading-edge 3.3V DRAM technologies. Support for synchronous DRAM allows the PC87550 to achieve improved performance in a cacheless system configuration. The DRAM controller implements the logic required to use high-speed DRAM, reducing the performance overhead of the L2-cache miss cycles. It provides a synchronous interface between the CPU and PCI buses to exploit the maximum potential of the PCI bandwidth.

Active and passive power management features enable systems with superior power and thermal management. PC87550 supports both legacy and Advanced Configuration and Power management Interface (ACPI) implementations. A special thermal control mechanism uses CPU clock throttling to efficiently control the power consumption and heat dissipation associated with the processor. An innovative programming model simplifies the BIOS development task without compromising any of the power management features.

The PC87550 provides a 32- or 64-bit data path between the CPU and the main memory; a 32-bit data path between the CPU bus and the PCI Local bus; and a 32-bit data path between the PCI Local bus and the main memory.

PC87560 PCI system I/O controller complements the PC87550 solution by providing a highly integrated bridge between the PCI and ISA buses. Both devices contain the necessary logic to support master and slave cycles on both PCI and ISA buses.

To enable a full-featured docking station design, the PC87550 provides all the hooks required to support PCI hot-warm-, and cold-docking. It is fully optimized to work with PC87560 and the NILE II devices to support a full secondary ISA bus in the PCI docking station, thus allowing PCI and ISA slots in the docking station. The PC87550 also implements the docking interface control logic to enable port replicator dock and PCI hot-, warm-, and cold-docking. This interface provides a seamless support for docking without requiring external logic.

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The 388-pin BGA packaging offers a sleek, durable package with good thermal properties and noise immunity. The device comes with full technical and hardware support, including samples, evaluation boards, and design examples.

Features

- Optimized single-chip PCI system controller for Intel® Pentium® processors
  - — Processor bus speeds of 50-, 60-, and 66-MHz
  - — Supports 5-class processors from AMD® and Cyrix®
  - — Supports processors with 3.2V or 2.5V CPU bus interface
  - — Supports level-1 write-back or write-through cache
  - — Supports both toggle and linear burst sequences
  - — Supports CPU address pipelining
  - — Optimized for Multimedia Extension (MMX) processors

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Windows® is a registered trademark of Microsoft Corporation.
AMD® is a registered trademark of Advanced Micro Devices, Inc.
Cyrix® is a registered trademark of
SmartDock™ is a trademark of

Features (Continued)

- 64-bit direct-mapped, write-through L2-cache controller
  - — Supports either a cacheless configuration or cache sizes of 256 Kbytes to 512 Kbytes with a 32-byte line size
  - — Supports synchronous burst and pipelined burst SRAM
  - — Supports 5V TAG RAM
- State-of-the-art DRAM controller
  - — 4 Mbytes to 256 Mbytes of system memory
  - — Supports 3.3V/5V Fast Page Mode (FPM), Extended Data Output (EDO), and Synchronous DRAM (SDRAM) in the mixed mode with auto-detect capability
  - — Allows mixing of 64- and 32-bit DRAM in non-SDRAM banks
  - — Supports up to 6 banks of 64-bit DRAM/SDRAM or 12 banks of 32-bit DRAM (non-SDRAM)
  - — Supports two concurrent write buffers—one 8-level, 64-bit DRAM write-buffer and one 16-level 32-bit PCI write buffer
    - − Supports 2-1-1-1 burst write (CPU bus)
    - − Supports read reordering
  - — Supports 512 Kbit, 1 Mbit, 2 Mbit, 4 Mbit, 16 Mbit, and 64 Mbit symmetric or asymmetric DRAM
  - — Slow/self-refresh support, including hidden, staggered, CAS-before-RAS refresh or RAS-only refresh
  - — Supports sustained bursting of 1-1-1-1 for Synchronous DRAM (SDRAM) for CPU pipelined back-to-back cycles with hidden lead-off
    - − 6-2-2-2 burst read cycles with 60 ns EDO DRAM at 66 MHz
    - − 6-1-1-1 burst read cycles with SDRAM
    - − 6-3-3-3 page-hit and 10-3-3-3 page-miss burst-read cycles with 60 ns standard DRAM at 66 MHz
  - — SMM RAM size from 32 Kbyte to 128 Kbyte. Easy SMI code copying to SMM RAM in normal memory mode
- Full PCI, DRAM, and CPU concurrency
  - — Concurrent CPU-to-L2 and PCI-to-DRAM operation
  - — Concurrent CPU-to-DRAM and PCI Master-to-PCI Target peer transfer
- PCI Local Bus interface
  - — Supports sustained PCI bursting up to 120 Mbytes per second
    - − CPU-to-PCI burst write
    - − PCI-to-DRAM write/read burst
  - — Twenty-four D-word PCI-to-DRAM write buffer
  - — Sixteen D-word pre-fetch read buffer
  - — Five PCI REQ#/GNT# pairs for PCI Master support
  - — Supports PCI Bus speeds up to 33 MHz
  - — Supports 3.3V I/O, 5V-tolerant 32-bit PCI local bus
  - — Synchronous interface between the CPU and PCI Bus
  - — Complies with PCI Local Bus revision 2.1
  - — Integrated PCI Bus arbiter with configurable priority schemes
  - — PCI parity and system error support
  - — PC87560 PCI System I/O controller provides a complete solution
- Power and thermal management
  - — Complies with ACPI and Windows 95 APM 1.2
  - — Active and passive power management cuts power consumption when the system is in use or in an idle state
  - — Supports both legacy and ACPI power management implementations
  - — Supports System Management Mode (SMM), System Management Interrupt (SMI), Stop Clock, and AutoHalt
  - — 3.3V voltage implementation
  - — Thermal control with thermal clock throttling (optional)
  - — User-programmable power setting
  - — Supports wakeup control, interrupt-as-wakeup-source, and ring-input-as-wakeup source
  - — Power management registers are fully compatible with the VESUVIUS-LS system controllers
  - — External activity detection and status indicator
  - — Supports 3.3V and 2.5V processor bus, 3.3V (5V-tolerant) PCI bus, 3.3V L2 cache controller, and 3.3V (5V-tolerant) DRAM subsystem
- Advanced docking support
  - — Hot-, warm-, or cold- PCI docking support
  - — Proprietary SmartDock and SmartDock-II hot-docking arbitration interface
  - — Supports DDMA and serialized IRQ (SERIRQ) open specifications for dual-ISA bus support and lowers the docking connector pin count
- Technology
  - — Supports JTAG boundary scan
  - — Space-efficient 388-pin BGA package
  - — 0.5 µm CMOS technology

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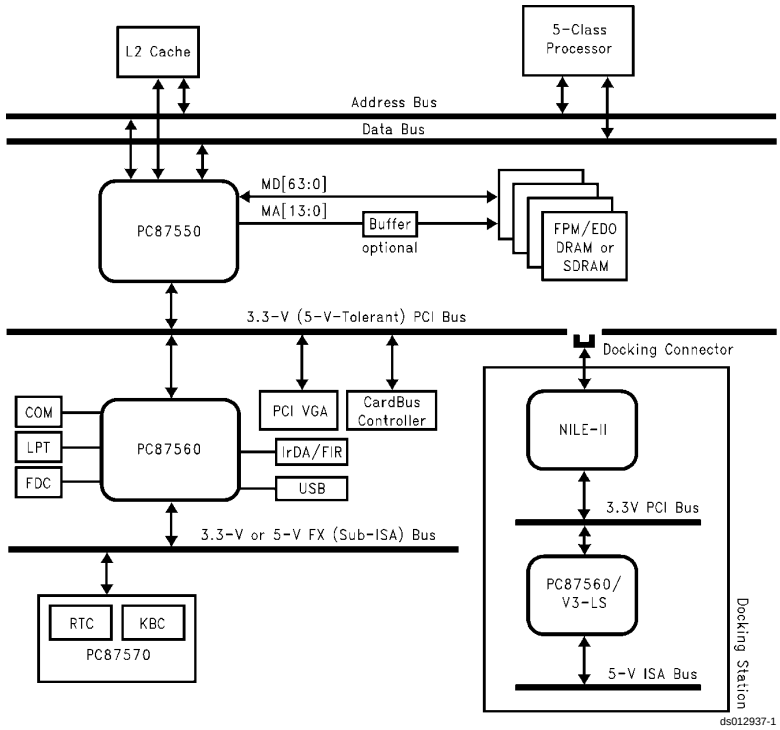
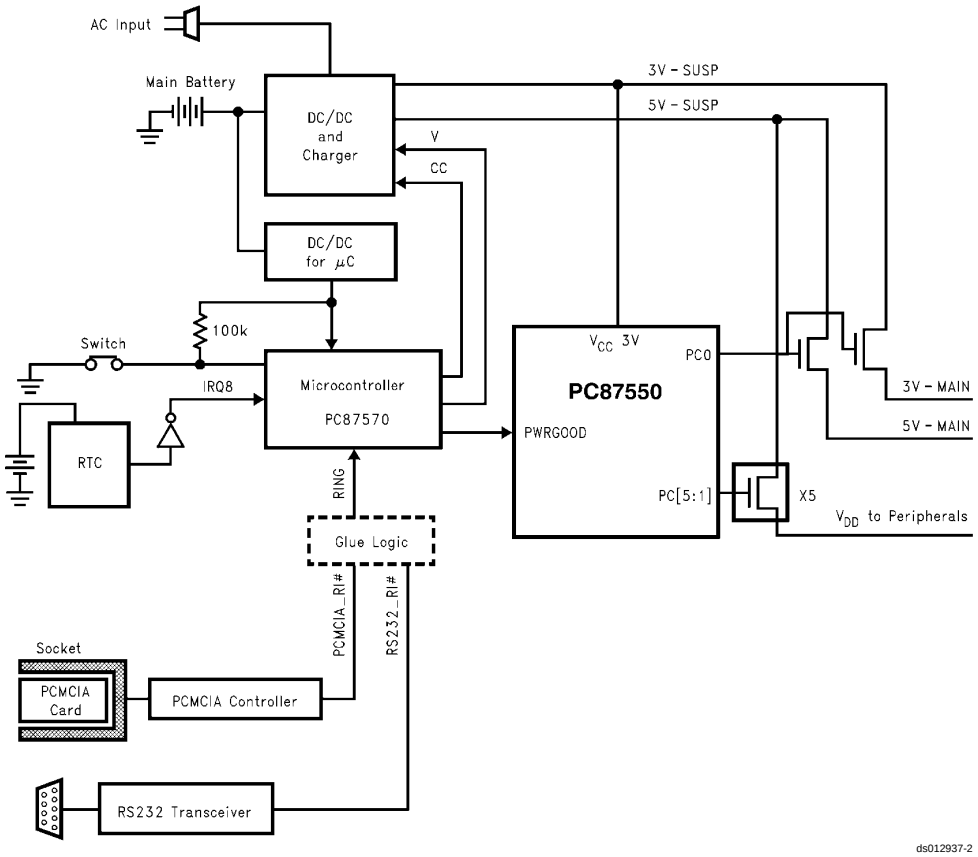
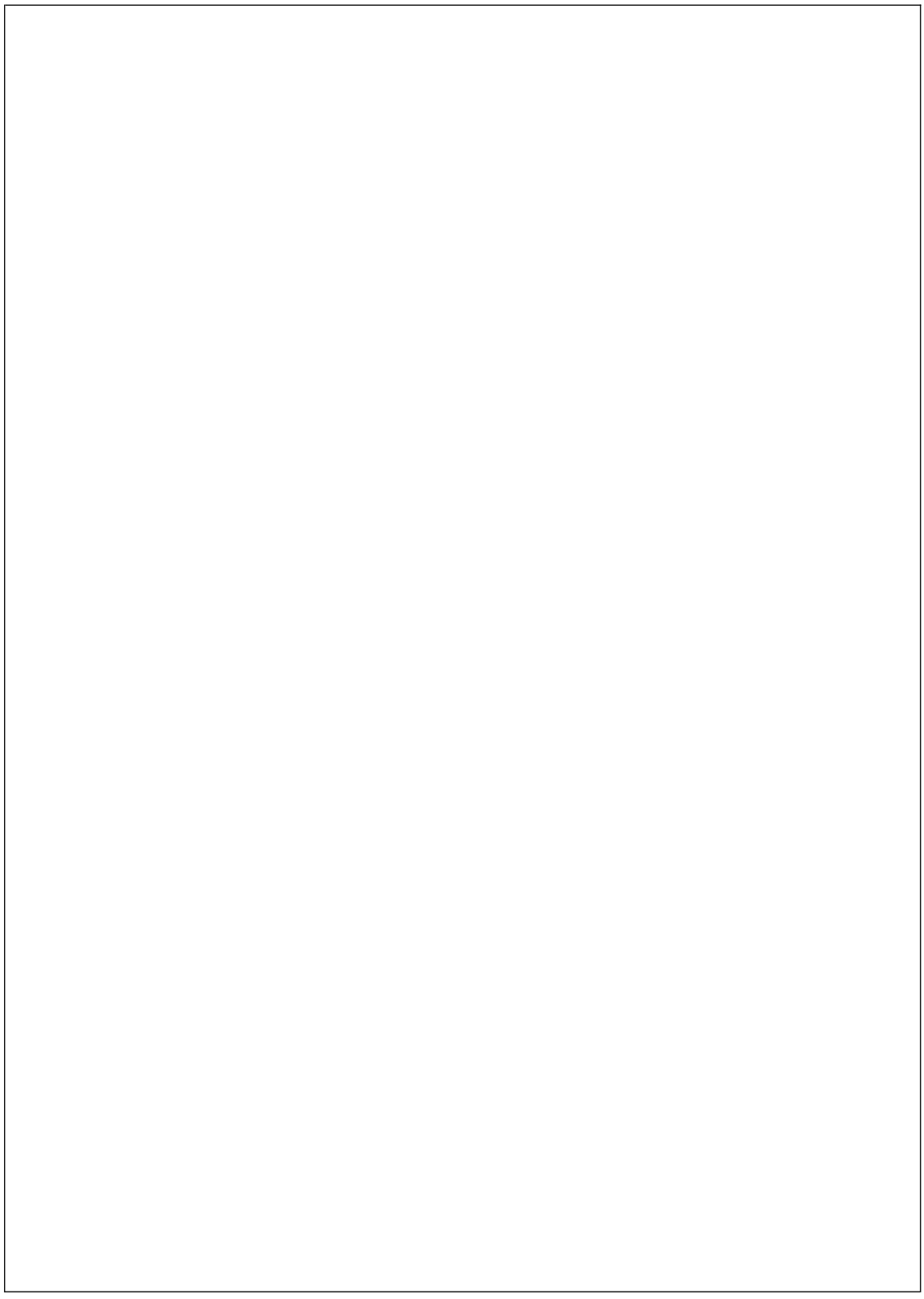
AMAZON System Block Diagram



Typical Portable Computer Design with Zero-Volt Suspend Implementation



LEGEND
V = VCC SUSP_ON/OFF
CC = Charger Control



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Physical Dimensions inches (millimeters)

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