RM42L432 16/32-Bit RISC Flash Microcontroller

Check for Samples: RM42L432

1 RM42L432 16/32-Bit RISC Flash Microcontroller

1.1 Features

- High-Performance Microcontroller for Safety Critical Applications
  - Dual CPU's Running in Lockstep
  - ECC on Flash and RAM interfaces
  - Built-In Self Test for CPU and On-chip RAMs
  - Error Signaling Module with Error Pin
  - Voltage and Clock Monitoring
- ARM® Cortex™ – R4 32-bit RISC CPU
  - Efficient 1.66DMIPS/MHz with 8-stage Pipeline
  - 8-Region Memory Protection Unit
  - Open Architecture with 3rd Party Support
- Operating Conditions
  - 100MHz System Clock
  - Core Supply Voltage (V_{CC}): 1.2V nominal
  - I/O Supply Voltage (V_{CCIO}): 3.3V nominal
  - ADC Supply Voltage (V_{CCAD}): 3.3V Nominal
- Integrated Memory
  - 384kB Program Flash with ECC
  - 32kB RAM with ECC
  - 16kB Flash for Emulated EEPROM with ECC
- Common Platform Architecture
  - Consistent Memory Map Across Family
  - Real-Time Interrupt Timer (RTI) OS Timer
  - 96-channel Vectored Interrupt Module (VIM)
  - 2-channel Cyclic Redundancy Checker (CRC)
- Frequency-Modulated Phase-Locked-Loop (FMPLL) with Built-In Slip Detector
- IEEE 1149.1 JTAG, Boundary Scan and ARM CoreSight Components
- Advanced JTAG Security Module (AJSM)
- Multiple Communication Interfaces
  - Two CAN Controllers (DCAN)
    - DCAN1 - 32 Mailboxes with Parity Protection
    - DCAN2 - 16 Mailboxes with Parity Protection
    - Compliant to CAN protocol Version 2.0B
  - Multi-buffered Serial Peripheral Interface (MibSPI)
    - 128 Words with Parity Protection
  - Two Standard Serial Peripheral Interfaces (SPI)
  - UART (SCI) interface with Local Network Interface (LIN 2.1) support
- High-End Timer Module (N2HET)
  - Up to 19 Programmable Pins
  - 128 Word Instruction RAM with Parity Protection
  - Each Includes Hardware Angle Generator
  - Dedicated Transfer Unit (HTU)
- Enhanced Quadrature Encoder Pulse (eQEP)
  - Motor Position Encoder Interface
- 12-bit Multi-Buffered ADC Module
  - 16channels
  - 64 Result Buffers with Parity Protection
- Up to 45 general purpose I/O (GIO) capable pins
  - 8 Dedicated General-Purpose I/O (GIO) Pins with up to 8 External Interrupts
- Packages
  - 100-pin Quad Flatpack (PZ) [Green]

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1.2 Applications

- **Industrial Safety Applications**
  - **Industrial Automation**
  - **Safe PLC's (Programmable Logic Controllers)**
  - **Power Generation and Distribution**
  - **Turbines and Windmills**
  - **Elevators and Escalators**
- **Medical Applications**
  - **Ventilators**
  - **Defibrillators**
  - **Infusion and Insulin pumps**
  - **Radiation therapy**
  - **Robotic surgery**

1.3 Description

The RM42L432 is a high performance microcontroller for safety systems. The safety architecture includes Dual CPUs in lockstep, CPU and Memory Built-In Self Test (BIST) logic, ECC on both the Flash and the data SRAM, parity on peripheral memories, and loop back capability on peripheral IOs.

The RM42L432 integrates the ARM® Cortex™-R4 CPU which offers an efficient 1.66DMIPS/MHz, and can run up to 100MHz providing up to 166 DMIPS. The device supports little-endian [LE32] format.

The RM42L432 has 384kB integrated Flash and 32kB data RAM configurations with single bit error correction and double bit error detection. The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 64-bit-wide data bus interface. The flash operates on a 3.3V supply input (same level as I/O supply) for all read, program and erase operations. The flash operates with a system clock frequency of up to 100 MHz in pipeline mode. The SRAM supports single-cycle read/write accesses in byte, halfword, and word modes.

The RM42L432 device features peripherals for real-time control-based applications, including a Next Generation High End Timer (N2HET) timing coprocessor with up to 19 total IO terminals and a 12-bit Analog-to-Digital converter supporting 16 inputs in the 100 pin package.

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. A High End Timer Transfer Unit (HET-TU) can perform DMA type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HET-TU.

The enhanced quadrature encoder pulse (eQEP) module is used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine as used in high-performance motion and position-control systems.

The device has a 12-bit-resolution MibADC with 16 total channels and 64 words of parity protected buffer RAM. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. There are three separate groupings. Each sequence can be converted once when triggered or configured for continuous conversion mode.

The device has multiple communication interfaces: one MibSPI, two SPIs, one UART/LIN, and two DCANs. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The UART/LIN supports the Local Interconnect standard 2.1 and can be used as a UART in full-duplex mode using the standard Non-Return-to-Zero (NRZ) format. The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The DCAN is ideal for applications operating in noisy and harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

The frequency-modulated phase-locked loop (FMPLL) clock module is used to multiply the external frequency reference to a higher frequency for internal use. The FMPLL provides one of the five possible clock source inputs to the global clock module (GCM). The GCM module manages the mapping between the available clock sources and the device clock domains.

The device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock on the ECLK pin. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (VCLK) frequency. This low frequency output can be monitored externally as an indicator of the device operating frequency.

The Error Signaling Module (ESM) monitors all device errors and determines whether an interrupt or external Error pin is triggered when a fault is detected. The nERROR can be monitored externally as an indicator of a fault condition in the microcontroller.

With integrated safety features and a wide choice of communication and control peripherals, the RM42L432 is an ideal solution for real time control applications with safety critical requirements.

1.4 Functional Block Diagram

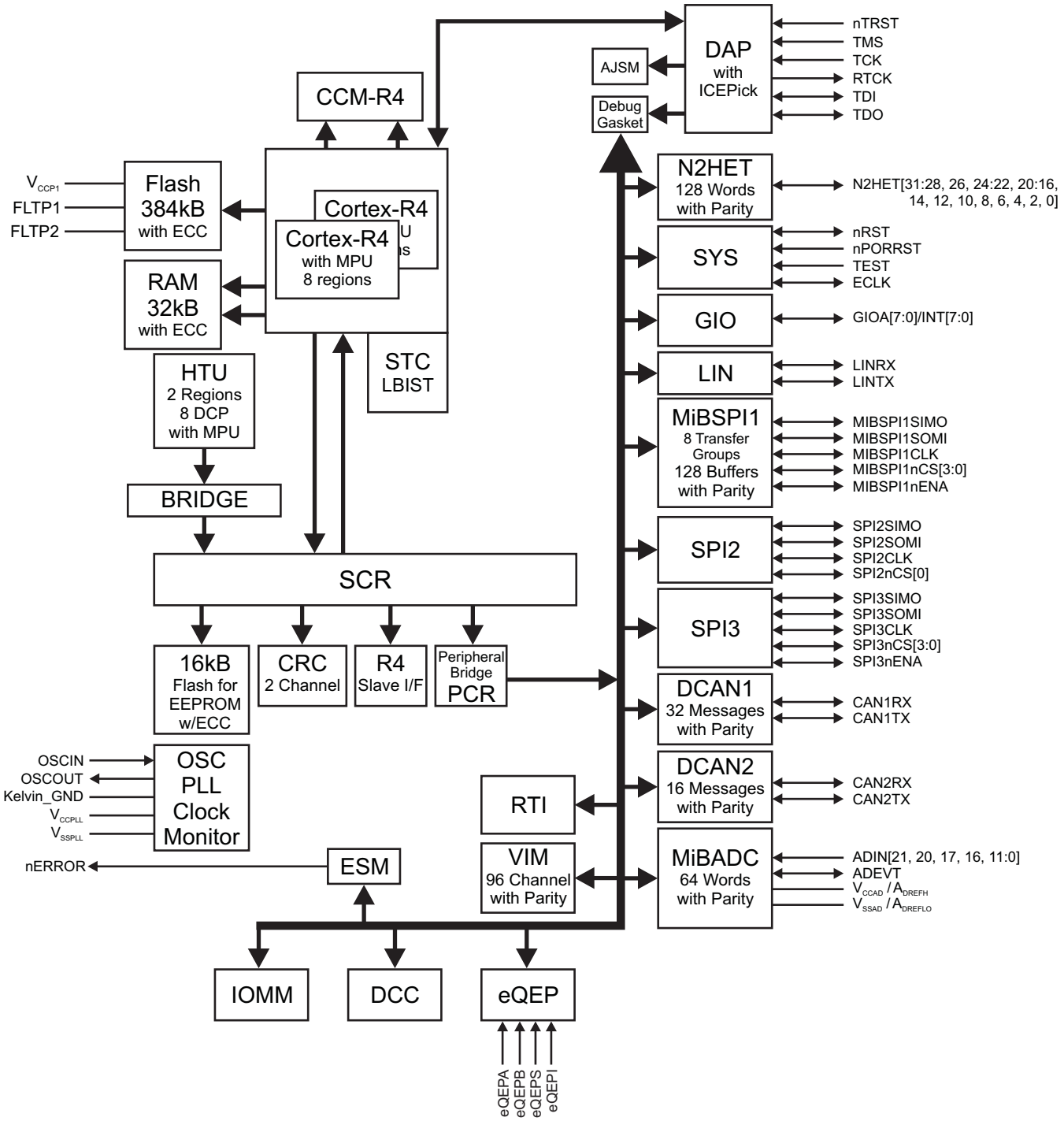

Figure 1-1. Functional Block Diagram

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2 Device Package and Terminal Functions

2.1 PZ QFP Package Pinout (100-Pin)

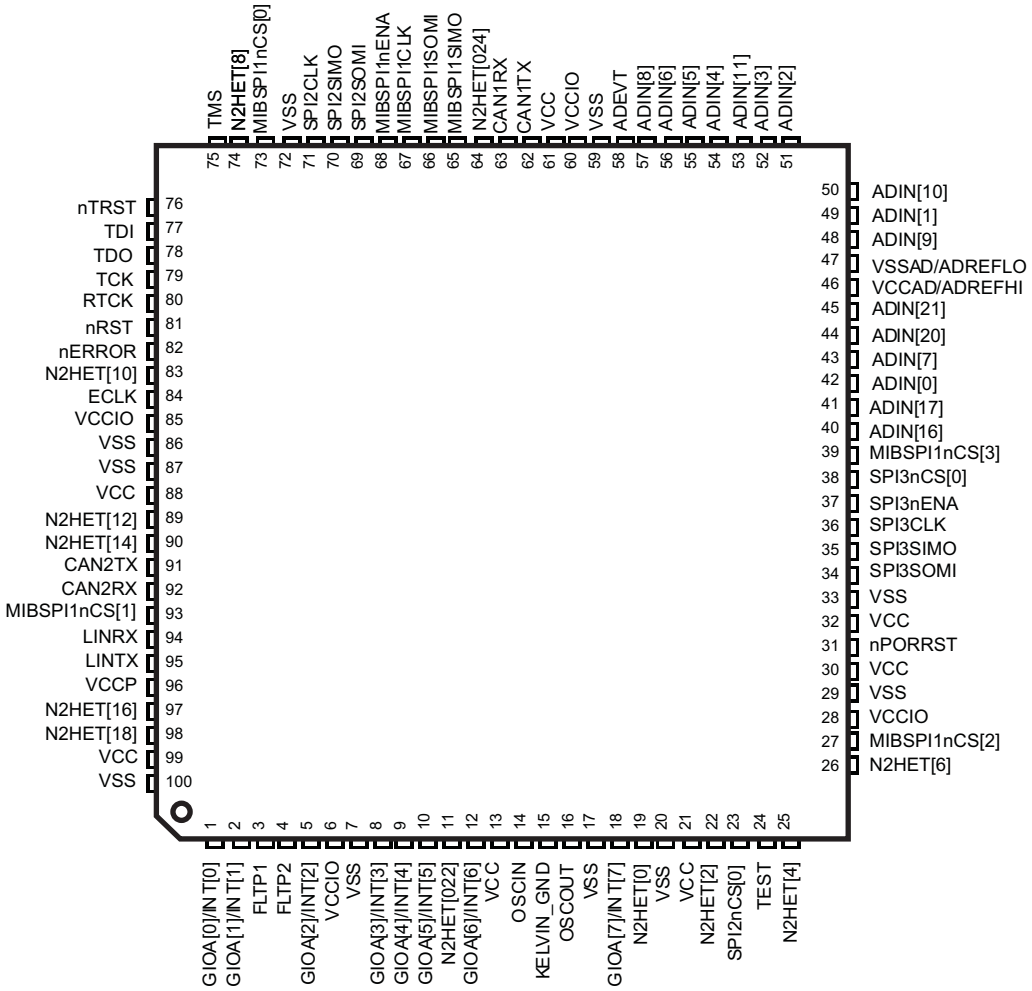

Figure 2-1. PZ QFP Package Pinout (100-Pin)

Note: Pins can have multiplexed functions. Only the default function is depicted in above diagram.

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2.2 Terminal Functions

The following table identifies the external signal names, the associated pin numbers along with the mechanical package designator, the pin type (Input, Output, IO, Power or Ground), whether the pin has any internal pullup/pulldown, whether the pin can be configured as a GIO, and a functional pin description.

NOTE

All I/O signals except nRST are configured as inputs while nPORRST is low and immediately after nPORRST goes High.

All output-only signals are configured as inputs while nPORRST is low, and are configured as outputs immediately after nPORRST goes High.

While nPORRST is low, the input buffers are disabled, and the output buffers are tri-stated.

2.2.1 High-End Timer (N2HET)

Table 2-1. High-End Timer (N2HET)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
High-End Timer (N2HET)					
N2HET[0]	19	I/O	Pull Down	Programmable, 20uA	Timer input capture or output compare. The N2HET applicable terminals can be programmed as general-purpose input/output (GIO). All N2HET terminals are high-resolution. The high-resolution (HR) SHARE feature allows even HR terminals to share the next higher odd HR structures. The next higher odd HR structure is always implemented, even the next higher odd HR pterminal itself is not. The HR sharing is independent of whether or not the odd terminal is available externally. If an odd terminal is available externally and shared, then the odd terminal can only be used as a general-purpose I/O. N2HET[0] provides SPI clock when used for SPI emulation. Each N2HET terminal is equipped with a suppression filter. If the terminal is configured as an input it enables to filter out pulses which are smaller than a programmable duration.
N2HET[2]	22				
N2HET[4]	25				
N2HET[6]	26				
N2HET[8]	74				
N2HET[10]	83				
N2HET[12]	89				
N2HET[14]	90				
N2HET[16]	97				
MIBSPI1nCS[1]/EQEPS/ **N2HET[17]**	93				
N2HET[18]	98				
MIBSPI1nCS[2]/N2HET[20]/ **N2HET[19]**	27				
MIBSPI1nCS[2]/**N2HET[20]**/ N2HET[19]	27				
N2HET[22]	11				
N2HET[24]	64				
MIBSPI1nCS[3]/**N2HET[26]**	39				
ADEVT/**N2HET[28]**	58				
GIOA[7]/**N2HET[29]**	18				
MIBSPI1nENA/NHET[23]/ **N2HET[30]**	68				
GIOA[6]/SPI2nCS[1]/**N2HET[31]**	12				

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2.2.2 Enhanced Quadrature Encoder Pulse Modules (eQEP)

Table 2-2. PGE Enhanced Quadrature Encoder Pulse Modules (eQEP)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
SPI3CLK/**EQEPA**	36	Input	Pullup	Fixed, 20uA	Enhanced QEP Input A
SPI3nENA/**EQEPB**	37	Input			Enhanced QEP Input B
SPI3nCS[0]/**EQEPI**	38	I/O			Enhanced QEP Index
MIBSPI1nCS[1]/**EQEPS**/NHET[17]	93	I/O			Enhanced QEP Strobe

2.2.3 General-Purpose Input/Output (GIO)

Table 2-3. General-Purpose Input/Output (GIO)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
GIOA[0]/SPI3nCS[3]	1	I/O	Pull Down	Programmable, 20uA	General-purpose input/output GIOA[7:0]/INT[7:0] are interrupt-capable terminals.
GIOA[1]/SPI3nCS[2]	2				
GIOA[2]/SPI3nCS[1]	5				
GIOA[3]/SPI2nCS[3]	8				
GIOA[4]/SPI2nCS[2]	9				
GIOA[5]/EXTCLKIN	10				
GIOA[6]/SPI2nCS[1]/N2HET[31]	12				
GIOA[7]/N2HET[29]	18				

2.2.4 Controller Area Network Interface Modules (DCAN1, DCAN2)

Table 2-4. Controller Area Network Interface Modules (DCAN1, DCAN2)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
CAN1RX	63	I/O	Pull Up	Programmable, 20uA	CAN1 Receive, or general-purpose I/O (GPIO)
CAN1TX	62				CAN1 Transmit, or GPIO
CAN2RX	92				CAN2 Receive, or GPIO
CAN2TX	91				CAN2 Transmit, or GPIO

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2.2.5 Multi-Buffered Serial Peripheral Interface (MibSPI1)

Table 2-5. Multi-Buffered Serial Peripheral Interface (MibSPI1)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	**100 PZ**				
MIBSPI1CLK	67	I/O	Pull Up	Programmable, 20uA	MibSPI1 Serial Clock, or GPIO
MIBSPI1nCS[0]	73				MibSPI1 Chip Select, or GPIO
MIBSPI1nCS[1]/EQEPS/N2HET[17]	93				
MIBSPI1nCS[2]/N2HET[20]/N2HET[19]	27				
MIBSPI1nCS[3]/N2HET[26]	39				
MIBSPI1nENA/N2HET[23]/N2HET[30]	68				MibSPI1 Enable, or GPIO
MIBSPI1SIMO	65				MibSPI1 Slave-In-Master-Out, or GPIO
MIBSPI1SOMI	66				MibSPI1 Slave-Out-Master-In, or GPIO

2.2.6 Standard Serial Peripheral Interface (SPI2)

Table 2-6. Standard Serial Peripheral Interface (SPI2)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	**100 PZ**				
SPI2CLK	71	I/O	Pull Up	Programmable, 20uA	SPI2 Serial Clock, or GPIO
SPI2nCS[0]	23				SPI2 Chip Select, or GPIO
GIOA[6]/**SPI2nCS[1]**/NHET[31]	12				
GIOA[4]/**SPI2nCS[2]**	9				
GIOA[3]/**SPI2nCS[3]**	8				
SPI2SIMO	70				SPI2 Slave-In-Master-Out, or GPIO
SPI2SOMI	69				SPI2 Slave-Out-Master-In, or GPIO
The drive strengths for the SPI2CLK, SPI2SIMO and SPI2SOMI signals are selected individually by configuring the respective SRS bits of the SPIPC9 register fo SPI2. SRS = 0 for 8mA drive (fast). This is the default mode as the SRS bits in the SPIPC9 register default to 0. SRS = 1 for 2mA drive (slow)					
SPI3CLK/EQEPA	36	I/O	Pull Up	Programmable, 20uA	SPI3 Serial Clock, or GPIO
SPI3nCS[0]/EQEPI	38				SPI3 Chip Select, or GPIO
GIOA[2]/**SPI3nCS[1]**	5				
GIOA[1]/**SPI3nCS[2]**	2				
GIOA[0]/**SPI3nCS[3]**	1				
SPI3nENA/EQEPB	37				SPI3 Enable, or GPIO
SPI3SIMO	35				SPI3 Slave-In-Master-Out, or GPIO
SPI3SOMI	34				SPI3 Slave-Out-Master-In, or GPIO

2.2.7 Local Interconnect Network Controller (LIN)

Table 2-7. Local Interconnect Network Controller (LIN)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
LINRX	94	I/O	Pull Up	Programmable, 20uA	LIN Receive, or GPIO
LINTX	95				LIN Transmit, or GPIO

2.2.8 Multi-Buffered Analog-to-Digital Converter (MibADC)

Table 2-8. Multi-Buffered Analog-to-Digital Converter (MibADC)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
ADEVT/N2HET[28]	58	I/O	Pull Up	Programmable, 20uA	ADC Event Trigger or GPIO
ADIN[0]	42	Input	-	-	Analog Inputs
ADIN[1]	49				
ADIN[2]	51				
ADIN[3]	52				
ADIN[4]	54				
ADIN[5]	55				
ADIN[6]	56				
ADIN[7]	43				
ADIN[8]	57				
ADIN[9]	48				
ADIN[10]	50				
ADIN[11]	53				
ADIN[16]	40				
ADIN[17]	41				
ADIN[20]	44				
ADIN[21]	45				
ADREFHI/VCCAD	46	Input/Power	-	-	ADC High Reference Level/ADC Operating Supply
ADREFLO/VSSAD	47	Input/Ground	-	-	ADC Low Reference Level/ADC Supply Ground

2.2.9 System Module

Table 2-9. System Module

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
ECLK	84	I/O	Pull Down	Programmable, 20uA	External Prescaled Clock
GIOA[5]/**EXTCLKIN**	10	Input	Pull Down	20uA	External Clock In
nPORRST	31	Input	Pull Down	100uA	Input master chip power-up reset. External power supply monitor circuitry must assert a power-on reset. This terminal has a glitch filter.

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Table 2-9. System Module (continued)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
nRST	81	I/O	Pull Up	100uA	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On this terminal, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal. This terminal has a glitch filter.

2.2.10 Error Signaling Module (ESM)

Table 2-10. Error Signaling Module (ESM)

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
nERROR	82	I/O	Pull Down	20uA	Dedicated Error Signal

2.2.11 Main Oscillator

Table 2-11. Main Oscillator

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
OSCIN	14	Input	-	-	Oscillator Input
OSCOUT	16	Output	-	-	Oscillator Output
KELVIN_GND	15	Input	-	-	Dedicated ground for oscillator

2.2.12 Test/Debug Interface

Table 2-12. Test/Debug Interface

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
nTRST	76	Input	Pull Down	Fixed, 100uA	Test hardware reset to TAP. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic
RTCK	80	Output	-	-	Return Test clock. (JTAG)
TCK	79	Input	Pull Down	Fixed, 100uA	Test clock. TCK controls the test hardware (JTAG)
TDI	77	I/O	Pull Up	Fixed, 100uA	Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG).
TDO	78	I/O	Pull Down	Fixed, 100uA	Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG).
TMS	75	I/O	Pull Up	Fixed, 100uA	Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG)
TEST	24	I/O	Pull Down	Fixed, 100uA	Test enable. Reserved for internal use only. This terminal has a glitch filter. For proper operation, this terminal must be connected to ground, e.g. using a external resistor.

2.2.13 Flash

Table 2-13. Flash

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
FLTP1	3	Input	-	-	Flash Test Pad 1. For proper operation this terminal must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event.
FLTP2	4	Input	-	-	Flash Test Pad 2. For proper operation this terminal must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event.
VCCP	96	Input	-	-	Flash external pump voltage (3.3 V). This terminal is required for both Flash read and Flash program and erase operations.

2.2.14 Core Supply

Table 2-14. Core Supply

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
VCC	13	-	-	-	Digital logic and RAM supply
VCC	21				
VCC	30				
VCC	32				
VCC	61				
VCC	88				
VCC	99				

2.2.15 I/O Supply

Table 2-15. I/O Supply

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
VCCIO	6	-	-	-	I/O Supply
VCCIO	28				
VCCIO	60				
VCCIO	85				

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2.2.16 Core and I/O Supply Ground Reference

Table 2-16. Core and I/O Supply Ground Reference

Terminal		Signal Type	Default Pull State	Pull Type	Description
Signal Name	100 PZ				
VSS	7	-	-	-	Device Ground Reference. This is a single ground reference for all supplies except for the ADC Supply.
VSS	17				
VSS	20				
VSS	29				
VSS	33				
VSS	59				
VSS	72				
VSS	86				
VSS	87				
VSS	100				

2.3 Output Multiplexing and Control

Output multiplexing will be utilized in the device. The multiplexing is utilized to allow development of additional package/feature combinations as well as to maintain pinout compatibility with the marketing device family.

In all cases indicated as multiplexed, the output buffers are multiplexed.

Table 2-17. Output Mux Options

100PZ Pin	Default Function	Control 1	Option2	Control 2	Option 3	Control 3
1	GIOA[0]	PINMMR0[8]	SPI3nCS[3]	PINMMR0[9]	-	-
2	GIOA[1]	PINMMR1[0]	SPI3nCS[2]	PINMMR1[1]	-	-
5	GIOA[2]	PINMMR1[8]	SPI3nCS[1]	PINMMR1[9]	-	-
8	GIOA[3]	PINMMR1[16]	SPI2nCS[3]	PINMMR1[17]	-	-
9	GIOA[4]	PINMMR1[24]	SPI2nCS[2]	PINMMR1[25]	-	-
10	GIOA[5]	PINMMR2[0]	EXTCLKIN	PINMMR2[1]	-	-
12	GIOA[6]	PINMMR2[8]	SPI2nCS[1]	PINMMR2[9]	N2HET[31]	PINMMR2[10]
18	GIOA[7]	PINMMR2[16]	N2HET[29]	PINMMR2[17]	-	-
93	MIBSPI1nCS[1]	PINMMR6[8]	EQEPS	PINMMR6[9]	N2HET[17]	PINMMR6[10]
27	MIBSPI1nCS[2]	PINMMR3[0]	N2HET[20]	PINMMR3[1]	N2HET[19]	PINMMR3[2]
39	MIBSPI1nCS[3]	PINMMR4[8]	N2HET[26]	PINMMR4[9]	-	-
68	MIBSPI1nENA	PINMMR5[8]	N2HET[23]	PINMMR5[9]	N2HET[30]	PINMMR5[10]
36	SPI3CLK	PINMMR3[16]	EQEPA	PINMMR3[17]	-	-
38	SPI3nCS[0]	PINMMR4[0]	EQEPI	PINMMR4[1]	-	-
37	SPI3nENA	PINMMR3[24]	EQEPB	PINMMR3[25]	-	-
58	ADEVT	PINMMR4[16]	N2HET[28]	PINMMR4[17]	-	-

2.3.1 Notes on Output Multiplexing

Table 2-17 shows the output signal multiplexing and control signals for selecting the desired functionality for each pin.

- The pins default to the signal defined by the "Default Function" column in Table 2-17
- The "CTRL x" columns indicate the multiplexing control register and the bit that must be set in order to select the corresponding functionality to be output on any particular pin.

  For example, consider the multiplexing on pin 18, shown below.

Table 2-18. Muxing Example

100PZ Pin	Default Function	Control 1	Option2	Control 2	Option 3	Control 3
18	GIOA[7]	PINMMR2[16]	N2HET[29]	PINMMR2[17]	-	-

- When GIOA[7] is configured as an output pin in the GIO module control register, then the programmed output level appears on pin 18 by default. The PINMMR2[16] bit is set by default to indicate that the GIOA[7] signal is selected to be output.
- If the application needs to output the N2HET[29] signal on pin 18, it must clear PINMMR2[16] and set PINMMR2[17].
- Note that the pin is connected as input to both the GIO and N2HET modules. That is, there is no input multiplexing on this pin.

2.3.2 General Rules for Multiplexing Control Registers

- The PINMMR control registers can only be written in privileged mode. A write in a non–privileged mode will generate an error response.
- If the application writes all 0's to any PINMMR control register, then the default functions are selected for the affected pins.

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- Each byte in a PINMMR control register is used to select the functionality for a given pin. If the application sets more than one bit within a byte for any pin, then the default function is selected for this pin.
- Some bits within the PINMMR registers could be associated with internal pads that are not brought out in the 100 pin package. As a result, bits marked reserved should not be written as a 1.

2.4 Special Multiplexed Options

Special controls are implemented to affect particular functions on this microcontroller. These controls are described in this section.

2.4.1 Filtering for eQEP Inputs

2.4.1.1 eQEPA Input

- When PINMMR8[0] = 1, the eQEPA input is double-synchronized using VCLK.
- When PINMMR8[0] = 0 and PINMMR8[1] = 1, the eQEPA input is double-synchronized and then qualified through a fixed 6-bit counter using VCLK.
- PINMMR8[0] = 0 and PINMMR8[1] = 0 is an illegal combination and behavior defaults to PINMMR8[0] = 1.

2.4.1.2 eQEPB Input

- When PINMMR8[8] = 1, the eQEPB input is double-synchronized using VCLK.
- When PINMMR8[8] = 0 and PINMMR8[9] = 1, the eQEPB input is double-synchronized and then qualified through a fixed 6-bit counter using VCLK.
- PINMMR8[8] = 0 and PINMMR8[9] = 0 is an illegal combination and behavior defaults to PINMMR8[8] = 1.

2.4.1.3 eQEPI Input

- When PINMMR8[16] = 1, the eQEPI input is double-synchronized using VCLK.
- When PINMMR8[16] = 0 and PINMMR8[17] = 1, the eQEPI input is double-synchronized and then qualified through a fixed 6-bit counter using VCLK.
- PINMMR8[16] = 0 and PINMMR8[17] = 0 is an illegal combination and behavior defaults to PINMMR8[16] = 1.

2.4.1.4 eQEPS Input

- When PINMMR8[24] = 1, the eQEPS input is double-synchronized using VCLK.
- When PINMMR8[24] = 0 and PINMMR8[25] = 1, the eQEPS input is double-synchronized and then qualified through a fixed 6-bit counter using VCLK.
- PINMMR8[24] = 0 and PINMMR8[25] = 0 is an illegal combination and behavior defaults to PINMMR8[24] = 1.

2.4.2 N2HET PIN_nDISABLE Input Port

- When PINMMR9[0] = 1, GIOA[5] is connected directly to N2HET PIN_nDISABLE input of the N2HET module.
- When PINMMR9[0] = 0 and PINMMR9[1] = 1, EQEPERR is inverted and double-synchronized using VCLK before connecting directly to the N2HET PIN_nDISABLE input of the N2HET module.
- PINMMR9[0] = 0 and PINMMR9[1] = 0 is an illegal combination and behavior defaults to PINMMR9[0] = 1.

3 Device Operating Conditions

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range, (1)

Supply voltage range:	V_{CC} (2)	-0.3 V to 1.43 V
	V_{CCIO}, V_{CCP} (2)	-0.3 V to 4.1 V
	V_{CCAD}	-0.3 V to 3.6 V
Input voltage range:	All input pins	-0.3 V to 4.1 V
	ADC input pins	-0.3 V to 5 V
Input clamp current:	I_{IK} (V_I < 0 or V_I > V_{CCIO}) All pins, except ADIN	±20 mA
	I_{IK} (V_I < 0 or V_I > V_{CCAD}) ADIN	±10 mA
	Total	±40 mA
Operating free-air temperature range, T_A:		-40°C to 105°C
Operating junction temperature range, T_J:		-40°C to 150°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to their associated grounds.

3.2 Device Recommended Operating Conditions(1)

		MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)	1.14	1.2	1.32	V
V_{CCIO}	Digital logic supply voltage (I/O)	3	3.3	3.6	V
V_{CCAD} / $V_{ADREFHI}$	MibADC supply voltage / A-to-D high-voltage reference source	3	3.3	3.6	V
V_{CCP}	Flash pump supply voltage	3	3.3	3.6	V
V_{SS}	Digital logic supply ground		0		V
V_{SSAD} / $V_{ADREFLO}$	MibADC supply ground / A-to-D low-voltage reference source	-0.1		0.1	V
T_A	Operating free-air temperature	-40		105	°C
T_J	Operating junction temperature	-40		150	°C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}

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3.3 Switching Characteristics over Recommended Operating Conditions for Clock Domains

Table 3-1. Clock Domain Timing Specifications(1)

Parameter	Description	Conditions	MIN	MAX	Unit
f_{OSC}	OSC - oscillator clock frequency		5	20	MHz
f_{RCLK}	Post-ODCLK – PLL Post-divider input clock frequency			400	MHz
f_{ODCLK}	VCOCLK – PLL Output Divider (OD) input clock frequency			500	MHz
f_{HCLK}	HCLK - System clock frequency			100	MHz
f_{GCLK}	GCLK - CPU clock frequency (ratio f_{GCLK} : f_{HCLK} = 1:1)			f_{HCLK}	MHz
f_{VCLK}	VCLK - Primary peripheral clock frequency			100	MHz
f_{VCLKA1}	VCLKA1 - Primary asynchronous peripheral clock frequency			100	MHz
f_{RTICLK}	RTICLK - clock frequency			f_{VCLK}	MHz
$f_{PROG/ERASE}$	System clock frequency - Flash programming/erase			f_{HCLK}	MHz

(1) The maximum frequency that can be output on the ECLK signal is dependent on the capacitive loading on this signal. The ECLK signal has a selectable 2mA / 8mA output buffer.

3.4 Wait States Required

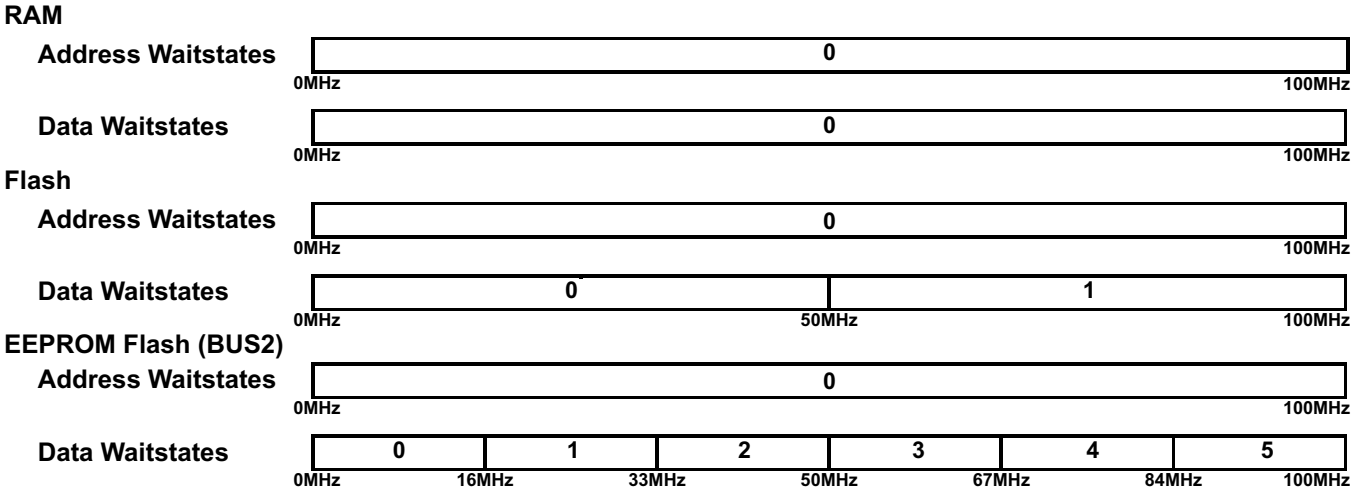

Figure 3-1. Wait States Scheme

As shown in the figure above, the TCM RAM can support program and data fetches at full CPU speed without any address or data wait states required.

The TCM flash can support zero address and data wait states up to a CPU speed of 50MHz in non-pipelined mode. The flash supports a maximum CPU clock speed of 100MHz in pipelined mode with no address wait states and one data wait state.

The flash wrapper defaults to non-pipelined mode with zero address wait state and one random-read data wait state.

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3.5 Power Consumption Over Recommended Operating Conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	V_{CC} digital supply current (operating mode)		f_{HCLK} = 100MHz f_{VCLK} = 100MHz, Flash in pipelined mode, V_{CCmax}			150	mA
	V_{CC} Digital supply current (LBIST mode)		LBIST clock rate = 50MHz			165	mA
	VCC Digital supply current (PBIST mode)	Peak	PBIST ROM clock frequency = 100MHz			150	mA
		RMS					
I_{CCIO}	V_{CCIO} Digital supply current (operating mode.		No DC load, V_{CCmax}			15	mA
I_{CCAD}	V_{CCAD} supply current (operating mode)		$V_{CCADmax}$			15	mA
$I_{CCREFHI}$	AD_{REFHI} supply current (operating mode)		$AD_{REFHImax}$			5	mA
I_{CCP}	V_{CCP} pump supply current		read operation V_{CCPmax}			34	mA
			program, V_{CCPmax}			37	
			read from one bank and program another, V_{CCPmax}			55	
			erase, V_{CCPmax}			27	

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3.6 Input/Output Electrical Characteristics Over Recommended Operating Conditions(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis	All inputs		180			mV
V_{IL}	Low-level input voltage	All inputs(2)		-0.3		0.8	V
V_{IH}	High-level input voltage	All inputs(2)		2		V_{CCIO} + 0.3	V
V_{OL}	Low-level output voltage		I_{OL} = I_{OLmax}			0.2 V_{CCIO}	V
			I_{OL} = 50 µA, standard output mode			0.2	
V_{OH}	High-level output voltage		I_{OH} = I_{OHmax}	0.8 V_{CCIO}			V
			I_{OH} = 50 µA, standard output mode	V_{CCIO} -0.2			
I_{IC}	Input clamp current (I/O pins)		V_I < V_{SSIO} - 0.3 or V_I > V_{CCIO} + 0.3	-2		2	mA
I_I	Input current (I/O pins)	I_{IH} Pulldown 20µA	V_I = V_{CCIO}	5		40	µA
		I_{IH} Pulldown 100µA	V_I = V_{CCIO}	40		195	
		I_{IL} Pullup 20µA	V_I = V_{SS}	-40		-5	
		I_{IL} Pullup 100µA	V_I = V_{SS}	-195		-40	
		All other pins	No pullup or pulldown	-1		1	
C_I	Input capacitance					2	pF
C_O	Output capacitance					3	pF

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) This does not apply to the nPORRST pin.

3.7 Output Buffer Drive Strengths

Table 3-2. Output Buffer Drive Strengths

Low-level Output Current, I_{OL} for V_I=V_{OLmax} or High-level Output Current, I_{OH} for V_I=V_{OHmin}	Signals
8mA	EQEPI, EQEPS, TMS, TDI, TDO, RTCK, nERROR
4mA	TEST, MIBSPI1SIMO, MIBSPI1SOMI, MIBSPI1CLK, SPI3CLK, SPI3SIMO, SPI3SOMI, nRST
2mA zero-dominant	AD1EVT, CAN1RX, CAN1TX, CAN2RX, CAN2TX, GIOA[0-7], LINRX, LINTX, MIBSPI1NCS[0-3], MIBSPI1NENA N2HET[0], N2HET[2], N2HET[4], N2HET[6], N2HET[8], N2HET[10], N2HET[12], N2HET[14], N2HET[16], N2HET[18], N2HET[22], N2HET[24], SPI2NCS[0-3], SPI3NENA

Table 3-2. Output Buffer Drive Strengths (continued)

Low-level Output Current, I_{OL} for $V_I=V_{OLmax}$ or High-level Output Current, I_{OH} for $V_I=V_{OHmin}$	Signals
selectable 8mA / 2mA	ECLK, SPI2CLK, SPI2SIMO, SPI2SOMI The default output buffer drive strength is 8mA for these signals.

3.8 Input Timings

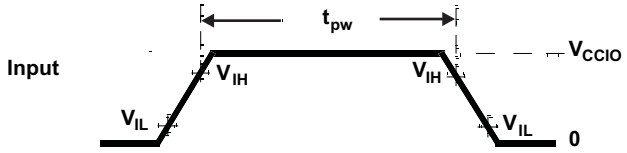

Figure 3-2. TTL-Level Inputs

Table 3-3. Timing Requirements for Inputs (1)

Parameter		MIN	MAX	Unit
t_{pw}	Input minimum pulse width	$t_{c(VCLK)}$ + 10 (2)		ns
t_{in_slew}	Time for input signal to go from V_{IL} to V_{IH} or from V_{IH} to V_{IL}		1	ns

(1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = 1 / $f_{(VCLK)}$
(2) The timing shown above is only valid for pin used in GIO mode.

3.9 Output Timings

Table 3-4. Switching Characteristics for Output Timings versus Load Capacitance (C_L)

Parameter			MIN	MAX	Unit
Rise time, t_r	8mA pins	CL = 15 pF		2.5	ns
		CL = 50 pF		4	
		CL = 100 pF		7.2	
		CL = 150 pF		12.5	
Fall time, t_f		CL = 15 pF		2.5	ns
		CL = 50 pF		4	
		CL = 100 pF		7.2	
		CL = 150 pF		12.5	
Rise time, t_r	4mA pins	CL = 15 pF		5.6	ns
		CL = 50 pF		10.4	
		CL = 100 pF		16.8	
		CL = 150 pF		23.2	
Fall time, t_f		CL = 15 pF		5.6	ns
		CL= 50 pF		10.4	
		CL = 100 pF		16.8	
		CL = 150 pF		23.2	

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Table 3-4. Switching Characteristics for Output Timings versus Load Capacitance (C_L) (continued)

Parameter				MIN	MAX	Unit
Rise time, t_r	2mA-z pins		CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Fall time, t_f			CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Rise time, t_r	Selectable 8mA / 2mA-z pins	8mA mode	CL = 15 pF		2	ns
			CL = 50 pF		4	
			CL = 100 pF		8	
			CL = 150 pF		11	
Fall time, t_f			CL = 15 pF		2	ns
			CL = 50 pF		4	
			CL = 100 pF		8	
			CL = 150 pF		11	
Rise time, t_r		2mA-z mode	CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Fall time, t_f			CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	

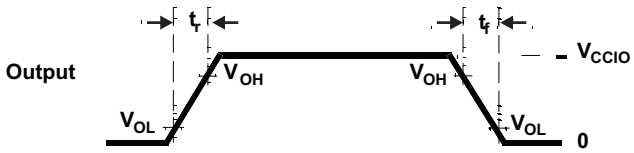

Figure 3-3. CMOS-Level Outputs

Table 3-5. Timing Requirements for Outputs (1)

Parameter		MIN	MAX	UNIT
$t_{d(parallel\_out)}$	Delay between low to high, or high to low transition of general-purpose output signals that can be configured by an application in parallel, e.g. all signals in a GIOA port, or all N2HET signals.		5	ns

(1) This specification does not account for any output buffer drive strength differences or any external capacitive loading differences. Check Table 3-2for output buffer drive strength information on each signal.

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4 System Information and Electrical Specifications

4.1 Voltage Monitor Characteristics

A voltage monitor is implemented on this device. The purpose of this voltage monitor is to eliminate the requirement for a specific sequence when powering up the core and I/O voltage supplies.

4.1.1 Important Considerations

- The voltage monitor does not eliminate the need of a voltage supervisor circuit to guarantee that the device is held in reset when the voltage supplies are out of range.
- The voltage monitor only monitors the core supply (VCC) and the I/O supply (VCCIO). The other supplies are not monitored by the VMON. For example, if the VCCAD or VCCP are supplied from a source different from that for VCCIO, then there is no internal voltage monitor for the VCCAD and VCCP supplies.

4.1.2 Voltage Monitor Operation

The voltage monitor generates the Power Good MCU signal (PGMCU) as well as the I/Os Power Good IO signal (PGIO) on the device. During power-up or power-down, the PGMCU and PGIO are driven low when the core or I/O supplies are lower than the specified minimum monitoring thresholds. The PGIO and PGMCU being low isolates the core logic as well as the I/O controls during the power-up or power-down of the supplies. This allows the core and I/O supplies to be powered up or down in any order.

When the voltage monitor detects a low voltage on the I/O supply, it will assert a power-on reset. When the voltage monitor detects an out-of-range voltage on the core supply, it asynchronously makes all output pins high impedance, and asserts a power-on reset. The voltage monitor is disabled when the device enters a low power mode.

The VMON also incorporates a glitch filter for the nPORRST input. Refer to Section 4.2.3.1 for the timing information on this glitch filter.

Table 4-1. Voltage Monitoring Specifications

PARAMETER			MIN	TYP	MAX	UNIT
V_{MON}	Voltage monitoring thresholds	VCC low - VCC level below this threshold is detected as too low.	0.8	0.9	1.0	V
		VCC high - VCC level above this threshold is detected as too high.	1.35	1.7	2.1	
		VCCIO low - VCCIO level below this threshold is detected as too low.	1.9	2.4	2.9	

4.1.3 Supply Filtering

The VMON has the capability to filter glitches on the VCC and VCCIO supplies.

The following table shows the characteristics of the supply filtering. Glitches in the supply larger than the maximum specification cannot be filtered.

Table 4-2. VMON Supply Glitch Filtering Capability

Parameter	MIN	MAX
Width of glitch on VCC that can be filtered	250ns	1us
Width of glitch on VCCIO that can be filtered	250ns	1us

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4.2 Power Sequencing and Power On Reset

4.2.1 Power-Up Sequence

There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage. The power-up sequence starts with the I/O voltage rising above the minimum I/O supply threshold, (see Table 4-4 for more details), core voltage rising above the minimum core supply threshold and the release of power-on reset. The high frequency oscillator will start up first and its amplitude will grow to an acceptable level. The oscillator start up time is dependent on the type of oscillator and is provided by the oscillator vendor. The different supplies to the device can be powered up in any order.

The device goes through the following sequential phases during power up.

Table 4-3. Power-Up Phases

Oscillator start-up and validity check	1032 oscillator cycles
eFuse autoload	1180 oscillator cycles
Flash pump power-up	688 oscillator cycles
Flash bank power-up	617 oscillator cycles
Total	**3517 oscillator cycles**

The CPU reset is released at the end of the above sequence and fetches the first instruction from address 0x00000000.

4.2.2 Power-Down Sequence

The different supplies to the device can be powered down in any order.

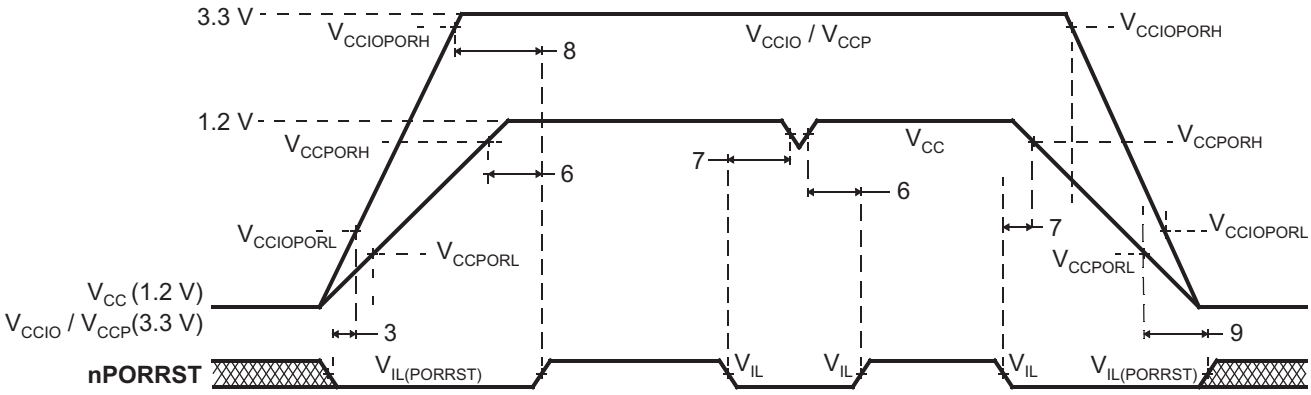
4.2.3 Power-On Reset: nPORRST

This reset must be asserted by an external circuitry whenever the I/O or core supplies are outside the recommended range. This signal has a glitch filter on it. It also has an internal pulldown.

4.2.3.1 nPORRST Electrical and Timing Requirements

Table 4-4. Electrical Requirements for nPORRST

NO	Parameter		MIN	MAX	Unit
	V_{CCPORL}	V_{CC} low supply level when nPORRST must be active during power-up		0.5	V
	V_{CCPORH}	V_{CC} high supply level when nPORRST must remain active during power-up and become active during power down	1.14		V
	$V_{CCIOPORL}$	V_{CCIO} / V_{CCP} low supply level when nPORRST must be active during power-up		1.1	V
	$V_{CCIOPORH}$	V_{CCIO} / V_{CCP} high supply level when nPORRST must remain active during power-up and become active during power down	3.0		V
	$V_{IL(PORRST)}$	Low-level input voltage of nPORRST V_{CCIO} > 2.5V		0.2 * V_{CCIO}	V
		Low-level input voltage of nPORRST V_{CCIO} < 2.5V		0.5	V
3	$t_{su(PORRST)}$	Setup time, nPORRST active before V_{CCIO} and V_{CCP} > $V_{CCIOPORL}$ during power-up	0		ms
6	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CC} > V_{CCPORH}	1		ms
7	$t_{su(PORRST)}$	Setup time, nPORRST active before V_{CC} < V_{CCPORH} during power down	2		µs
8	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CCIO} and V_{CCP} > $V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CC} < V_{CCPORL}	0		ms
	$t_{f(nPORRST)}$	Filter time nPORRST pin; Pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset.	500	2000	ns



NOTE: There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage; this is just an exemplary drawing.

Figure 4-1. nPORRST Timing Diagram

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4.3 Warm Reset (nRST)

This is a bidirectional reset signal. The internal circuitry drives the signal low on detecting any device reset condition. An external circuit can assert a device reset by forcing the signal low. On this terminal, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal.

This terminal has a glitch filter. It also has an internal pullup

4.3.1 Causes of Warm Reset

Table 4-5. Causes of Warm Reset

DEVICE EVENT	SYSTEM STATUS FLAG
Power-Up Reset	Exception Status Register, bit 15
Oscillator fail	Global Status Register, bit 0
PLL slip	Global Status Register, bits 8 and 9
Watchdog exception / Debugger reset	Exception Status Register, bit 13
CPU Reset (driven by the CPU STC)	Exception Status Register, bit 5
Software Reset	Exception Status Register, bit 4
External Reset	Exception Status Register, bit 3

4.3.2 nRST Timing Requirements

Table 4-6. nRST Timing Requirements(1)

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, nRST active after nPORRST inactive	eFuse autoload time + $1048t_{c(OSC)}$		ns
	Valid time, nRST active (all other System reset conditions)	$8t_{c(VCLK)}$		
$t_{f(nRST)}$	Filter time nRST pin; Pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	500	2000	ns

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see Table 3-4.

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4.4 ARM© Cortex-R4™ CPU Information

4.4.1 Summary of ARM Cortex-R4 CPU Features

The features of the ARM Cortex-R4™ CPU include:

- An integer unit with integral Embedded ICE-RT logic.
- High-speed Advanced Microprocessor Bus Architecture (AMBA) Advanced eXtensible Interfaces (AXI) for Level two (L2) master and slave interfaces.
- Dynamic branch prediction with a global history buffer, and a 4-entry return stack
- Low interrupt latency.
- Non-maskable interrupt.
- A Harvard Level one (L1) memory system with:
  - Tightly-Coupled Memory (TCM) interfaces with support for error correction or parity checking memories
  - ARMv7-R architecture Memory Protection Unit (MPU) with 8 regions
- Dual core logic for fault detection in safety-critical applications.
- An L2 memory interface:
  - Single 64-bit master AXI interface
  - 64-bit slave AXI interface to TCM RAM blocks
- A debug interface to a CoreSight Debug Access Port (DAP).
- A Vectored Interrupt Controller (VIC) port.

For more information on the ARM Cortex-R4 CPU please see www.arm.com.

4.4.2 ARM Cortex-R4 CPU Features Enabled by Software

The following CPU features are disabled on reset and must be enabled by the application if required.

- ECC On Tightly-Coupled Memory (TCM) Accesses
- Hardware Vectored Interrupt (VIC) Port
- Memory Protection Unit (MPU)

4.4.3 Dual Core Implementation

The device has two Cortex-R4 cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed by 2 clock cycles as shown in Figure 4-3.

The CPUs have a diverse CPU placement given by following requirements:

- different orientation; e.g. CPU1 = "north" orientation, CPU2 = "flip west" orientation
- dedicated guard ring for each CPU

Figure 4-2. Dual - CPU Orientation

4.4.4 Duplicate clock tree after GCLK

The CPU clock domain is split into two clock trees, one for each CPU, with the clock of the 2nd CPU running at the same frequency and in phase to the clock of CPU1. See Figure 4-3.

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4.4.5 ARM Cortex-R4 CPU Compare Module (CCM) for Safety

This device has two ARM Cortex-R4 CPU cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed in a different way as shown in the figure below.

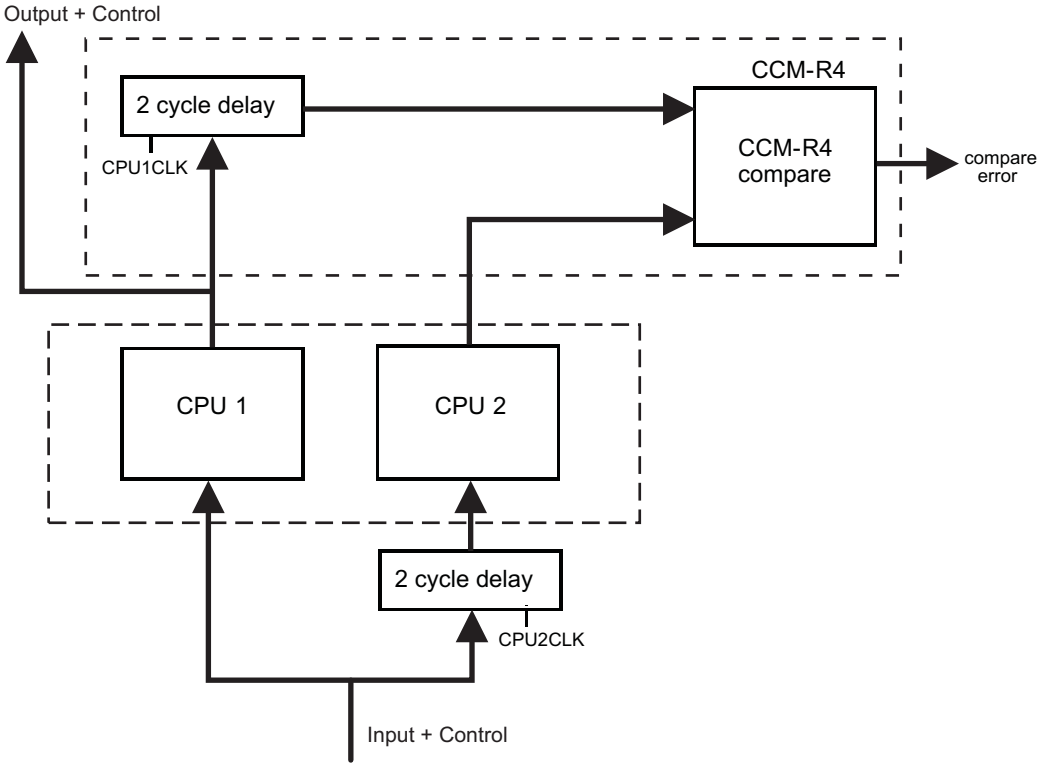

Figure 4-3. Dual Core Implementation

To avoid an erroneous CCM-R4 compare error, the application software must initialize the registers of both CPUs before the registers are used, including function calls where the register values are pushed onto the stack.

4.4.6 CPU Self-Test

The CPU STC (Self-Test Controller) is used to test the two Cortex-R4 CPU Cores using the Deterministic Logic BIST Controller as the test engine.

The main features of the self-test controller are:

- Ability to divide the complete test run into independent test intervals
- Capable of running the complete test or running a few intervals at a time
- Ability to continue from the last executed interval (test set) or to restart from the beginning (First test set)
- Complete isolation of the self-tested CPU core from the rest of the system during the self-test run
- Ability to capture the failure interval number
- Timeout counter for the CPU self-test run as a fail-safe feature

4.4.6.1 Application Sequence for CPU Self-Test

1. Configure clock domain frequencies.
2. Select the number of test intervals to be run.
3. Configure the timeout period for the self-test run.

4. Save the CPU state if required
5. Enable self-test.
6. Wait for CPU reset.
7. In the reset handler, read CPU self-test status to identify any failures.
8. Retrieve CPU state if required.

For more information refer to the device technical reference manual.

4.4.6.2 CPU Self-Test Clock Configuration

The maximum clock rate for the self-test is 50MHz. The STCCLK is divided down from the CPU clock, when necessary. This divider is configured by the STCCLKDIV register at address 0xFFFFE108.

For more information see the device Technical Reference Manual..

4.4.6.3 CPU Self-Test Coverage

Table 4-7 shows CPU test coverage achieved for each self-test interval. It also lists the cumulative test cycles. The test time can be calculated by multiplying the number of test cycles with the STC clock period.

Table 4-7. CPU Self-Test Coverage

INTERVALS	TEST COVERAGE, %	TEST CYCLES
0	0	0
1	60.06	1365
2	68.71	2730
3	73.35	4095
4	76.57	5460
5	78.7	6825
6	80.4	8190
7	81.76	9555
8	82.94	10920
9	83.84	12285
10	84.58	13650
11	85.31	15015
12	85.9	16380
13	86.59	17745
14	87.17	19110
15	87.67	20475
16	88.11	21840
17	88.53	23205
18	88.93	24570
19	89.26	25935
20	89.56	27300
21	89.86	28665
22	90.1	30030
23	90.36	31395
24	90.62	32760
25	90.86	34125
26	91.06	35490

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4.5 Clocks

4.5.1 Clock Sources

The table below lists the available clock sources on the device. Each of the clock sources can be enabled or disabled using the CSDISx registers in the system module. The clock source number in the table corresponds to the control bit in the CSDISx register for that clock source.

The table also shows the default state of each clock source.

Table 4-8. Available Clock Sources

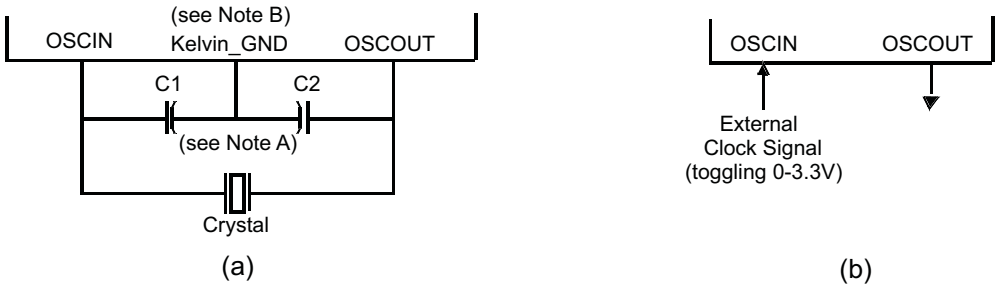
Clock Source #	Name	Description	Default State
0	OSCIN	Main Oscillator	Enabled
1	PLL1	Output From PLL1	Disabled
2	Reserved	Reserved	Disabled
3	EXTCLKIN1	External Clock Input #1	Disabled
4	CLK80K	Low Frequency Output of Internal Reference Oscillator	Enabled
5	CLK10M	High Frequency Output of Internal Reference Oscillator	Enabled
6	Reserved	Reserved	Disabled
7	Reserved	Reserved	Disabled

4.5.1.1 Main Oscillator

The oscillator is enabled by connecting the appropriate fundamental resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 4-4. The oscillator is a single stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and low power modes.

TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 3.3V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in the figure below.



Note A: The values of C1 and C2 should be provided by the resonator/crystal vendor.
Note B: Kelvin_GND should not be connected to any other GND.

Figure 4-4. Recommended Crystal/Clock Connection

4.5.1.1.1 Timing Requirements for Main Oscillator

Table 4-9. Timing Requirements for Main Oscillator

Parameter		MIN	Type	MAX	Unit
tc(OSC)	Cycle time, OSCIN (when using a sine-wave input)	50		200	ns
tc(OSC_SQR)	Cycle time, OSCIN, (when input to the OSCIN is a square wave)	12.5		200	ns
tw(OSCIL)	Pulse duration, OSCIN low (when input to the OSCIN is a square wave)	6			ns
tw(OSCIH)	Pulse duration, OSCIN high (when input to the OSCIN is a square wave)	6			ns

4.5.1.2 Low Power Oscillator

The Low Power Oscillator (LPO) is comprised of two oscillators — HF LPO and LF LPO, in a single macro.

4.5.1.2.1 Features

The main features of the LPO are:

- Supplies a clock at extremely low power for power-saving modes. This is connected as clock source # 4 of the Global Clock Module.
- Supplies a high-frequency clock for non-timing-critical systems. This is connected as clock source # 5 of the Global Clock Module.
- Provides a comparison clock for the crystal oscillator failure detection circuit.

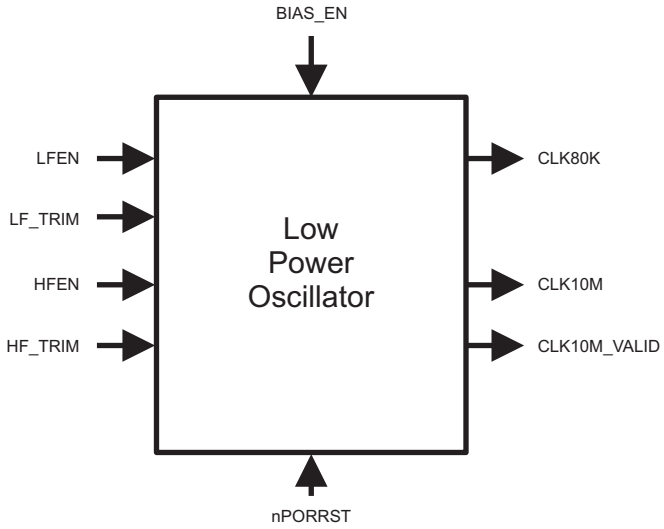


Figure 4-5. LPO Block Diagram

Figure 4-5 shows a block diagram of the internal reference oscillator. This is a low power oscillator (LPO) and provides two clock sources: one nominally 80KHz and one nominally 10MHz.

4.5.1.2.2 LPO Electrical and Timing Specifications

Table 4-10. LPO Specifications

Parameter		MIN	Type	MAX	Unit
LPO - HF oscillator	untrimmed frequency	5.5	9.6	19.5	MHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900µs)			10	µs
	cold startup time			900	µs
LPO - LF oscillator	untrimmed frequency	36	85	180	kHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900µs)			100	µs
	cold startup time			2000	µs

4.5.1.3 Phase Locked Loop (PLL) Clock Modules

The PLL is used to multiply the input frequency to some higher frequency.

The main features of the PLL are:

- Frequency modulation can be optionally superimposed on the synthesized frequency of PLL.
- Configurable frequency multipliers and dividers.
- Built-in PLL Slip monitoring circuit.
- Option to reset the device on a PLL slip detection.

4.5.1.3.1 Block Diagram

Figure below shows a high-level block diagram of the PLL macro on this microcontroller.

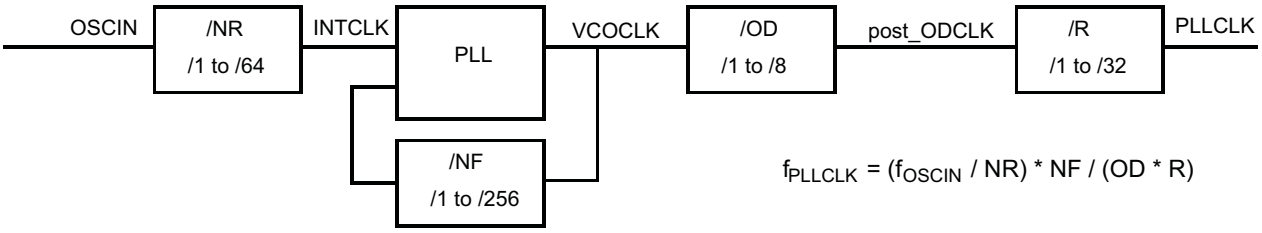


Figure 4-6. PLL Block Diagram

4.5.2 Clock Domains

4.5.2.1 Clock Domain Descriptions

The table below lists the device clock domains and their default clock sources. The table also shows the system module control register that is used to select an available clock source for each clock domain.

Table 4-11. Clock Domain Descriptions

Clock Domain Name	Default Clock Source	Clock Source Selection Register	Description
HCLK	OSCIN	GHVSRC	• Is disabled via the CDDISx registers bit 1
GCLK	OSCIN	GHVSRC	• Always the same frequency as HCLK • In phase with HCLK • Is disabled separately from HCLK via the CDDISx registers bit 0 • Can be divided by 1 up to 8 when running CPU self-test (LBIST) using the CLKDIV field of the STCCLKDIV register at address 0xFFFFE108
GCLK2	OSCIN	GHVSRC	• Always the same frequency as GCLK • 2 cycles delayed from GCLK • Is disabled along with GCLK • Gets divided by the same divider setting as that for GCLK when running CPU self-test (LBIST)
VCLK	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Is disabled separately from HCLK via the CDDISx registers bit 2 • Can be disabled separately for eQEP using CDDISx registers bit 9
VCLK2	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Frequency must be an integer multiple of VCLK frequency • Is disabled separately from HCLK via the CDDISx registers bit 3

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Table 4-11. Clock Domain Descriptions (continued)

Clock Domain Name	Default Clock Source	Clock Source Selection Register	Description
VCLKA1	VCLK	VCLKASRC	• Defaults to VCLK as the source • Frequency can be as fast as HCLK frequency • Is disabled via the CDDISx registers bit 4
RTICLK	VCLK	RCLKSRC	• Defaults to VCLK as the source • If a clock source other than VCLK is selected for RTICLK, then the RTICLK frequency must be less than or equal to VCLK/3 – Application can ensure this by programming the RTI1DIV field of the RCLKSRC register, if necessary • Is disabled via the CDDISx registers bit 6

4.5.2.2 Mapping of Clock Domains to Device Modules

Each clock domain has a dedicated functionality as shown in the figure below.

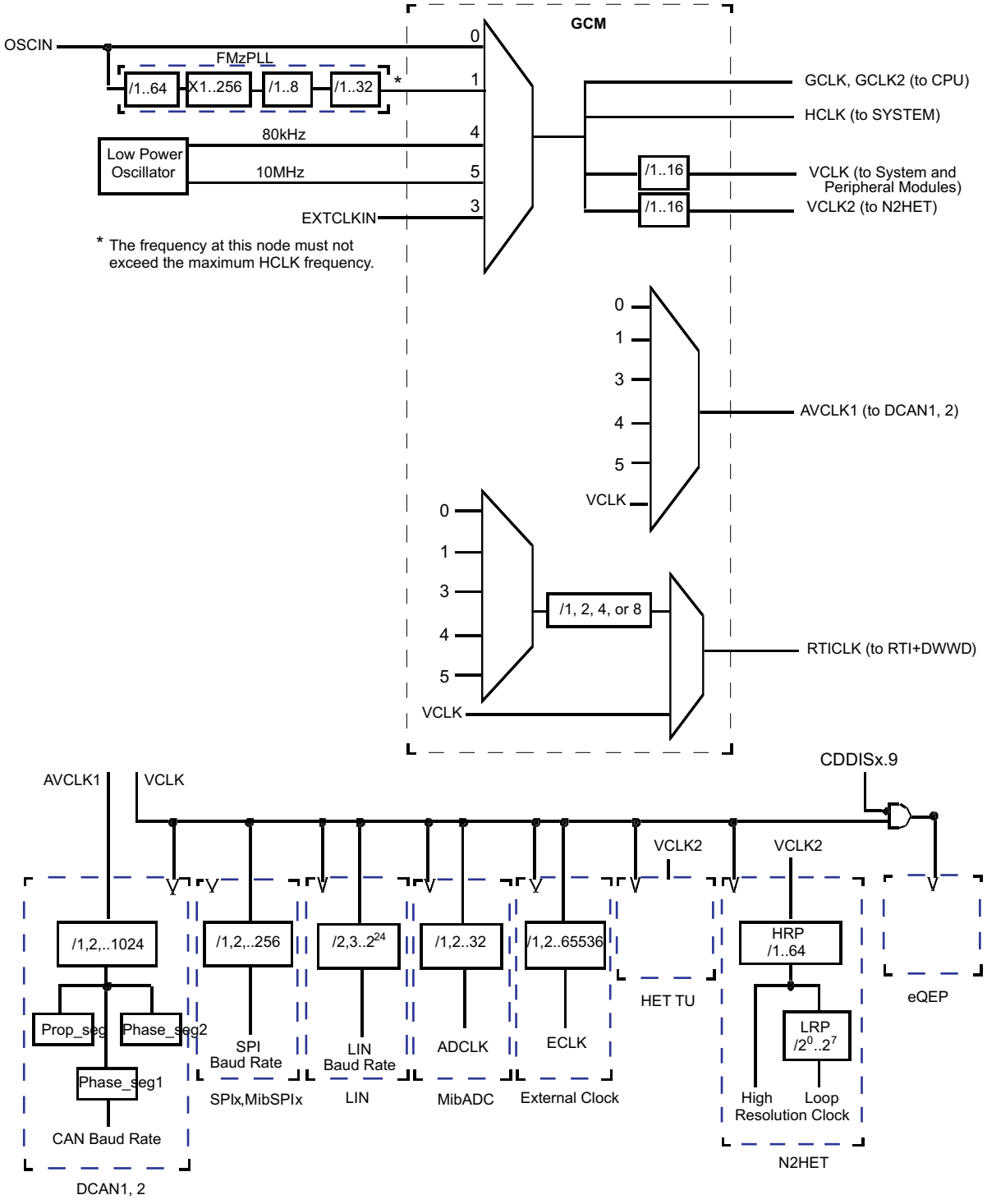

Figure 4-7. Device Clock Domains

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4.5.3 Clock Test Mode

The RM4x platform architecture defines a special mode that allows various clock signals to be brought out on to the ECLK pin and N2HET[2] device outputs. This mode is called the Clock Test mode. It is very useful for debugging purposes and can be configured via the CLKTEST register in the system module.

Table 4-12. Clock Test Mode Options

CLKTEST[3-0]	SIGNAL ON ECLK		CLKTEST[11-8]	SIGNAL ON N2HET[2]
0000	Oscillator		0000	Oscillator Valid Status
0001	Main PLL free-running clock output (PLLCLK)		0001	Main PLL Valid status
0010	Reserved		0010	Reserved
0011	Reserved		0011	Reserved
0100	CLK80K		0100	Reserved
0101	CLK10M		0101	CLK10M Valid status
0110	Reserved		0110	Reserved
0111	Reserved		0111	Reserved
1000	GCLK		1000	CLK80K
1001	RTI Base		1001	Oscillator Valid status
1010	Reserved		1010	Oscillator Valid status
1011	VCLKA1		1011	Oscillator Valid status
1100	Reserved		1100	Oscillator Valid status
1101	Reserved		1101	Oscillator Valid status
1110	Reserved		1110	Oscillator Valid status
1111	Flash HD Pump Oscillator		1111	Oscillator Valid status

4.6 Clock Monitoring

The LPO Clock Detect (LPOCLKDET) module consists of a clock monitor (CLKDET) and an internal low power oscillator (LPO).

The LPO provides two different clock sources – a low frequency (CLK80K) and a high frequency (CLK10M).

The CLKDET is a supervisor circuit for an externally supplied clock signal (OSCIN). In case the OSCIN frequency falls out of a frequency window, the CLKDET flags this condition in the global status register (GLBSTAT bit 0: OSC FAIL) and switches all clock domains sourced by OSCIN to the CLK10M clock (limp mode clock).

The valid OSCIN frequency range is defined as: $f_{CLK10M} / 4 < f_{OSCIN} < f_{CLK10M} * 4$.

4.6.1 Clock Monitor Timings

Table 4-13. LPO and Clock Detection

Parameter		MIN	Type	MAX	Unit
Clock Detection	oscillator fail frequency - lower threshold, using untrimmed LPO output	1.375	2.4	4.875	MHz
	oscillator fail frequency - higher threshold, using untrimmed LPO output	22	38.4	78	MHz
LPO - HF oscillator	untrimmed frequency	5.5	9.6	19.5	MHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900ms)			10	µs
	cold startup time			900	µs
	ICC, CLK10M and CLK80K active			150	µA
LPO - LF oscillator	untrimmed frequency	36	85	180	kHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900ms)			100	µs
	cold startup time			2000	µs
	ICC, only CLK80K active			27	µA
LPO	total ICC STANDBY current			20	µA

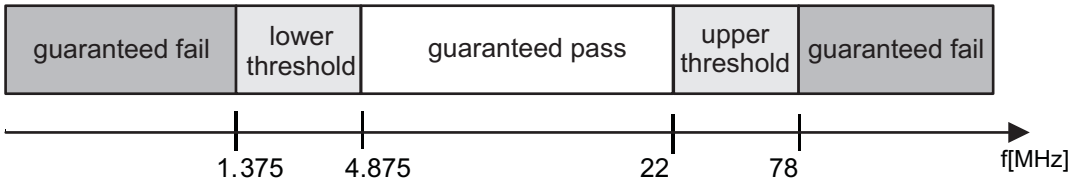

Figure 4-8. LPO and Clock Detection, Untrimmed CLK10M

4.6.2 External Clock (ECLK) Output Functionality

The ECLK pin can be configured to output a pre-scaled clock signal indicative of an internal device clock. This output can be externally monitored as a safety diagnostic.

4.6.3 Dual Clock Comparator

The Dual Clock Comparator (DCC) module determines the accuracy of selectable clock sources by counting the pulses of two independent clock sources (counter 0 and counter 1). If one clock is out of spec, an error signal is generated. For example, the DCC can be configured to use CLK10M as the reference clock (for counter 0) and VCLK as the "clock under test" (for counter 1). This configuration allows the DCC to monitor the PLL output clock when VCLK is using the PLL output as its source.

An additional use of this module is to measure the frequency of a selectable clock source, using the input clock as a reference, by counting the pulses of two independent clock sources. Counter 0 generates a fixed-width counting window after a preprogrammed number of pulses. Counter 1 generates a fixed-width pulse (1 cycle) after a pre-programmed number of pulses. This pulse sets as an error signal if counter 1 does not reach 0 within the counting window generated by counter 0.

4.6.3.1 Features

- Takes two different clock sources as input to two independent counter blocks.
- One of the clock sources is the known-good, or reference clock; the second clock source is the "clock under test."
- Each counter block is programmable with initial, or seed values.
- The counter blocks start counting down from their seed values at the same time; a mismatch from the expected frequency for the clock under test generates an error signal which is used to interrupt the CPU.

4.6.3.2 Mapping of DCC Clock Source Inputs

Table 4-14. DCC Counter 0 Clock Sources

TEST MODE	CLOCK SOURCE [3:0]	CLOCK NAME
0	others	oscillator (OSCIN)
	0x5	high frequency LPO
	0xA	test clock (TCK)
1	X	VCLK

Table 4-15. DCC Counter 1 Clock Sources

TEST MODE	KEY [3:0]	CLOCK SOURCE [3:0]	CLOCK NAME
0	others	-	N2HET[31]
	0xA	0x0	Main PLL free-running clock output
		0x1	n/a
		0x2	low frequency LPO
		0x3	high frequency LPO
		0x4	flash HD pump oscillator
		0x5	EXTCLKIN
		0x6	n/a
		0x7	ring oscillator
		0x8 - 0xF	VCLK
1	X	X	HCLK

4.7 Glitch Filters

A glitch filter is present on the following signals.

Table 4-16. Glitch Filter Timing Specifications

Pin	Parameter		MIN	MAX	Unit
nPORRST	$t_{f(nPORRST)}$	Filter time nPORRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset(1)	500	2000	ns
nRST	$t_{f(nRST)}$	Filter time nRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	500	2000	ns
TEST	$t_{f(TEST)}$	Filter time TEST pin; pulses less than MIN will be filtered out, pulses greater than MAX will pass through	500	2000	ns

(1) The glitch filter design on the nPORRST signal is designed such that no size pulse will reset any part of the microcontroller (flash pump, I/O pins, etc.) without also generating a valid reset signal to the CPU.

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4.8 Device Memory Map

4.8.1 Memory Map Diagram

The figure below shows the device memory map.

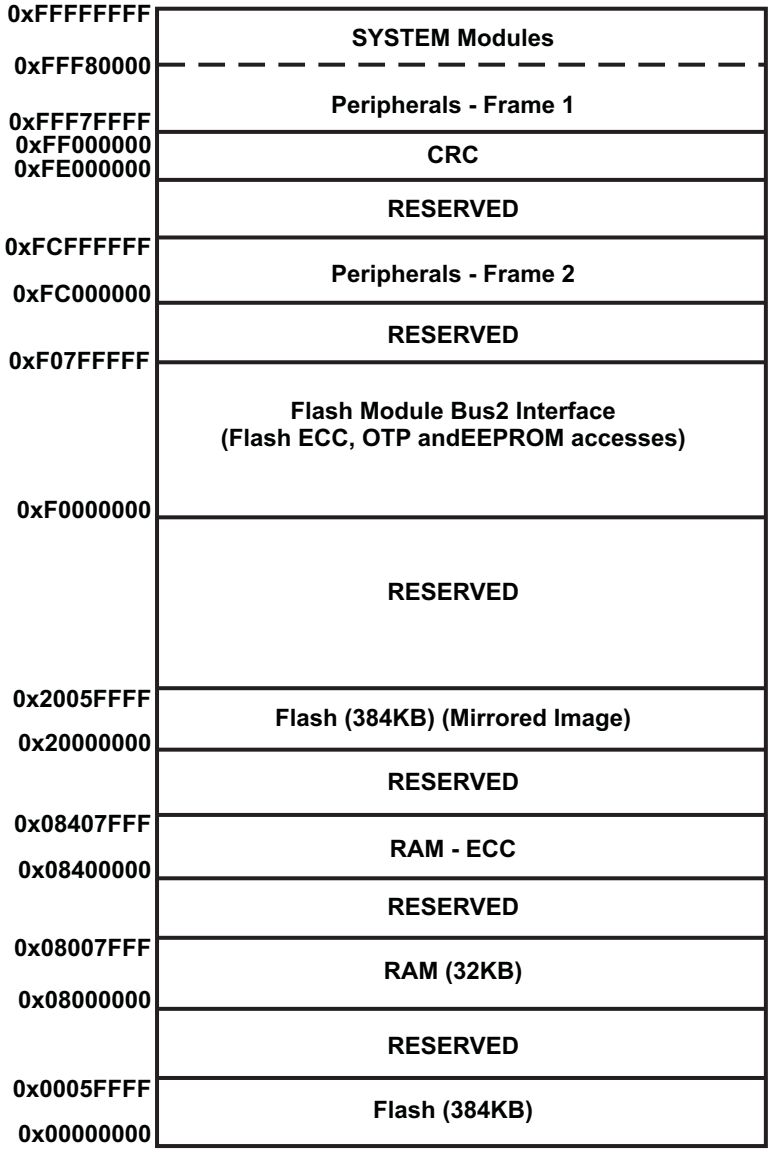

Figure 4-9. RM42LS432 Memory Map

The Flash memory in all configurations is mirrored to support ECC logic testing. The base address of the mirrored Flash image is 0x2000 0000.

4.8.2 Memory Map Table

Please refer to Figure 1-1 for a block diagram showing the device interconnects.

Table 4-17. Device Memory Map

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
Memories tightly coupled to the ARM Cortex-R4 CPU						
TCM Flash	CS0	0x0000_0000	0x00FF_FFFF	16MB	384KB	Abort
TCM RAM + RAM ECC	CSRAM0	0x0800_0000	0x0BFF_3FFF	64MB	32KB	
Mirrored Flash	Flash mirror frame	0x2000_0000	0x20FF_FFFF	16MB	384KB	
Flash Module Bus2 Interface						
Customer OTP, TCM Flash Banks	0xF000_0000	0xF000_FFFF	64KB	2KB		Abort
Customer OTP, EEPROM Bank	0xF000_E000	0xF000_FFFF	8KB	1KB		
Customer OTP–ECC, TCM Flash Banks	0xF004_0000	0xF004_03FF	1KB	512B		
Customer OTP–ECC, EEPROM Bank	0xF004_1C00	0xF004_1FFF	1KB	128B		
TI OTP, TCM Flash Banks	0xF008_0000	0xF008_FFFF	64KB	2KB		
TI OTP, EEPROM Bank	0xF008_E000	0xF008_FFFF	8KB	1KB		
TI OTP–ECC, TCM Flash Banks	0xF00C_0000	0xF00C_03FF	8KB	512B		
TI OTP–ECC, EEPROM Bank	0xF00C_1C00	0xF00C_1FFF	1KB	128B		
EEPROM Bank–ECC	0xF010_0000	0xF013_FFFF	256KB	2KB		
EEPROM Bank	0xF020_0000	0xF03F_FFFF	2MB	16KB		
Flash Data Space ECC	0xF040_0000	0xF04F_FFFF	1MB	48KB		
Cyclic Redundancy Checker (CRC) Module Registers						
CRC	CRC frame	0xFE00_0000	0xFEFF_FFFF	16MB	512B	Accesses above 0x200 generate abort.
Peripheral Memories						
MIBSPI1 RAM	PCS[7]	0xFF0E_0000	0xFF0F_FFFF	128KB	2KB	Abort for accesses above 2KB
DCAN2 RAM	PCS[14]	0xFF1C_0000	0xFF1D_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
DCAN1 RAM	PCS[15]	0xFF1E_0000	0xFF1F_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
MIBADC RAM	PCS[31]	0xFF3E_0000	0xFF3F_FFFF	128KB	8KB	Wrap around for accesses to unimplemented address offsets lower than 0x1FFF.
MIBADC Look-Up Table					384 bytes	Look-up table for ADC wrapper. Starts at offset 0x2000 ans ends at 0x217F. Wrap around for accesses between offsets 0x180 and 0x3FFF. Aborts generated for accesses beyond 0x4000

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Table 4-17. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
N2HET RAM	PCS[35]	0xFF46_0000	0xFF47_FFFF	128KB	16KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF.
N2HET RAM	PCS[39]	0xFF4E_0000	0xFF4F_FFFF	128KB	1KB	Abort
Debug Components						
CoreSight Debug ROM	CSCS0	0xFFA0_0000	0xFFA0_0FFF	4KB	4KB	Reads return zeros, writes have no effect
Cortex-R4 Debug	CSCS1	0xFFA0_1000	0xFFA0_1FFF	4KB	4KB	Reads return zeros, writes have no effect
Peripheral Control Registers						
HTU	PS[22]	0xFFF7_A400	0xFFF7_A4FF	256B	256B	Reads return zeros, writes have no effect
N2HET	PS[17]	0xFFF7_B800	0xFFF7_B8FF	256B	256B	Reads return zeros, writes have no effect
GIO	PS[16]	0xFFF7_BC00	0xFFF7_BCFF	256B	256B	Reads return zeros, writes have no effect
MIBADC	PS[15]	0xFFF7_C000	0xFFF7_C1FF	512B	512B	Reads return zeros, writes have no effect
DCAN1	PS[8]	0xFFF7_DC00	0xFFF7_DDFF	512B	512B	Reads return zeros, writes have no effect
DCAN2	PS[8]	0xFFF7_DE00	0xFFF7_DFFF	512B	512B	Reads return zeros, writes have no effect
LIN	PS[6]	0xFFF7_E400	0xFFF7_E4FF	256B	256B	Reads return zeros, writes have no effect
MibSPI1	PS[2]	0xFFF7_F400	0xFFF7_F5FF	512B	512B	Reads return zeros, writes have no effect
SPI2	PS[2]	0xFFF7_F600	0xFFF7_F7FF	512B	512B	Reads return zeros, writes have no effect
SPI3	PS[1]	0xFFF7_F800	0xFFF7_F9FF	512B	512B	Reads return zeros, writes have no effect
EQEP	PS[25]	0xFFF7_9900	0xFFF7_99FF	256B	256B	Reads return zeros, writes have no effect
EQEP (Mirrored)	PS2[25]	0xFCF7_9900	0xFCF7_99FF	256B	256B	Reads return zeros, writes have no effect
System Modules Control Registers and Memories						
VIM RAM	PPCS2	0xFFF8_2000	0xFFF8_2FFF	4KB	1KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FF. Accesses beyond 0x3FF will be ignored.
Flash Wrapper	PPCS7	0xFFF8_7000	0xFFF8_7FFF	4KB	4KB	Abort
eFuse Farm Controller	PPCS12	0xFFF8_C000	0xFFF8_CFFF	4KB	4KB	Abort
PCR registers	PPS0	0xFFFF_E000	0xFFFF_E0FF	256B	256B	Reads return zeros, writes have no effect
System Module - Frame 2 (see device TRM)	PPS0	0xFFFF_E100	0xFFFF_E1FF	256B	256B	Reads return zeros, writes have no effect
PBIST	PPS1	0xFFFF_E400	0xFFFF_E5FF	512B	512B	Reads return zeros, writes have no effect
STC	PPS1	0xFFFF_E600	0xFFFF_E6FF	256B	256B	Reads return zeros, writes have no effect
IOMM Multiplexing control module	PPS2	0xFFFF_EA00	0xFFFF_EBFF	512B	512B	Generates address error interrupt if enabled.

Table 4-17. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
DCC	PPS3	0xFFFF_EC00	0xFFFF_ECFF	256B	256B	Reads return zeros, writes have no effect
ESM	PPS5	0xFFFF_F500	0xFFFF_F5FF	256B	256B	Reads return zeros, writes have no effect
CCMR4	PPS5	0xFFFF_F600	0xFFFF_F6FF	256B	256B	Reads return zeros, writes have no effect
RAM ECC even	PPS6	0xFFFF_F800	0xFFFF_F8FF	256B	256B	Reads return zeros, writes have no effect
RAM ECC odd	PPS6	0xFFFF_F900	0xFFFF_F9FF	256B	256B	Reads return zeros, writes have no effect
RTI + DWWD	PPS7	0xFFFF_FC00	0xFFFF_FCFF	256B	256B	Reads return zeros, writes have no effect
VIM Parity	PPS7	0xFFFF_FD00	0xFFFF_FDFF	256B	256B	Reads return zeros, writes have no effect
VIM	PPS7	0xFFFF_FE00	0xFFFF_FEFF	256B	256B	Reads return zeros, writes have no effect
System Module - Frame 1 (see device TRM)	PPS7	0xFFFF_FF00	0xFFFF_FFFF	256B	256B	Reads return zeros, writes have no effect

4.8.3 Master/Slave Access Privileges

The table below lists the access permissions for each bus master on the device. A bus master is a module that can initiate a read or a write transaction on the device.

Each slave module on the main interconnect is listed in the table. A "Yes" indicates that the module listed in the "MASTERS" column can access that slave module.

Table 4-18. Master / Slave Access Matrix

MASTERS	ACCESS MODE	SLAVES ON MAIN SCR			
		Flash Module Bus2 Interface: OTP, ECC, EEPROM Bank	Non-CPU Accesses to Program Flash and CPU Data RAM	CRC	Peripheral Control Registers, All Peripheral Memories, And All System Module Control Registers And Memories
CPU READ	User/Privilege	Yes	Yes	Yes	Yes
CPU WRITE	User/Privilege	No	Yes	Yes	Yes
HTU	Privilege	No	Yes	Yes	Yes

4.9 Flash Memory

4.9.1 Flash Memory Configuration

Flash Bank: A separate block of logic consisting of 1 to 16 sectors. Each flash bank normally has a customer-OTP and a TI-OTP area. These flash sectors share input/output buffers, data paths, sense amplifiers, and control logic.

Flash Sector: A contiguous region of flash memory which must be erased simultaneously due to physical construction constraints.

Flash Pump: A charge pump which generates all the voltages required for reading, programming, or erasing the flash banks.

Flash Module: Interface circuitry required between the host CPU and the flash banks and pump module.

Table 4-19. Flash Memory Banks and Sectors

Memory Arrays (or Banks)(1)	Block No.	Sector No.	Segment	Low Address	High Address
BANK0 (384kBytes)	0	0	8K Bytes	0x0000_0000	0x0000_1FFF
		1	8K Bytes	0x0000_2000	0x0000_3FFF
		2	8K Bytes	0x0000_4000	0x0000_5FFF
		3	8K Bytes	0x0000_6000	0x0000_7FFF
		4	8K Bytes	0x0000_8000	0x0000_9FFF
		5	8K Bytes	0x0000_A000	0x0000_BFFF
		6	8K Bytes	0x0000_C000	0x0000_DFFF
		7	8K Bytes	0x0000_E000	0x0000_FFFF
		8	8K Bytes	0x0001_0000	0x0001_1FFF
		9	8K Bytes	0x0001_2000	0x0001_3FFF
		10	8K Bytes	0x0001_4000	0x0001_5FFF
		11	8K Bytes	0x0001_6000	0x0001_7FFF
		12	32K Bytes	0x0001_8000	0x0001_FFFF
	1	13	128K Bytes	0x0002_0000	0x0003_FFFF
	2	14	128K Bytes	0x0004_0000	0x0005_FFFF
BANK7 (16kBytes) for EEPROM emulation(2)(3)	0	0	4K Bytes	0xF020_0000	0xF020_0FFF
	1	1	4K Bytes	0xF020_1000	0xF020_1FFF
	2	2	4K Bytes	0xF020_2000	0xF020_2FFF
	3	3	4K Bytes	0xF020_3000	0xF020_3FFF

(1) The Flash banks are 144-bit wide bank with ECC support.
(2) Flash bank7 is an FLEE bank and can be programmed while executing code from flash bank0.
(3) Code execution is not allowed from flash bank7.

4.9.2 Main Features of Flash Module

- Support for multiple flash banks for program and/or data storage
- Simultaneous read access on a bank while performing program or erase operation on any other bank
- Integrated state machines to automate flash erase and program operations
- Software interface for flash program and erase operations
- Pipelined mode operation to improve instruction access interface bandwidth
- Support for Single Error Correction Double Error Detection (SECDED) block inside Cortex-R4 CPU
  - Error address is captured for host system debugging
- Support for a rich set of diagnostic features

4.9.3 ECC Protection for Flash Accesses

All accesses to the program flash memory are protected by Single Error Correction Double Error Detection (SECDED) logic embedded inside the CPU. The flash module provides 8 bits of ECC code for 64 bits of instructions or data fetched from the flash memory. The CPU calculates the expected ECC code based on the 64 bits received and compares it with the ECC code returned by the flash module. A signle-bit error is corrected and flagged by the CPU, while a multi-bit error is only flagged. The CPU signals an ECC error via its Event bus. This signaling mechanism is not enabled by default and must be enabled by setting the "X" bit of the Performance Monitor Control Register, c9.

```
MRC p15,#0,r1,c9,c12,#0    ;Enabling Event monitor states
ORR r1, r1, #0x00000010
MCR p15,#0,r1,c9,c12,#0    ;Set 4th bit (‘X’) of PMNC register
MRC p15,#0,r1,c9,c12,#0
```

The application must also explicitly enable the CPU's ECC checking for accesses on the CPU's ATCM and BTCM interfaces. These are connected to the program flash and data RAM respectively. ECC checking for these interfaces can be done by setting the B1TCMPCEN, B0TCMPCEN and ATCMPCEN bits of the System Control coprocessor's Auxiliary Control Register, c1.

```
MRC p15, #0, r1, c1, c0, #1
ORR r1, r1, #0x0e000000        ;Enable ECC checking for ATCM and BTCMs
DMB
MCR p15, #0, r1, c1, c0, #1
```

4.9.4 Flash Access Speeds

For information on flash memory access speeds and the relevant wait states required, refer to Section 3.4.

4.10 Flash Program and Erase Timings for Program Flash

Table 4-20. Timing Specifications for Program Flash

Parameter			MIN	NOM	MAX	Unit
t_{prog} (144bit)	Wide Word (144bit) programming time			40	300	µs
t_{prog} (Total)	384KByte programming time(1)	-40°C to 105°C			4	s
		0°C to 60°C, for first 25 cycles		1	2	s
t_{erase}	Sector/Bank erase time	-40°C to 105°C		0.30	4	s
		0°C to 60°C, for first 25 cycles		14	100	ms
t_{wec}	Write/erase cycles with 15 year Data Retention requirement	-40°C to 105°C			1000	cycles

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.

4.11 Flash Program and Erase Timings for Data Flash

Table 4-21. Timing Specifications for Data Flash

Parameter			MIN	NOM	MAX	Unit
t_{prog} (72 bit)	Wide Word (72bit) programming time			40	300	µs
t_{prog} (Total)	64KByte programming time(1)	-40°C to 105°C			1.3	s
		0°C to 60°C, for first 25 cycles		330	660	ms
t_{erase}	Sector/Bank erase time	-40°C to 105°C		0.200	8	s
		0°C to 60°C, for first 25 cycles		14	100	ms
t_{wec}	Write/erase cycles with 15 year Data Retention requirement	-40°C to 105°C			100000	cycles

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.

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4.12 Tightly-Coupled RAM Interface Module

Figure 4-10 illustrates the connection of the Tightly Coupled RAM (TCRAM) to the Cortex-R4™ CPU.

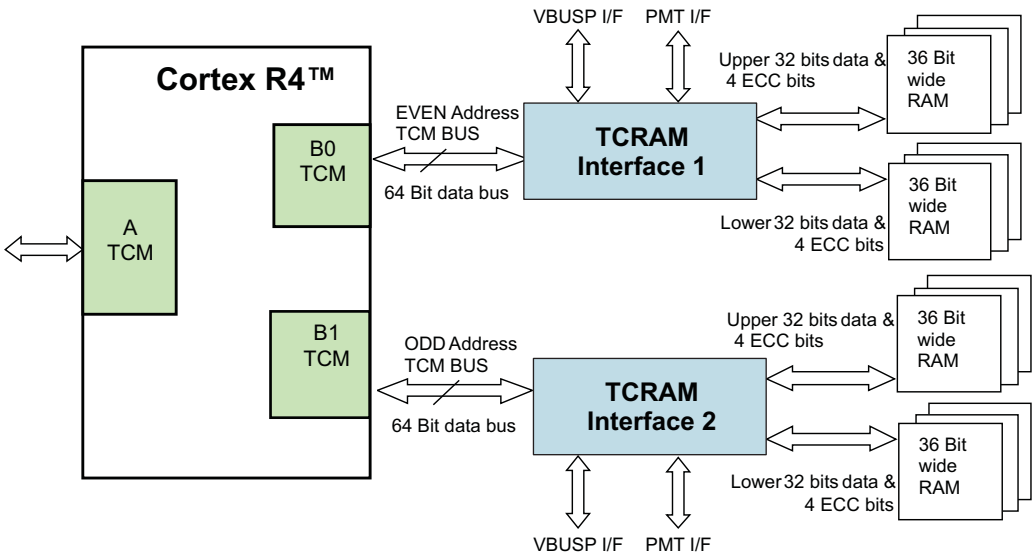

Figure 4-10. TCRAM Block Diagram

4.12.1 Features

The features of the Tightly Coupled RAM (TCRAM) Module are:

- Acts as slave to the Cortex-R4 CPU's BTCM interface
- Supports CPU's internal ECC scheme by providing 64-bit data and 8-bit ECC code
- Monitors CPU Event Bus and generates single or multi-bit error interrupts
- Stores addresses for single and multi-bit errors
- Provides CPU address bus integrity checking by supporting parity checking on the address bus
- Performs redundant address decoding for the RAM bank chip select and ECC select generation logic
- Provides enhanced safety for the RAM addressing by implementing two 36-bit wide byte-interleaved RAM banks and generating independent RAM access control signals to the two banks
- Supports auto-initialization of the RAM banks along with the ECC bits
- No support for bit-wise RAM accesses

4.12.2 TCRAMW ECC Support

The TCRAMW passes on the ECC code for each data read by the Cortex-R4 CPU from the RAM. It also stores the CPU's ECC port contents in the ECC RAM when the CPU does a write to the RAM. The TCRAMW monitors the CPU's event bus and provides registers for indicating single/multi-bit errors and also for identifying the address that caused the single or multi-bit error. The event signaling and the ECC checking for the RAM accesses must be enabled inside the CPU.

For more information see the device Technical Reference Manual.

4.13 Parity Protection for Accesses to peripheral RAMs

Accesses to some peripheral RAMs are protected by odd/even parity checking. During a read access the parity is calculated based on the data read from the peripheral RAM and compared with the good parity value stored in the parity RAM for that peripheral. If any word fails the parity check, the module generates a parity error signal that is mapped to the Error Signaling Module. The module also captures the peripheral RAM address that caused the parity error.

The parity protection for peripheral RAMs is not enabled by default and must be enabled by the application. Each individual peripheral contains control registers to enable the parity protection for accesses to its RAM.

NOTE

The CPU read access gets the actual data from the peripheral. The application can choose to generate an interrupt whenever a peripheral RAM parity error is detected.

4.14 On-Chip SRAM Initialization and Testing

4.14.1 On-Chip SRAM Self-Test Using PBIST

4.14.1.1 Features

- Extensive instruction set to support various memory test algorithms
- ROM-based algorithms allow application to run TI production-level memory tests
- Independent testing of all on-chip SRAM

4.14.1.2 PBIST RAM Groups

Table 4-22. PBIST RAM Grouping

Memory	RAM Group	Test Clock	MEM Type	Test Pattern (Algorithm)			
				triple read slow read	triple read fast read	March 13N[1] two port (cycles)	March 13N[1] single port (cycles)
				ALGO MASK 0x1	ALGO MASK 0x2	ALGO MASK 0x4	ALGO MASK 0x8
PBIST_ROM	1	ROM CLK	ROM	X	X		
STC_ROM	2	ROM CLK	ROM	X	X		
DCAN1	3	VCLK	Dual Port			12720	
DCAN2	4	VCLK	Dual Port			6480	
ESRAM1	6	HCLK	Single Port				133160
MIBSPI1	7	VCLK	Dual Port			33440	
VIM	10	VCLK	Dual Port			12560	
MIBADC	11	VCLK	Dual Port			4200	
N2HET1	13	VCLK	Dual Port			25440	
HET TU1	14	VCLK	Dual Port			6480	

(1) There are several memory testing algorithms stored in the PBIST ROM. However, TI recommends the March13N algorithm for application testing.

The PBIST ROM clock can be divided down from HCLK. The divider is selected by programming the ROM_DIV field of the Memory Self-Test Global Control Register (MSTGCR) at address 0xFFFFFF58.

4.14.2 On-Chip SRAM Auto Initialization

This microcontroller allows some of the on-chip memories to be initialized via the Memory Hardware Initialization mechanism in the System module. This hardware mechanism allows an application to program the memory arrays with error detection capability to a known state based on their error detection scheme (odd/even parity or ECC).

The MINITGCR register enables the memory initialization sequence, and the MSINENA register selects the memories that are to be initialized.

For more information on these registers refer to the device Technical Reference Manual.

The mapping of the different on-chip memories to the specific bits of the MSINENA registers is shown in Table 4-23.

Table 4-23. Memory Initialization

CONNECTING MODULE	ADDRESS RANGE		MSINENA REGISTER BIT #(1)
	BASE ADDRESS	ENDING ADDRESS	
RAM	0x08000000	0x08007FFF	0
MIBSPI1 RAM	0xFF0E0000	0xFF0FFFFF	7(2)
DCAN2 RAM	0xFF1C0000	0xFF1DFFFF	6
DCAN1 RAM	0xFF1E0000	0xFF1FFFFF	5
MIBADC RAM	0xFF3E0000	0xFF3FFFFF	8
N2HET RAM	0xFF460000	0xFF47FFFF	3
HET TU RAM	0xFF4E0000	0xFF4FFFFF	4
VIM RAM	0xFFF82000	0xFFF82FFF	2

(1) Unassigned register bits are reserved.
(2) The MibSPI1 module performs an initialization of the transmit and receive RAMs as soon as the module is brought out of reset using the SPI Global Control Register 0 (SPIGCR0). This is independent of whether the application chooses to initialize the MibSPI1 RAMs using the system module auto-initialization method.

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4.15 Vectored Interrupt Manager

The vectored interrupt manager (VIM) provides hardware assistance for prioritizing and controlling the many interrupt sources present on this device. Interrupts are caused by events outside of the normal flow of program execution. Normally, these events require a timely response from the central processing unit (CPU); therefore, when an interrupt occurs, the CPU switches execution from the normal program flow to an interrupt service routine (ISR).

4.15.1 VIM Features

The VIM module has the following features:

- Supports 96 interrupt channels.
  - Provides programmable priority and enable for interrupt request lines.
- Provides a direct hardware dispatch mechanism for fastest IRQ dispatch.
- Provides two software dispatch mechanisms when the CPU VIC port is not used.
  - Index interrupt
  - Register vectored interrupt
- Parity protected vector interrupt table against soft errors.

4.15.2 Interrupt Request Assignments

Table 4-24. Interrupt Request Assignments

Modules	Interrupt Sources	Default VIM Interrupt Channel
ESM	ESM High level interrupt (NMI)	0
Reserved	Reserved	1
RTI	RTI compare interrupt 0	2
RTI	RTI compare interrupt 1	3
RTI	RTI compare interrupt 2	4
RTI	RTI compare interrupt 3	5
RTI	RTI overflow interrupt 0	6
RTI	RTI overflow interrupt 1	7
Reserved	Reserved	8
GIO	GIO interrupt A	9
N2HET	N2HET level 0 interrupt	10
HET TU	HET TU level 0 interrupt	11
MIBSPI1	MIBSPI1 level 0 interrupt	12
LIN	LIN level 0 interrupt	13
MIBADC	MIBADC event group interrupt	14
MIBADC	MIBADC sw group 1 interrupt	15
DCAN1	DCAN1 level 0 interrupt	16
SPI2	SPI2 level 0 interrupt	17
Reserved	Reserved	18
Reserved	Reserved	19
ESM	ESM Low level interrupt	20
SYSTEM	Software interrupt (SSI)	21
CPU	PMU interrupt	22
GIO	GIO interrupt B	23
N2HET	N2HET level 1 interrupt	24
HET TU	HET TU level 1 interrupt	25
MIBSPI1	MIBSPI1 level 1 interrupt	26

Table 4-24. Interrupt Request Assignments (continued)

Modules	Interrupt Sources	Default VIM Interrupt Channel
LIN	LIN level 1 interrupt	27
MIBADC	MIBADC sw group 2 interrupt	28
DCAN1	DCAN1 level 1 interrupt	29
SPI2	SPI2 level 1 interrupt	30
MIBADC	MIBADC magnitude compare interrupt	31
Reserved	Reserved	32-34
DCAN2	DCAN2 level 0 interrupt	35
Reserved	Reserved	36
SPI3	SPI3 level 0 interrupt	37
SPI3	SPI3 level 1 interrupt	38
Reserved	Reserved	39-41
DCAN2	DCAN2 level 1 interrupt	42
Reserved	Reserved	43-60
FMC	FSM_DONE interrupt	61
Reserved	Reserved	62-79
HWAG	HWA_INT_REQ_H	80
Reserved	Reserved	81
DCC	DCC done interrupt	82
Reserved	Reserved	83
eQEPINTn	eQEP Interrupt	84
PBIST	PBIST Done Interrupt	85
Reserved	Reserved	86-87
HWAG	HWA_INT_REQ_L	88
Reserved	Reserved	89-95

NOTE

Address location 0x00000000 in the VIM RAM is reserved for the phantom interrupt ISR entry; therefore only request channels 0..94 can be used and are offset by 1 address in the VIM RAM.

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4.16 Real Time Interrupt Module

The real-time interrupt (RTI) module provides timer functionality for operating systems and for benchmarking code. The RTI module can incorporate several counters that define the timebases needed for scheduling an operating system.

The timers also allow you to benchmark certain areas of code by reading the values of the counters at the beginning and the end of the desired code range and calculating the difference between the values.

4.16.1 Features

The RTI module has the following features:

- Two independent 64 bit counter blocks
- Four configurable compares for generating operating system ticks. Each event can be driven by either counter block 0 or counter block 1.
- Fast enabling/disabling of events
- Two time-stamp (capture) functions for system or peripheral interrupts, one for each counter block

4.16.2 Block Diagrams

Figure 4-11 shows a high-level block diagram for one of the two 64-bit counter blocks inside the RTI module. Both the counter blocks are identical.

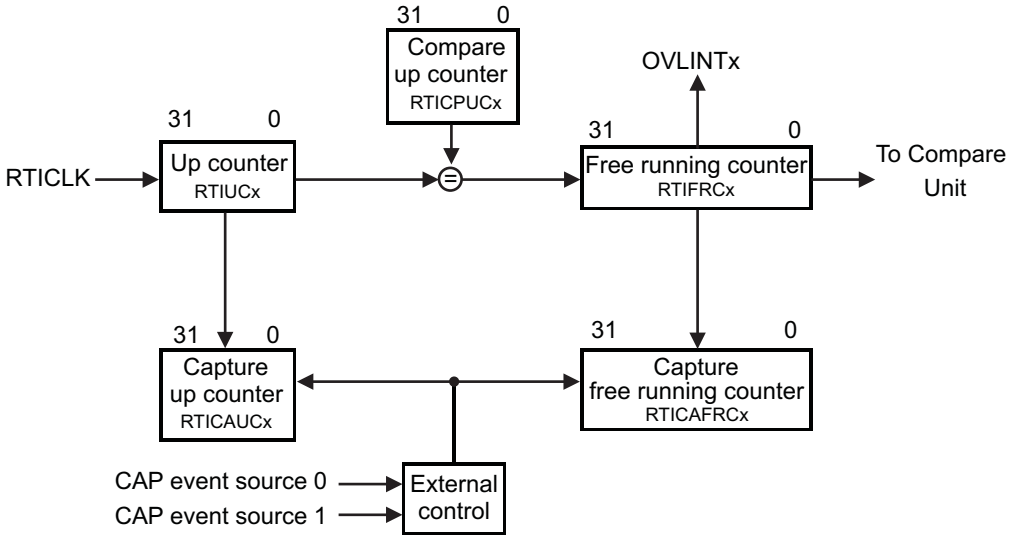

Figure 4-11. Counter Block Diagram

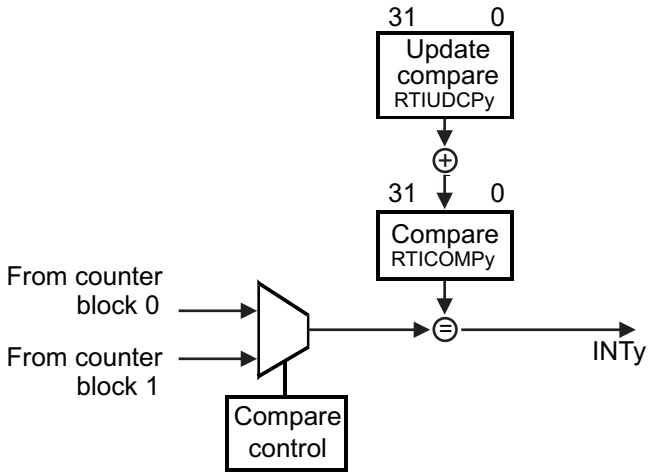

Figure 4-12. Compare Block Diagram

4.16.3 Clock Source Options

The RTI module uses the RTICLK clock domain for generating the RTI time bases.

The application can select the clock source for the RTICLK by configuring the RCLKSRC register in the System module at address 0xFFFFFF50. The default source for RTICLK is VCLK.

For more information on clock sources refer to Table 4-8 and Table 4-11.

4.17 Error Signaling Module

The Error Signaling Module (ESM) manages the various error conditions on the RM4x microcontroller. The error condition is handled based on a fixed severity level assigned to it. Any severe error condition can be configured to drive a low level on a dedicated device terminal called nERROR. This can be used as an indicator to an external monitor circuit to put the system into a safe state.

4.17.1 Features

The features of the Error Signaling Module are:

- 128 interrupt/error channels are supported, divided into 3 different groups
  - 64 channels with maskable interrupt and configurable error pin behavior
  - 32 error channels with non-maskable interrupt and predefined error pin behavior
  - 32 channels with predefined error pin behavior only
- Error pin to signal severe device failure
- Configurable timebase for error signal
- Error forcing capability

4.17.2 ESM Channel Assignments

The Error Signaling Module (ESM) integrates all the device error conditions and groups them in the order of severity. Group1 is used for errors of the lowest severity while Group3 is used for errors of the highest severity. The device response to each error is determined by the severity group it is connected to. Table 4-26 shows the channel assignment for each group.

Table 4-25. ESM Groups

ERROR GROUP	INTERRUPT CHARACTERISTICS	INFLUENCE ON ERROR PIN
Group1	maskable, low or high priority	configurable
Group2	non-maskable, high priority	fixed
Group3	no interrupt generated	fixed

Table 4-26. ESM Channel Assignments

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group1	0
Reserved	Group1	1
Reserved	Group1	2
Reserved	Group1	3
Reserved	Group1	4
Reserved	Group1	5
FMC - correctable error: bus1 and bus2 interfaces (does not include accesses to EEPROM bank)	Group1	6
N2HET - parity	Group1	7
HET TU - parity	Group1	8
HET TU - MPU	Group1	9
PLL - Slip	Group1	10
Clock Monitor - interrupt	Group1	11
Reserved	Group1	12
Reserved	Group1	13
Reserved	Group1	14
VIM RAM - parity	Group1	15
Reserved	Group1	16
MibSPI1 - parity	Group1	17

Table 4-26. ESM Channel Assignments (continued)

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group1	18
MibADC - parity	Group1	19
Reserved	Group1	20
DCAN1 - parity	Group1	21
Reserved	Group1	22
DCAN2 - parity	Group1	23
Reserved	Group1	24
Reserved	Group1	25
RAM even bank (B0TCM) - correctable error	Group1	26
CPU - selftest	Group1	27
RAM odd bank (B1TCM) - correctable error	Group1	28
Reserved	Group1	29
DCC - error	Group1	30
CCM-R4 - selftest	Group1	31
Reserved	Group1	32
Reserved	Group1	33
Reserved	Group1	34
FMC - correctable error (EEPROM bank access)	Group1	35
FMC - uncorrectable error (EEPROM bank access)	Group1	36
IOMM - Mux configuration error	Group1	37
Reserved	Group1	38
Reserved	Group1	39
eFuse farm – this error signal is generated whenever any bit in the eFuse farm error status register is set. The application can choose to generate and interrupt whenever this bit is set in order to service any eFuse farm error condition.	Group1	40
eFuse farm - self test error. It is not necessary to generate a separate interrupt when this bit gets set.	Group1	41
Reserved	Group1	42
Reserved	Group1	43
Reserved	Group1	44
Reserved	Group1	45
Reserved	Group1	46
Reserved	Group1	47
Reserved	Group1	48
Reserved	Group1	49
Reserved	Group1	50
Reserved	Group1	51
Reserved	Group1	52
Reserved	Group1	53
Reserved	Group1	54
Reserved	Group1	55
Reserved	Group1	56
Reserved	Group1	57
Reserved	Group1	58
Reserved	Group1	59
Reserved	Group1	60
Reserved	Group1	61
Reserved	Group1	62

Table 4-26. ESM Channel Assignments (continued)

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group1	63
Reserved	Group2	0
Reserved	Group2	1
CCMR4 - compare	Group2	2
Reserved	Group2	3
FMC - uncorrectable error (address parity on bus1 accesses)	Group2	4
Reserved	Group2	5
RAM even bank (B0TCM) - uncorrectable error	Group2	6
Reserved	Group2	7
RAM odd bank (B1TCM) - uncorrectable error	Group2	8
Reserved	Group2	9
RAM even bank (B0TCM) - address bus parity error	Group2	10
Reserved	Group2	11
RAM odd bank (B1TCM) - address bus parity error	Group2	12
Reserved	Group2	13
Reserved	Group2	14
Reserved	Group2	15
Flash (ATCM) - ECC live lock detect	Group2	16
Reserved	Group2	17
Reserved	Group2	18
Reserved	Group2	19
Reserved	Group2	20
Reserved	Group2	21
Reserved	Group2	22
Reserved	Group2	23
RTI_WWD_NMI	Group2	24
Reserved	Group2	25
Reserved	Group2	26
Reserved	Group2	27
Reserved	Group2	28
Reserved	Group2	29
Reserved	Group2	30
Reserved	Group2	31
Reserved	Group3	0
eFuse Farm - autoload error	Group3	1
Reserved	Group3	2
RAM even bank (B0TCM) - ECC uncorrectable error	Group3	3
Reserved	Group3	4
RAM odd bank (B1TCM) - ECC uncorrectable error	Group3	5
Reserved	Group3	6
FMC - uncorrectable error: bus1 and bus2 interfaces (does not include address parity error and errors on accesses to EEPROM bank)	Group3	7
Reserved	Group3	8
Reserved	Group3	9
Reserved	Group3	10
Reserved	Group3	11
Reserved	Group3	12
Reserved	Group3	13

Table 4-26. ESM Channel Assignments (continued)

ERROR SOURCES	GROUP	CHANNELS
Reserved	Group3	14
Reserved	Group3	15
Reserved	Group3	16
Reserved	Group3	17
Reserved	Group3	18
Reserved	Group3	19
Reserved	Group3	20
Reserved	Group3	21
Reserved	Group3	22
Reserved	Group3	23
Reserved	Group3	24
Reserved	Group3	25
Reserved	Group3	26
Reserved	Group3	27
Reserved	Group3	28
Reserved	Group3	29
Reserved	Group3	30
Reserved	Group3	31

4.18 Reset / Abort / Error Sources

Table 4-27. Reset/Abort/Error Sources

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP group.channel
CPU TRANSACTIONS			
Precise write error (NCNB/Strongly Ordered)	User/Privilege	Precise Abort (CPU)	n/a
Precise read error (NCB/Device or Normal)	User/Privilege	Precise Abort (CPU)	n/a
Imprecise write error (NCB/Device or Normal)	User/Privilege	Imprecise Abort (CPU)	n/a
Illegal instruction	User/Privilege	Undefined Instruction Trap (CPU)(1)	n/a
MPU access violation	User/Privilege	Abort (CPU)	n/a
SRAM			
B0 TCM (even) ECC single error (correctable)	User/Privilege	ESM	1.26
B0 TCM (even) ECC double error (non-correctable)	User/Privilege	Abort (CPU), ESM => nERROR	3.3
B0 TCM (even) uncorrectable error (i.e. redundant address decode)	User/Privilege	ESM => NMI => nERROR	2.6
B0 TCM (even) address bus parity error	User/Privilege	ESM => NMI => nERROR	2.10
B1 TCM (odd) ECC single error (correctable)	User/Privilege	ESM	1.28
B1 TCM (odd) ECC double error (non-correctable)	User/Privilege	Abort (CPU), ESM => nERROR	3.5
B1 TCM (odd) uncorrectable error (i.e. redundant address decode)	User/Privilege	ESM => NMI => nERROR	2.8
B1 TCM (odd) address bus parity error	User/Privilege	ESM => NMI => nERROR	2.12
FLASH WITH CPU BASED ECC			
FMC correctable error - Bus1 and Bus2 interfaces (does not include accesses to EEPROM bank)	User/Privilege	ESM	1.6
FMC uncorrectable error - Bus1 accesses (does not include address parity error)	User/Privilege	Abort (CPU), ESM => nERROR	3.7
FMC uncorrectable error - Bus2 accesses (does not include address parity error and EEPROM bank accesses)	User/Privilege	ESM => nERROR	3.7
FMC uncorrectable error - address parity error on Bus1 accesses	User/Privilege	ESM => NMI => nERROR	2.4
FMC correctable error - Accesses to EEPROM bank	User/Privilege	ESM	1.35
FMC uncorrectable error - Accesses to EEPROM bank	User/Privilege	ESM	1.36
HET TU (HTU)			
NCNB (Strongly Ordered) transaction with slave error response	User/Privilege	Interrupt => VIM	n/a
External imprecise error (Illegal transaction with ok response)	User/Privilege	Interrupt => VIM	n/a
Memory access permission violation	User/Privilege	ESM	1.9
Memory parity error	User/Privilege	ESM	1.8
N2HET			
Memory parity error	User/Privilege	ESM	1.7
MIBSPI			
MibSPI1 memory parity error	User/Privilege	ESM	1.17
MIBADC			
MibADC Memory parity error	User/Privilege	ESM	1.19
DCAN			
DCAN1 memory parity error	User/Privilege	ESM	1.21
DCAN2 memory parity error	User/Privilege	ESM	1.23

(1) The Undefined Instruction TRAP is NOT detectable outside the CPU. The trap is taken only if the instruction reaches the execute stage of the CPU.

Table 4-27. Reset/Abort/Error Sources (continued)

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP group.channel
PLL			
PLL slip error	User/Privilege	ESM	1.10
CLOCK MONITOR			
Clock monitor interrupt	User/Privilege	ESM	1.11
DCC			
DCC error	User/Privilege	ESM	1.30
CCM-R4			
Self test failure	User/Privilege	ESM	1.31
Compare failure	User/Privilege	ESM => NMI => nERROR	2.2
VIM			
Memory parity error	User/Privilege	ESM	1.15
VOLTAGE MONITOR			
VMON out of voltage range	n/a	Reset	n/a
CPU SELFTEST (LBIST)			
CPU Selftest (LBIST) error	User/Privilege	ESM	1.27
PIN MULTIPLEXING CONTROL			
Mux configuration error	User/Privilege	ESM	1.37
eFuse Controller			
eFuse Controller Autoload error	User/Privilege	ESM => nERROR	3.1
eFuse Controller - Any bit set in the error status register	User/Privilege	ESM	1.40
eFuse Controller self-test error	User/Privilege	ESM	1.41
WINDOWED WATCHDOG			
WWD Non-Maskable Interrupt exception	n/a	ESM => NMI => nERROR	2.24
ERRORS REFLECTED IN THE SYSESR REGISTER			
Power-Up Reset	n/a	Reset	n/a
Oscillator fail / PLL slip(2)	n/a	Reset	n/a
Watchdog exception	n/a	Reset	n/a
CPU Reset (driven by the CPU STC)	n/a	Reset	n/a
Software Reset	n/a	Reset	n/a
External Reset	n/a	Reset	n/a

(2) Oscillator fail/PLL slip can be configured in the system register (SYS.PLLCTL1) to generate a reset.

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4.19 Digital Windowed Watchdog

This device includes a digital windowed watchdog (DWWD) module that protects against runaway code execution.

The DWWD module allows the application to configure the time window within which the DWWD module expects the application to service the watchdog. A watchdog violation occurs if the application services the watchdog outside of this window, or fails to service the watchdog at all. The application can choose to generate a system reset or a non-maskable interrupt to the CPU in case of a watchdog violation.

The watchdog is disabled by default and must be enabled by the application. Once enabled, the watchdog can only be disabled upon a system reset.

4.20 Debug Subsystem

4.20.1 Block Diagram

The device contains an ICEPICK module to allow JTAG access to the scan chains.

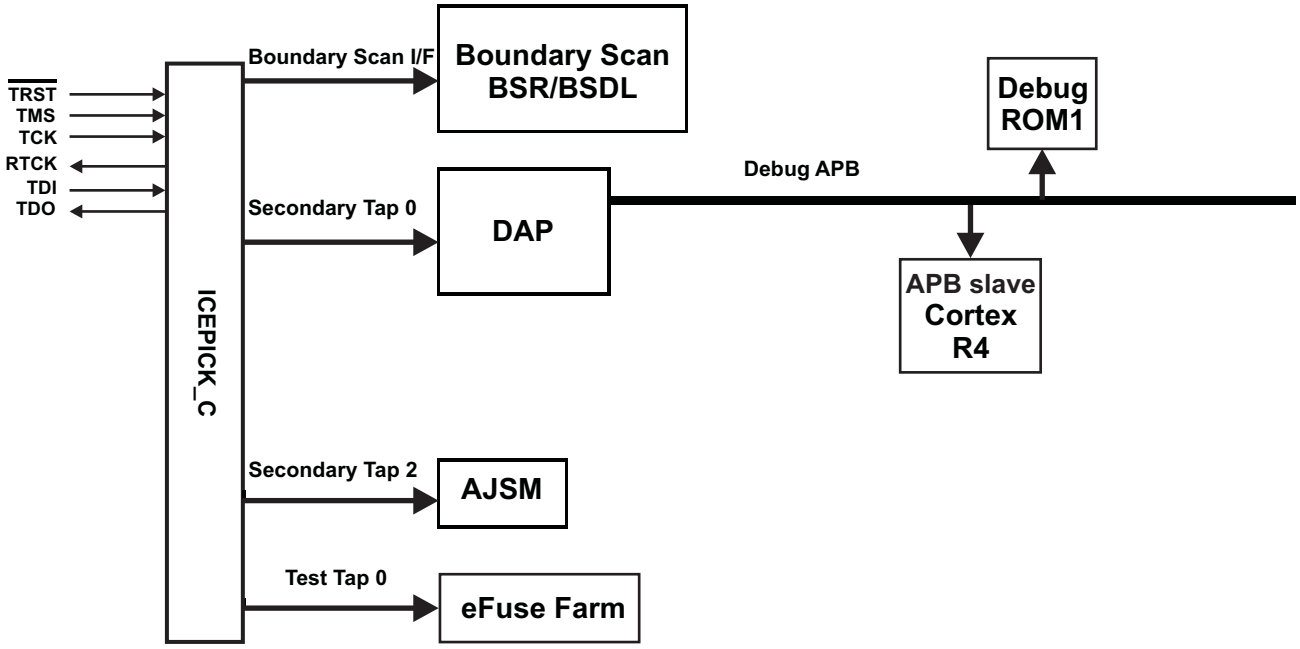

Figure 4-13. ZWT Debug Subsystem Block Diagram

4.20.2 Debug Components Memory Map

Table 4-28. Debug Components Memory Map

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
CoreSight Debug ROM	CSCS0	0xFFA0_0000	0xFFA0_0FFF	4KB	4KB	Reads return zeros, writes have no effect
Cortex-R4 Debug	CSCS1	0xFFA0_1000	0xFFA0_1FFF	4KB	4KB	Reads return zeros, writes have no effect

4.20.3 JTAG Identification Code

The JTAG ID code for this device is 0x0B97102F. This is the same as the device ICEPick Identification Code.

4.20.4 Debug ROM

The Debug ROM stores the location of the components on the Debug APB bus:

Table 4-29. Debug ROM table

ADDRESS	DESCRIPTION	VALUE
0x000	pointer to Cortex-R4	0x0000 1003
0x001	Reserved	0x0000 2002
0x002	Reserved	0x0000 3002
0x003	Reserved	0x0000 4002
0x004	end of table	0x0000 0000

4.20.5 JTAG Scan Interface Timings

Table 4-30. JTAG Scan Interface Timing(1)

No.	Parameter		Min	MAX	Unit
	fTCK	TCK frequency (at HCLKmax)		12	MHz
	fRTCK	RTCK frequency (at TCKmax and HCLKmax)	10		MHz
1	td(TCK -RTCK)	Delay time, TCK to RTCK		24	ns
2	tsu(TDI/TMS - RTCKr)	Setup time, TDI, TMS before RTCK rise (RTCKr)	15		ns
3	th(RTCKr -TDI/TMS)	Hold time, TDI, TMS after RTCKr	0		ns
4	th(RTCKr -TDO)	Hold time, TDO after RTCKf	0		ns
5	td(TCKf -TDO)	Delay time, TDO valid after RTCK fall (RTCKf)		10	ns

(1) Timings for TDO are specified for a maximum of 50pF load on TDO

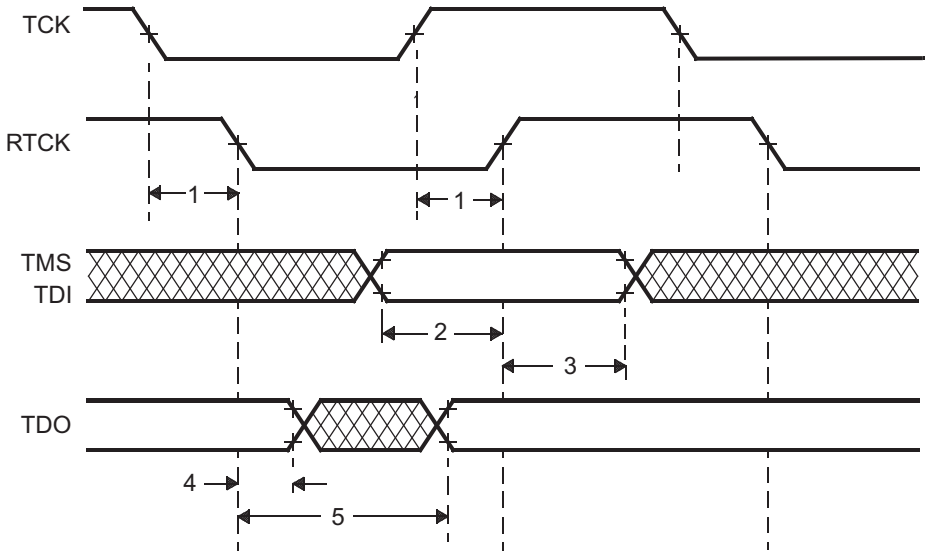

Figure 4-14. JTAG Timing

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4.20.6 Advanced JTAG Security Module

This device includes a an Advanced JTAG Security Module (AJSM). which provides maximum security to the device's memory content by allowing users to secure the device after programming.

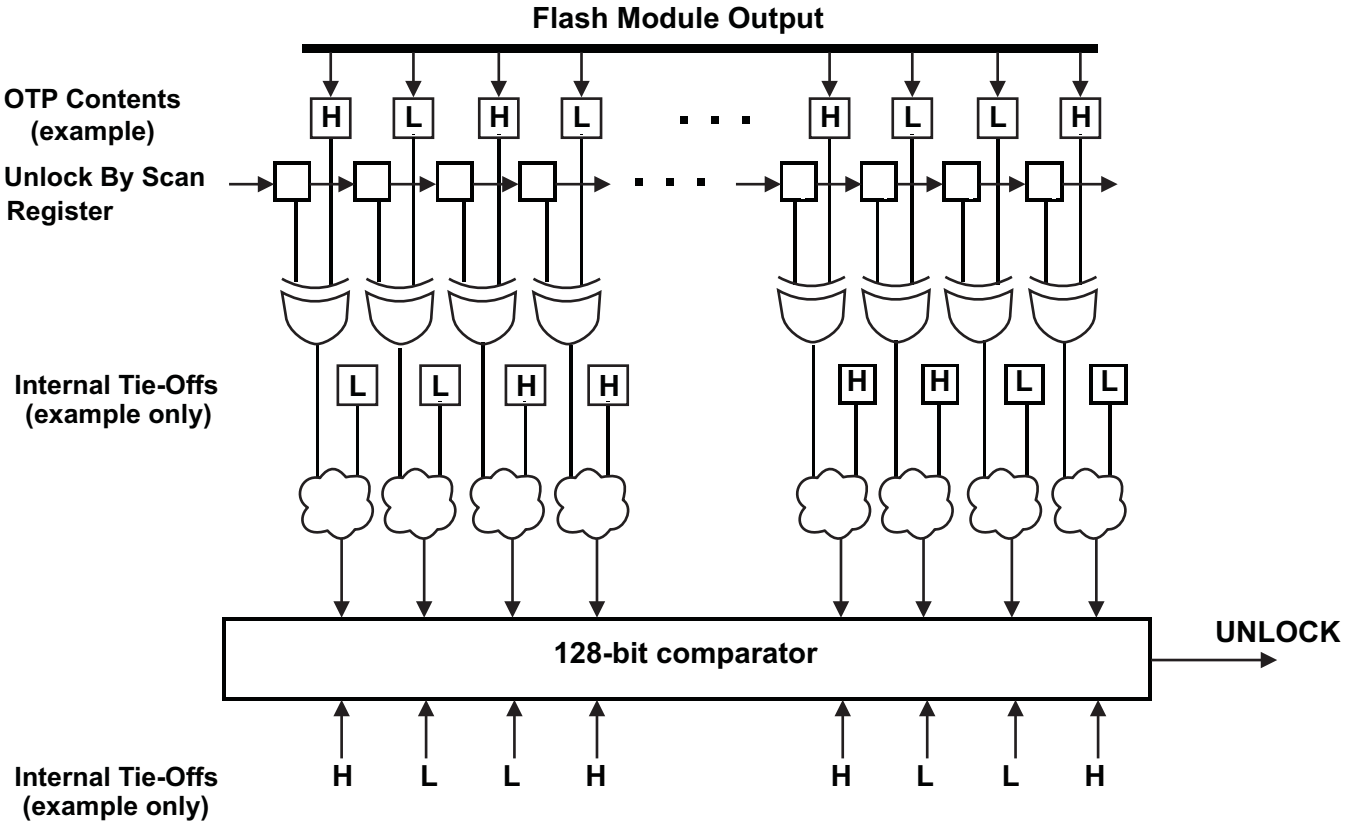

Figure 4-15. AJSM Unlock

The device is unsecure by default by virtue of a 128-bit visible unlock code programmed in the OTP address 0xF0000000.The OTP contents are XOR-ed with the "Unlock By Scan" register contents. The outputs of these XOR gates are again combined with a set of secret internal tie-offs. The output of this combinational logic is compared against a secret hard-wired 128-bit value. A match results in the UNLOCK signal being asserted, so that the device is now unsecure.

A user can secure the device by changing at least one bit in the visible unlock code from 1 to 0. Changing a 0 to 1 is not possible since the visible unlock code is stored in the One Time Programmable (OTP) flash region. Also, changing all the 128 bits to zeros is not a valid condition and will permanently secure the device.

Once secured, a user can unsecure the device by scanning an appropriate value into the "Unlock By Scan" register of the AJSM module. The value to be scanned is such that the XOR of the OTP contents and the Unlock-By-Scan register contents results in the original visible unlock code.

The Unlock-By-Scan register is reset only upon asserting power-on reset (nPORRST).

A secure device only permits JTAG accesses to the AJSM scan chain via the Secondary Tap # 2 of the ICEPick module. All other secondary taps, test taps and the boundary scan interface are not accessible in this state.

4.20.7 Boundary Scan Chain

The device supports BSDL-compliant boundary scan for testing pin-to-pin compatibility. The boundary scan chain is connected to the Boundary Scan Interface of the ICEPICK module.

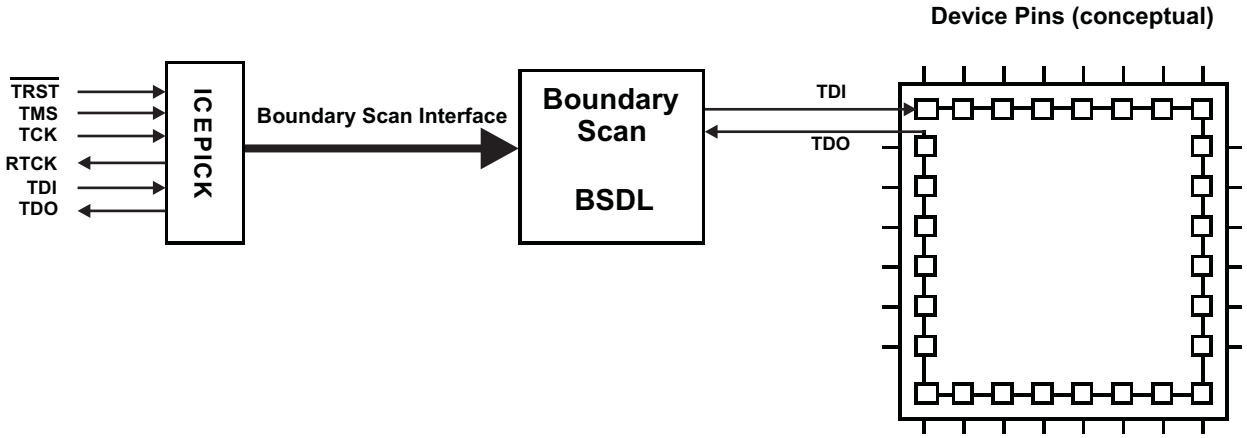

Figure 4-16. Boundary Scan Implementation (Conceptual Diagram)

Data is serially shifted into all boundary-scan buffers via TDI, and out via TDO.

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5 Peripheral Information and Electrical Specifications

5.1 Peripheral Legend

Table 5-1. Peripheral Legend

Abbreviation	Full Name
MibADC	Multi-Buffered Analog to Digital Converter
CCM-R4	CPU Compare Module – CortexR4
CRC	Cyclic Redundancy Check
DCAN	Controller Area Network
DCC	Dual Clock Comparator
ESM	Error Signaling Module
GIO	General-Purpose Input/Output
HTU	High End Timer Transfer Unit
LIN	Local Interconnect Network
MibSPI	Multi-Buffered Serial Peripheral Interface
N2HET	Platform High End Timer
RTI	Real-Time Interrupt Module
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
VIM	Vectored Interrupt Manager
eQEP	Enhanced Quadrature Encoder Pulse

5.2 Multi-Buffered 12-bit Analog-to-Digital Converter

The multibuffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on V_{SS} and V_{CC} from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

Table 5-2. MibADC Overview

Description	Value
Resolution	12 bits
Monotonic	Assured
Output conversion code	00h to FFFh [00 for $V_{AI} \le AD_{REFLO}$; FFF for $V_{AI} \ge AD_{REFHI}$]

5.2.1 Features

- 12-bit resolution
- AD_{REFHI} and AD_{REFLO} pins (high and low reference voltages)
- Total Sample/Hold/Convert time: 600ns Typical Minimum at 30MHz ADCLK
- One memory region per conversion group is available (event, group 1, group 2)
- Allocation of channels to conversion groups is completely programmable
- Memory regions are serviced by interrupt
- Programmable interrupt threshold counter is available for each group
- Programmable magnitude threshold interrupt for each group for any one channel
- Option to read either 8-bit, 10-bit or 12-bit values from memory regions
- Single or continuous conversion modes
- Embedded self-test
- Embedded calibration logic

- Enhanced power-down mode
  - Optional feature to automatically power down ADC core when no conversion is in progress
- External event pin (ADEVT) programmable as general-purpose I/O

5.2.2 The ADC module supports 3 conversion groups: Event Group, Group1 and Group2. Each of these 3 groups can be configured to be hardware event-triggered. In that case, the application can select from among 8 event sources to be the trigger for a group's conversions.

5.2.2.1 Default MIBADC Event Trigger Hookup

Table 5-3. MIBADC Event Trigger Hookup

Event #	Source Select Bits For G1, G2 Or Event (G1SRC[2:0], G2SRC[2:0] or EVSRC[2:0])	Trigger
1	000	ADEVT
2	001	N2HET[8]
3	010	N2HET[10]
4	011	RTI compare 0 interrupt
5	100	N2HET[12]
6	101	N2HET[14]
7	110	N2HET[17]
8	111	N2HET[19]

NOTE

For ADEVT, N2HET trigger sources, the connection to the MibADC module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad, or by driving the function from an external trigger source as input. If the mux controller module is used to select different functionality instead of ADEVT or N2HET[x], care must be taken to disable these signals from triggering conversions; there is no multiplexing on input connections.

NOTE

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

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5.2.3 ADC Electrical and Timing Specifications

Table 5-4. MibADC Recommended Operating Conditions

Parameter		MIN	MAX	Unit
AD_{REFHI}	A-to-D high-voltage reference source	AD_{REFLO}	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	AD_{REFHI}	V
V_{AI}	Analog input voltage	AD_{REFLO}	AD_{REFHI}	V
I_{AIC}	Analog input clamp current (VAI < VSSAD – 0.3 or VAI > VCCAD + 0.3)	- 2	2	mA

Table 5-5. MibADC Electrical Characteristics Over Full Ranges of Recommended Operating Conditions(1)

Parameter		Description/Conditions		MIN	Type	MAX	Unit
R_{mux}	Analog input mux on-resistance	See Figure 5-1			95	250	Ω
R_{samp}	ADC sample switch on-resistance	See Figure 5-1			60	250	Ω
C_{mux}	Input mux capacitance	See Figure 5-1			7	16	pF
C_{samp}	ADC sample capacitance	See Figure 5-1			8	13	pF
I_{AIL}	Analog off-state input leakage current, for V_{CCAD} = 3.6V maximum	Off-state input leakage per ADC input pin	$V_{SSAD} < V_{IN} < V_{CCAD}$		-0.3	250	nA
$I_{ADREFHI}$	AD_{REFHI} input current	$AD_{REFHI} = V_{CCAD}$, $AD_{REFLO} = V_{SSAD}$				3	mA
I_{CCAD}	Static supply current	Normal operating mode				15	mA
		ADC core in power down mode				5	µA

(1) 1 LSB = $(AD_{REFHI} – AD_{REFLO})/ 2^n$ where n = 10 in 10-bit mode and 12 in 12-bit mode

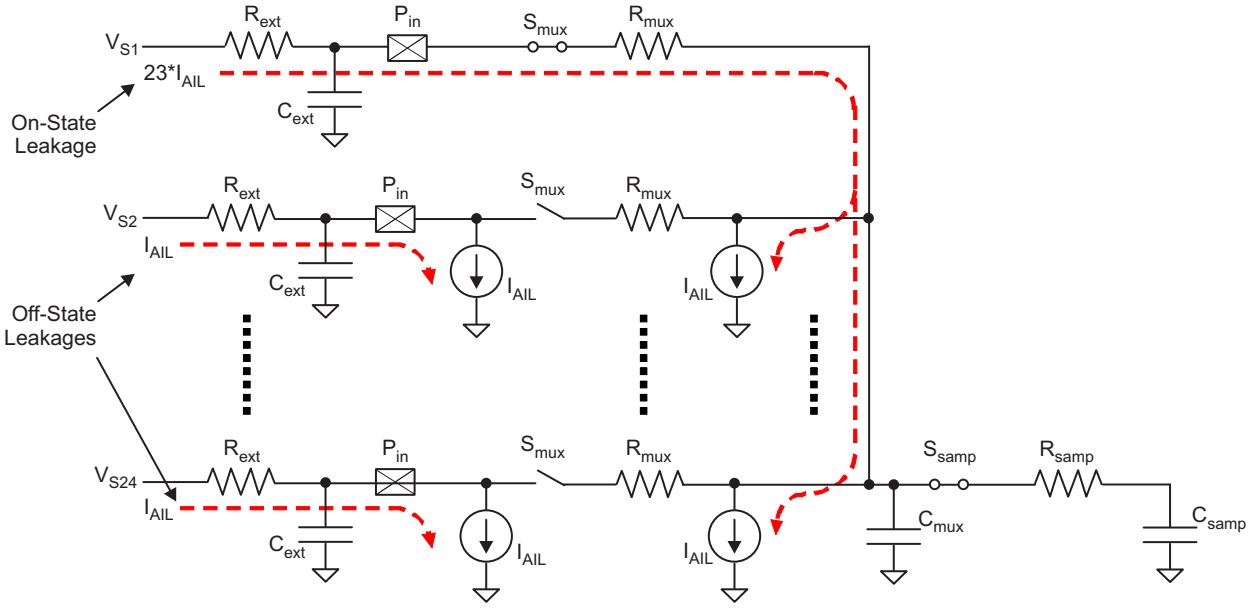

Figure 5-1. MibADC Input Equivalent Circuit

Table 5-6. MibADC Timing Specifications

Parameter		MIN	NOM	MAX	Unit
$t_{c(ADCLK)}$ (1)	Cycle time, MibADC clock	33			ns

(1) The MibADC clock is the ADCLK, generated by dividing down the VCLK by a prescale factor defined by the ADCLOCKCR register bits 4:0.

Table 5-6. MibADC Timing Specifications (continued)

Parameter		MIN	NOM	MAX	Unit
$t_{d(SH)}$ (2)	Delay time, sample and hold time	200			ns
12-bit mode					
$t_{d(C)}$	Delay time, conversion time	400			ns
$t_{d(SHC)}$ (3)	Delay time, total sample/hold and conversion time	600			ns
10-bit mode					
$t_{d(C)}$	Delay time, conversion time	330			ns
$t_{d(SHC)}$ (3)	Delay time, total sample/hold and conversion time	530			ns

(2) The sample and hold time for the ADC conversions is defined by the ADCLK frequency and the AD<GP>SAMP register for each conversion group. The sample time needs to be determined by accounting for the external impedance connected to the input channel as well as the ADC's internal impedance.
(3) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, e.g the prescale settings.

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Table 5-7. MibADC Operating Characteristics Over Full Ranges of Recommended Operating Conditions

Parameter		Description/Conditions		MIN	Type	MAX	Unit
CR	Conversion range over which specified accuracy is maintained	AD_{REFHI} - AD_{REFLO}		3		3.6	V
Z_{SET}	Offset Error	Difference between the first ideal transition (from code 000h to 001h) and the actual transition	10-bit mode			1	LSB
			12-bit mode			2	LSB
F_{SET}	Gain Error	Difference between the last ideal transition (from code FFEh to FFFh) and the actual transition minus offset.	10-bit mode			2	LSB
			12-bit mode			3	LSB
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value. (See Figure 5-2)	10-bit mode			± 1.5	LSB
			12-bit mode			± 2	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. (See Figure 5-3)	10-bit mode			± 2	LSB
			12-bit mode			± 2	LSB
E_{TOT}	Total unadjusted error (after calibration)	Maximum value of the difference between an analog value and the ideal midstep value. (See Figure 5-4)	10-bit mode			± 2	LSB
			12-bit mode			± 4	LSB

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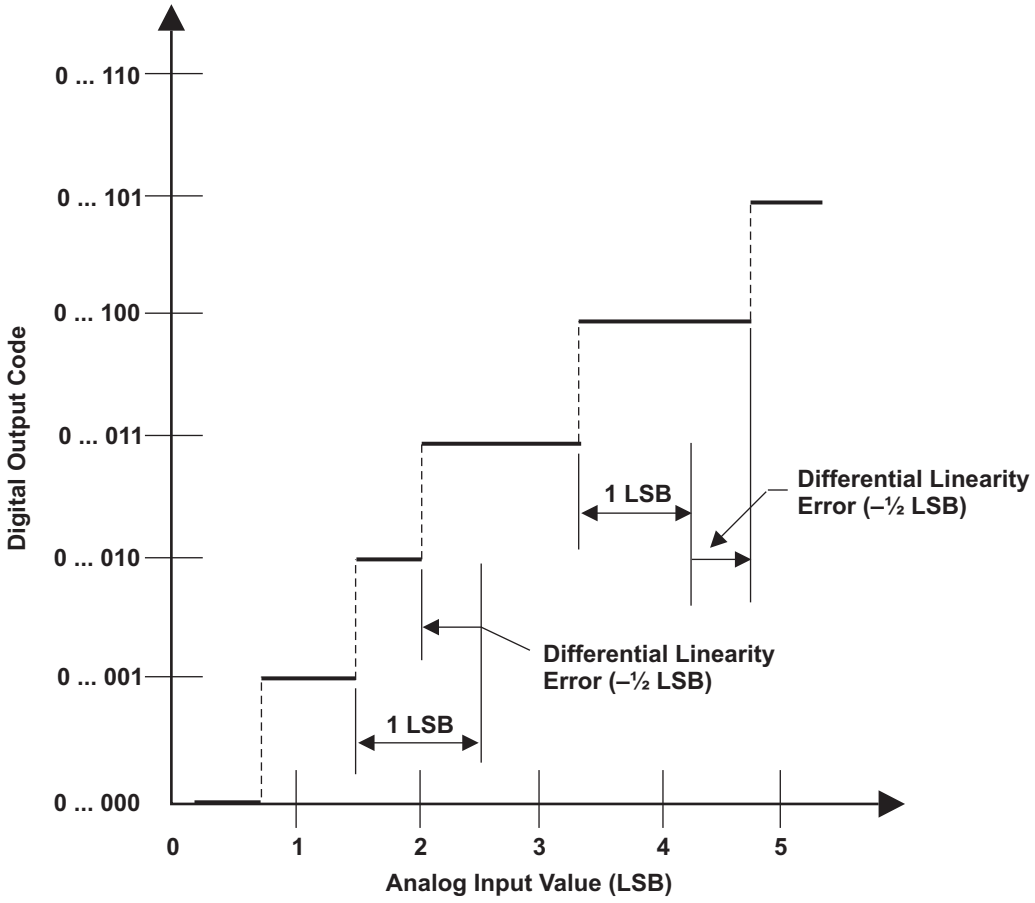
5.2.4 Performance (Accuracy) Specifications

5.2.4.1 MibADC Nonlinearity Errors

The differential nonlinearity error shown in Figure Figure 5-2 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^n$ where n=10 in 10-bit mode and 12 in 12-bit mode

Figure 5-2. Differential Nonlinearity (DNL) Error

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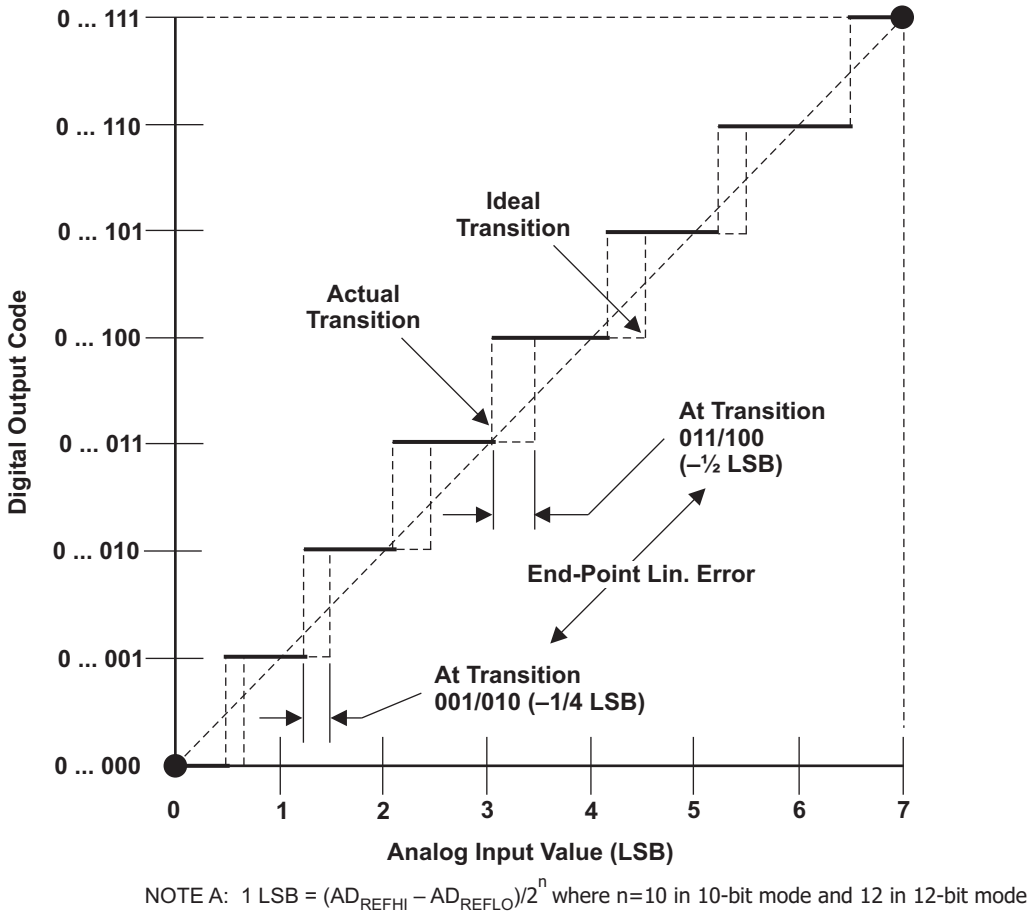
The integral nonlinearity error shown in Figure Figure 5-3 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^n$ where n=10 in 10-bit mode and 12 in 12-bit mode

Figure 5-3. Integral Nonlinearity (INL) Error

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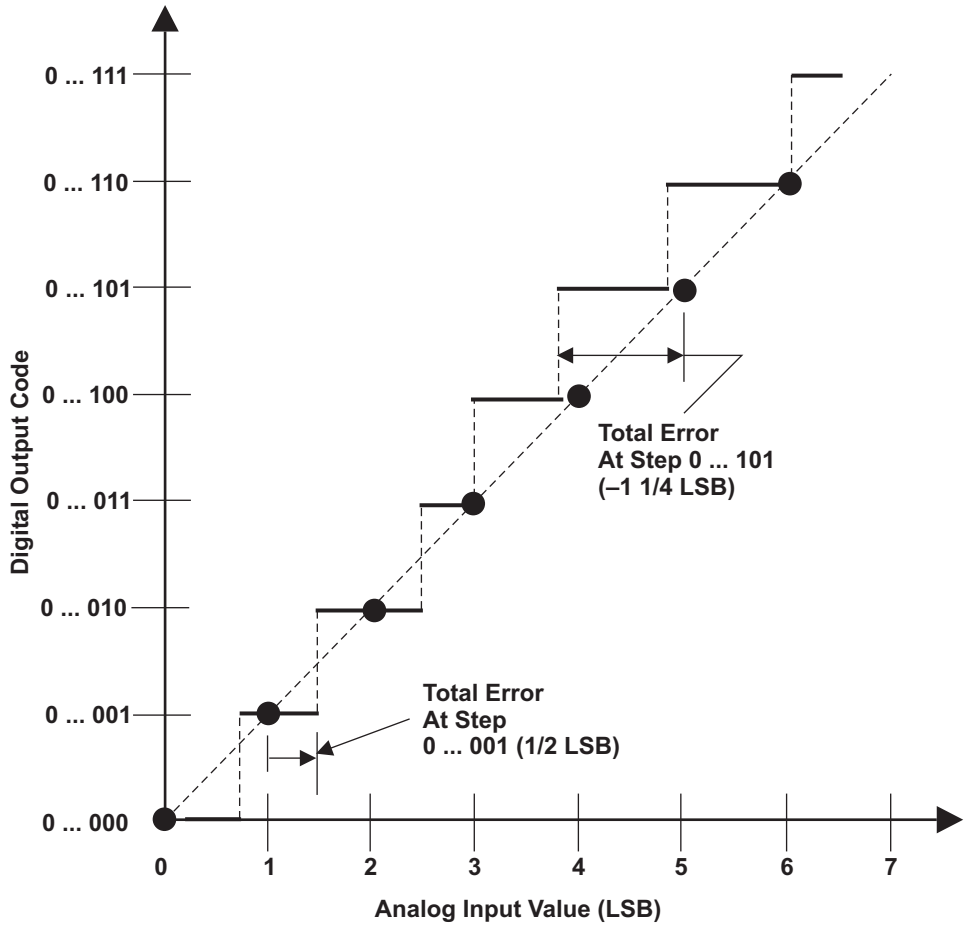
5.2.4.2 MibADC Total Error

The absolute accuracy or total error of an MibADC as shown in Figure Figure 5-4 is the maximum value of the difference between an analog value and the ideal midstep value.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^n$ where n=10 in 10-bit mode and 12 in 12-bit mode

Figure 5-4. Absolute Accuracy (Total) Error

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5.3 General-Purpose Input/Output

The GPIO module on this device supports one port GIOA. The I/O pins are bidirectional and bit-programmable. GIOA supports external interrupt capability.

5.3.1 Features

The GPIO module has the following features:

- Each IO pin can be configured as:
  - Input
  - Output
  - Open Drain
- The interrupts have the following characteristics:
  - Programmable interrupt detection either on both edges or on a single edge (set in GIOINTDET)
  - Programmable edge-detection polarity, either rising or falling edge (set in GIOPOL register)
  - Individual interrupt flags (set in GIOFLG register)
  - Individual interrupt enables, set and cleared through GIOENASET and GIOENACLR registers respectively
  - Programmable interrupt priority, set through GIOLVLSET and GIOLVLCLR registers
- Internal pullup/pulldown allows unused I/O pins to be left unconnected

For information on input and output timings see Section 3.8 and Section 3.9

5.4 Enhanced High-End Timer (N2HET)

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O.. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses.

5.4.1 Features

The N2HET module has the following features:

- Programmable timer for input and output timing functions
- Reduced instruction set (30 instructions) for dedicated time and angle functions
- 128 words of instruction RAM protected by parity
- User defined number of 25-bit virtual counters for timer, event counters and angle counters
- 7-bit hardware counters for each pin allow up to 32-bit resolution in conjunction with the 25-bit virtual counters
- Up to 19 pins usable for input signal measurements or output signal generation
- Programmable suppression filter for each input pin with adjustable limiting frequency
- Low CPU overhead and interrupt load
- Efficient data transfer to or from the CPU memory with dedicated High-End-Timer Transfer Unit (HTU)
- Diagnostic capabilities with different loopback mechanisms and pin status readback functionality

5.4.2 N2HET RAM Organization

The timer RAM uses 4 RAM banks, where each bank has two port access capability. This means that one RAM address may be written while another address is read. The RAM words are 96-bits wide, which are split into three 32-bit fields (program, control, and data).

5.4.3 Input Timing Specifications

The N2HET instructions PCNT and WCAP impose some timing constraints on the input signals.

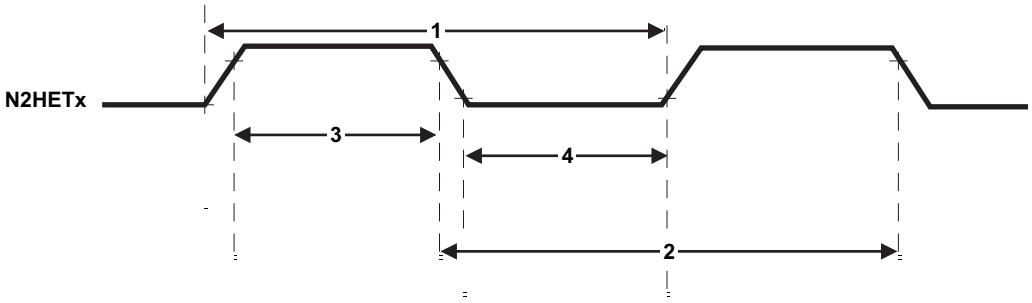

Figure 5-5. N2HET Input Capture Timings

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Table 5-8. Dynamic Characteristics for the N2HET Input Capture Functionality(1)(2)

PARAMETER		MIN	MAX	UNIT
1	Input signal period, PCNT or WCAP for rising edge to rising edge	(HRP) (LRP) $t_{c(VCLK2)}$ + 2	2^{25} (HRP) (LRP) $t_{c(VCLK2)}$ - 2	ns
2	Input signal period, PCNT or WCAP for falling edge to falling edge	(HRP) (LRP) $t_{c(VCLK2)}$ + 2	2^{25} (HRP) (LRP) $t_{c(VCLK2)}$ - 2	ns
3	Input signal high phase, PCNT or WCAP for rising edge to falling edge	2(HRP) $t_{c(VCLK2)}$ + 2	2^{25} (HRP) (LRP) $t_{c(VCLK2)}$ - 2	ns
4	Input signal low phase, PCNT or WCAP for falling edge to rising edge	2(HRP) $t_{c(VCLK2)}$ + 2	2^{25} (HRP) (LRP) $t_{c(VCLK2)}$ - 2	ns

(1) In the above table, LRP = Low Resolution Clock Period and HRP = High Resolution Clock Period
(2) Timings in the above table represent the inclusion of the NHET channel enhancement to allow a finer resolution on input capture.

5.4.4 N2HET Checking

5.4.4.1 Output Monitoring using Dual Clock Comparator (DCC)

N2HET[31] is connected as a clock source for counter 1 in DCC1. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET[31].

N2HET[31] can be configured to be an internal-only channel. That is, the connection to the DCC module is made directly from the output of the N2HET module (from the input of the output buffer).

For more information on DCC see Section 4.6.3.

5.4.5 Disabling N2HET Outputs

Some applications require the N2HET outputs to be disabled under some fault condition. The N2HET module provides this capability via the "Pin Disable" input signal. This signal, when driven low, causes the N2HET outputs identified by a programmable register (HETPINDIS) to be tri-stated. Please refer to the device Technical Reference Manual for more details on the "N2HET Pin Disable" feature.

GIOA[5] and EQEPERR are connected to the "Pin Disable" input for N2HET. In the case of GIOA[5] connection, this connection is made from the output of the input buffer. In the case of EQEPERR, the EQEPERR output signal is asserted in the event of a phase error. This signal is inverted and double-synchronized to VCLK2 for input into the N2HET PIN_nDISABLE port.

The PIN_nDISABLE port input source is selectable between the GIOA[5] and EQEPERR sources. This is achieved via the PINMMR9[1:0] bits.

5.4.6 High-End Timer Transfer Unit (N2HET)

A High End Timer Transfer Unit (N2HET) can perform DMA type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the N2HET.

5.4.6.1 Features

- CPU independent
- Master Port to access system memory
- 8 control packets supporting dual buffer configuration
- Control packet information is stored in RAM protected by parity
- Event synchronization (N2HET transfer requests)
- Supports 32 or 64 bit transactions
- Addressing modes for N2HET address (8 byte or 16 byte) and system memory address (fixed, 32 bit or 64bit)
- One shot, circular and auto switch buffer transfer modes
- Request lost detection

5.4.6.2 Trigger Connections

Table 5-9. N2HET Request Line Connection

Modules	Request Source	HET TU1 Request
N2HET	HTUREQ[0]	HET TU1 DCP[0]
N2HET	HTUREQ[1]	HET TU DCP[1]
N2HET	HTUREQ[2]	HET TU DCP[2]
N2HET	HTUREQ[3]	HET TU DCP[3]
N2HET	HTUREQ[4]	HET TU DCP[4]
N2HET	HTUREQ[5]	HET TU DCP[5]
N2HET	HTUREQ[6]	HET TU DCP[6]
N2HET	HTUREQ[7]	HET TU DCP[7]

5.5 Controller Area Network (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The DCAN is ideal for applications operating in noisy and harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

5.5.1 Features

Features of the DCAN module include:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- The CAN kernel can be clocked by the oscillator for baud-rate generation.
- 32 and 16 mailboxes on DCAN1 and DCAN2, respectively
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM protected by parity
- Direct access to Message RAM during test mode
- CAN Rx / Tx pins configurable as general purpose IO pins
- Message RAM Auto Initialization

For more information on the DCAN see the device Technical Reference Manual.

5.5.2 Electrical and Timing Specifications

Table 5-10. Dynamic Characteristics for the DCANx TX and RX pins

Parameter		MIN	MAX	Unit
$t_{d(CANnTX)}$	Delay time, transmit shift register to CANnTX pin(1)		15	ns
$t_{d(CANnRX)}$	Delay time, CANnRX pin to receive shift register		5	ns

(1) These values do not include rise/fall times of the output buffer.

5.6 Local Interconnect Network Interface (LIN)

The SCI/LIN module can be programmed to work either as an SCI or as a LIN. The core of the module is an SCI. The SCI's hardware features are augmented to achieve LIN compatibility.

The SCI module is a universal asynchronous receiver-transmitter that implements the standard nonreturn to zero format. The SCI can be used to communicate, for example, through an RS-232 port or over a K-line.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master/multiple-slave with a message identification for multi-cast transmission between any network nodes.

5.6.1 LIN Features

The following are features of the LIN module:

- Compatible to LIN 1.3, 2.0 and 2.1 protocols
- Multi-buffered receive and transmit units
- Identification masks for message filtering
- Automatic Master Header Generation
  - Programmable Synch Break Field
  - Synch Field
  - Identifier Field
- Slave Automatic Synchronization
  - Synch break detection
  - Optional baudrate update
  - Synchronization Validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Error detection
- 2 Interrupt lines with priority encoding

5.7 Multi-Buffered / Standard Serial Peripheral Interface

The MibSPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted in and out of the device at a programmed bit-transfer rate. Typical applications for the SPI include interfacing to external peripherals, such as I/Os, memories, display drivers, and analog-to-digital converters.

5.7.1 Features

Both Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator, supports max up to 20Mhz baud rate
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format
- SPI I/Os not used in the communication can be used as digital input/output signals

Table 5-11. MibSPI/SPI Default Configurations

MibSPIx/SPIx	I/Os
MibSPI1	MIBSPI1SIMO[0], MIBSPI1SOMI[0], MIBSPI1CLK, MIBSPI1nCS[3:0], MIBSPI1nENA
SPI2	SPI2SIMO, SPI2SOMI, SPI2CLK, SPI2nCS[0]
SPI3	SPI3SIMO, SPI3SOMI, SPI3CLK, SPI3nENA, SPI3nCS[0]

5.7.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 128 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

5.7.3 MibSPI Transmit Trigger Events

Each of the transfer groups can be configured individually. For each of the transfer groups a trigger event and a trigger source can be chosen. A trigger event can be, for example, a rising edge or a permanent low level at a selectable trigger source. Up to 15 trigger sources are available which can be utilized by each transfer group. These trigger options are listed in Table 5-12 and .

5.7.3.1 MIBSPI1 Event Trigger Hookup

Table 5-12. MIBSPI1 Event Trigger Hookup

Event #	TGxCTRL TRIGSRC[3:0]	Trigger
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0]
EVENT1	0010	GIOA[1]
EVENT2	0011	GIOA[2]
EVENT3	0100	GIOA[3]
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	GIOA[6]
EVENT7	1000	GIOA[7]
EVENT8	1001	N2HET[8]
EVENT9	1010	N2HET[10]
EVENT10	1011	N2HET[12]
EVENT11	1100	N2HET[14]
EVENT12	1101	N2HET[16]
EVENT13	1110	N2HET[18]
EVENT14	1111	Intern Tick counter

NOTE

For N2HET trigger sources, the connection to the MibSPI1 module trigger input is made from the input side of the output buffer (at the N2HET module boundary). This way, a trigger condition can be generated even if the N2HET signal is not selected to be output on the pad.

NOTE

For GIOx trigger sources, the connection to the MibSPI1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin, or by driving the GIOx pin from an external trigger source.

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5.7.4 MibSPI/SPI Master Mode I/O Timing Specifications

Table 5-13. SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	Parameter			MIN	MAX	Unit
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		30	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4(5)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 5$		ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 5$		
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)} - 3$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)} - 3$		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		$0.5t_{f(SPC)} + 2$		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		$0.5t_{f(SPC)} + 2$		
7(5)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		5		ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		5		
8(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 5$	$(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	ns
			CSHOLD = 1	$C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 5$	$(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 5$	$(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	ns
			CSHOLD = 1	$C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 5$	$(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	
9(6)	$t_{T2CDELAY}$	Hold time SPICLK low CS until inactive (clock polarity = 0)		$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 5$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 8$	ns
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + tr(SPICS) - 5$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 8$	ns
10	t_{SPIENA}	SPIENAn Sample point		$(C2TDELAY+1) * t_{c(VCLK)} - t_{f(SPICS)} - 25$	$(C2TDELAY+1)*t_{c(VCLK)}$	ns
11	$t_{SPIENAW}$	SPIENAn Sample point from write to buffer			$(C2TDELAY+2)*t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see Table 3-4.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(VCLK)} \geq 30ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 30ns$.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

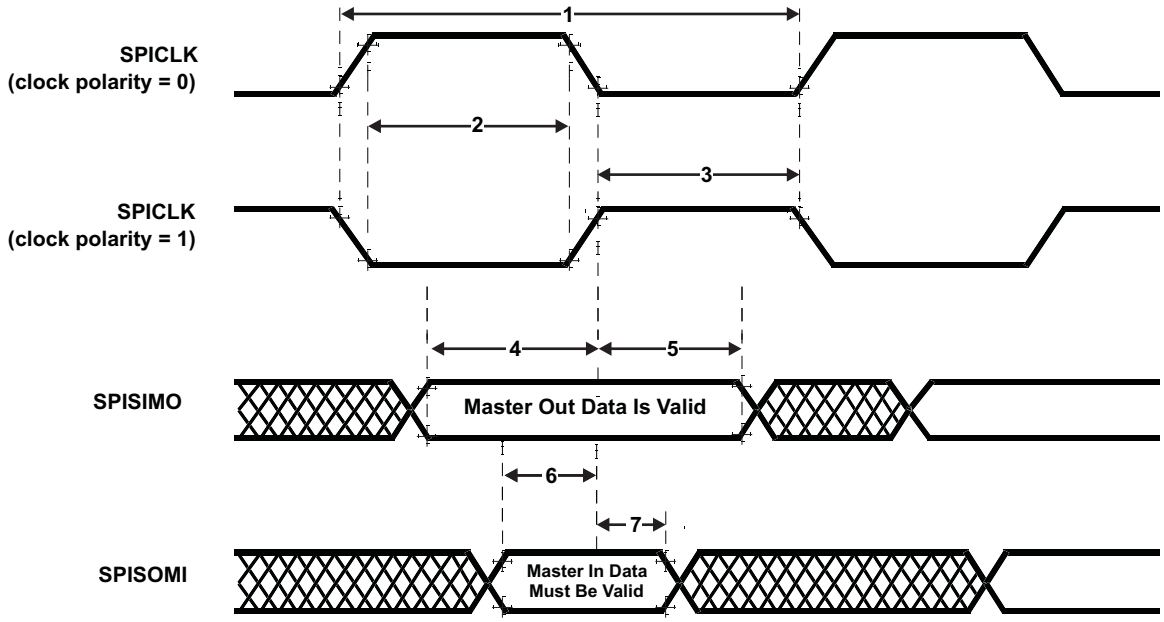

Figure 5-6. SPI Master Mode External Timing (CLOCK PHASE = 0)

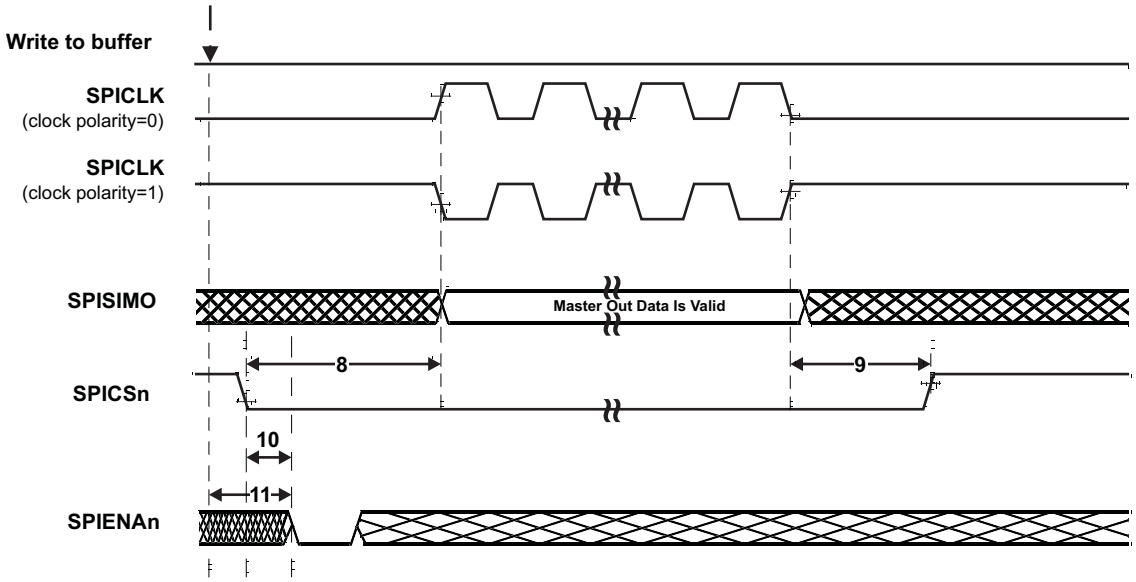

Figure 5-7. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

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Table 5-14. SPI Master Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	Parameter			MIN	MAX	Unit
1	$t_{c(SPC)M}$	Cycle time, SPICLK (4)		30	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4(5)	$t_{v(SIMO-SPCH)M}$	Valid time, SPICLK high after SPISIMO data valid (clock polarity = 0)		$0.5t_{c(SPC)M} - 2$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPICLK low after SPISIMO data valid (clock polarity = 1)		$0.5t_{c(SPC)M} - 2$		
5(5)	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)} - 3$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)} - 3$		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)		$t_{r(SPC)}$		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)		$t_{f(SPC)}$		
7(5)	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)		5		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)		5		
8(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 15$	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 5$	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 3$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 5$	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 3$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 5$	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 3$	
9(6)	$t_{T2CDELAY}$	Hold time SPICLK low CS until inactive (clock polarity = 0)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 5$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 8$	ns
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 5$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 8$	ns
10	t_{SPIENA}	SPIENAn Sample Point		$(C2TDELAY+1)* t_{c(VCLK)} - t_{f(SPICS)} - 25$	$(C2TDELAY+1)*t_{c(VCLK)}$	ns
11	$t_{SPIENAW}$	SPIENAn Sample point from write to buffer			$(C2TDELAY+2)*t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see the Table 3-4.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1)t_{c(VCLK)} \geq 30ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 30ns$.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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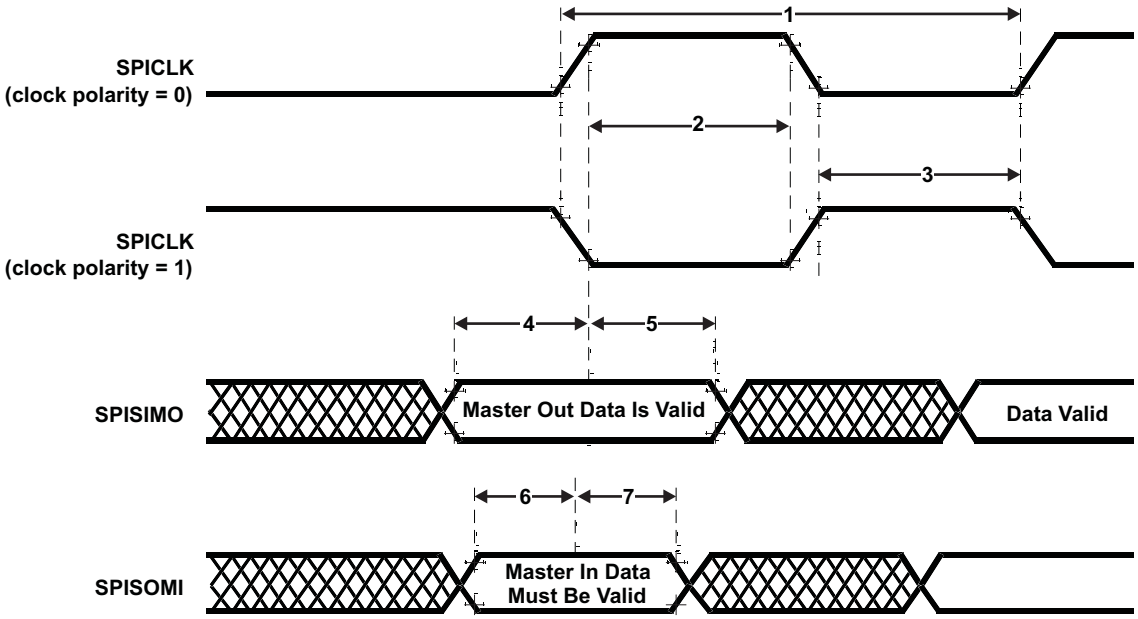

Figure 5-8. SPI Master Mode External Timing (CLOCK PHASE = 1)

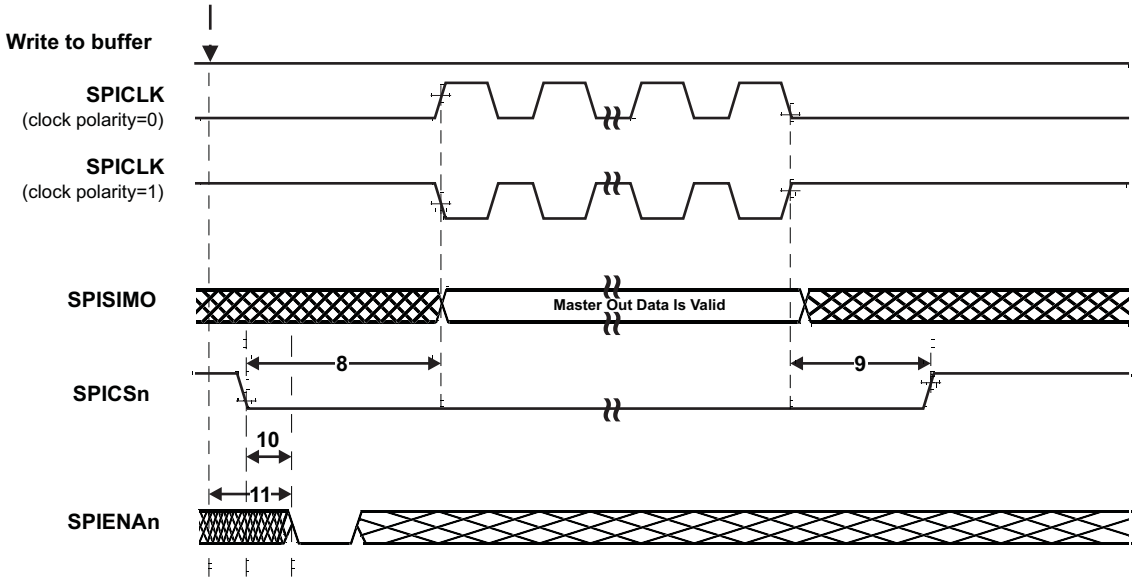

Figure 5-9. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

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5.7.5 SPI Slave Mode I/O Timings

Table 5-15. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

NO.	Parameter		MIN	MAX	Unit
1	$t_{c(SPC)S}$	Cycle time, SPICLK(5)	30	$256t_{c(VCLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	14		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	14		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	14		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	14		
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)		$t_{rf(SOMI)}$ + 10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)		$t_{rf(SOMI)}$ + 10	
5(6)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity =0)	2		ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity =1)	2		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	2		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	2		
7(6)	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	2		ns
	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after S PICLK high (clock polarity = 1)	2		
8	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$	ns
	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}+t_{f(ENAn)}+14$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(VCLK)}$, where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see Table 3-4.
(4) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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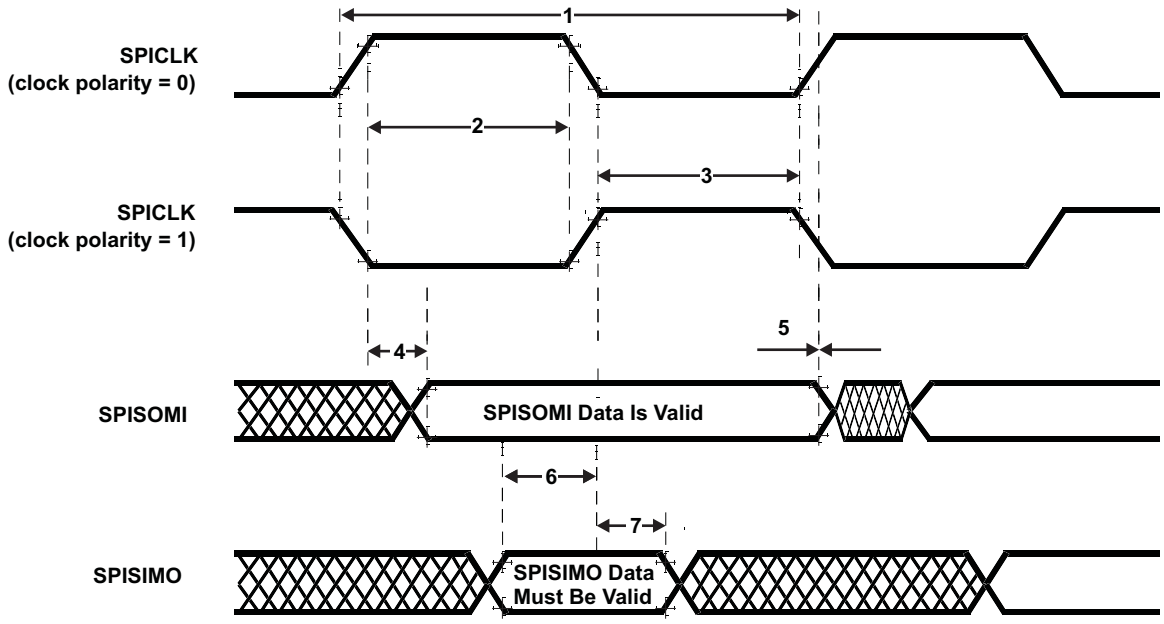

Figure 5-10. SPI Slave Mode External Timing (CLOCK PHASE = 0)

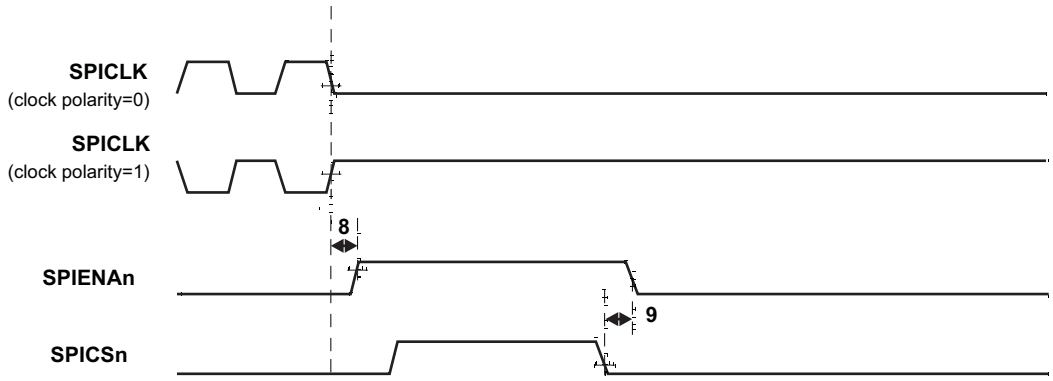

Figure 5-11. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)

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Table 5-16. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

NO.	Parameter		MIN	MAX	Unit
1	$t_{c(SPC)S}$	Cycle time, SPICLK(5)	30	$256t_{c(VCLK)}$	ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	14		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	14		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	14		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	14		
4(6)	$t_{d(SOMI-SPCL)S}$	Dealy time, SPISOMI data valid after SPICLK low (clock polarity = 0)		$t_{rf(SOMI)}$ + 10	ns
	$t_{d(SOMI-SPCH)S}$	Delay time, SPISOMI data valid after SPICLK high (clock polarity = 1)		$t_{rf(SOMI)}$ + 10	
5(6)	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity =0)	2		ns
	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity =1)	2		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	2		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	2		
7(6)	$t_{v(SPCH-SIMO)S}$	High time, SPISIMO data valid after SPICLK high (clock polarity = 0)	2		ns
	$t_{v(SPCL-SIMO)S}$	High time, SPISIMO data valid after SPICLK low (clock polarity = 1)	2		
8	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$	ns
	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}+t_{f(ENAn)}+14$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) If the SPI is in slave mode, the following must be true: tc(SPC)S ≤ (PS + 1) tc(VCLK), where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see Table 3-4.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /$f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(VCLK)} \geq 40ns$, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40ns$.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

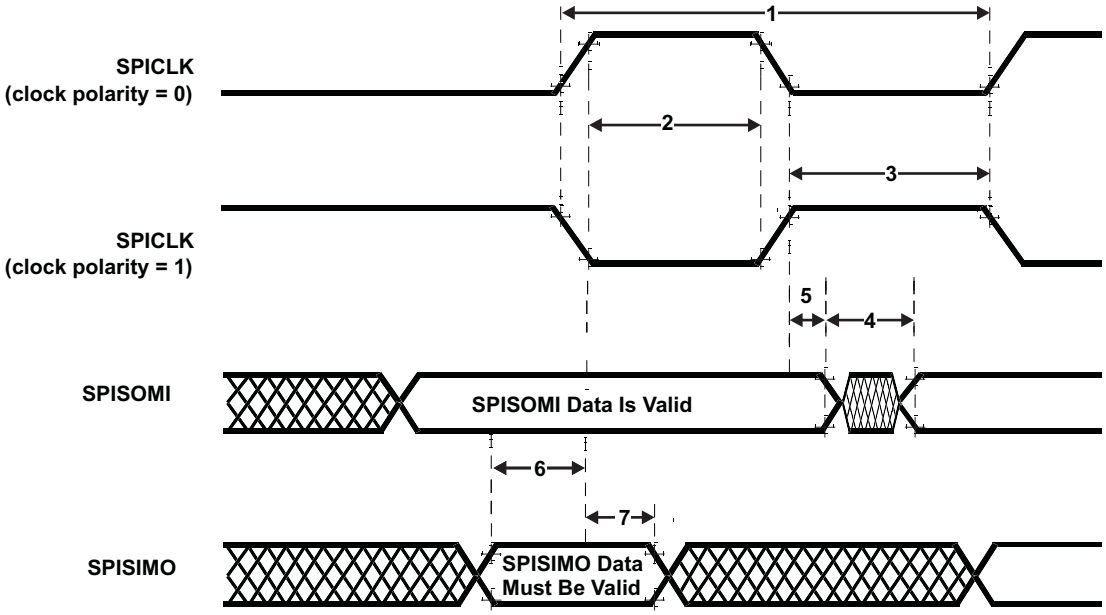

Figure 5-12. SPI Slave Mode External Timing (CLOCK PHASE = 1)

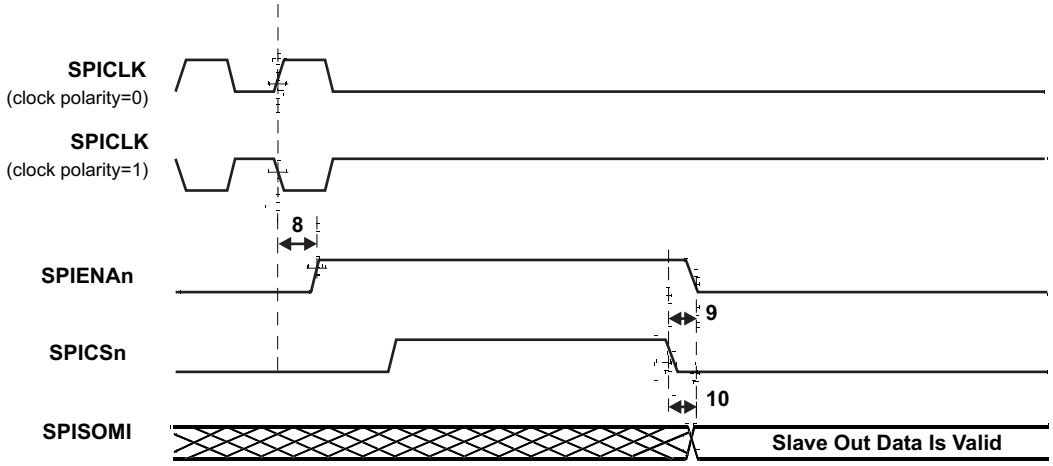

Figure 5-13. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)

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5.8 Enhanced Quadrature Encoder (eQEP)

Figure 5-14 shows the eQEP module interconnections on the device.

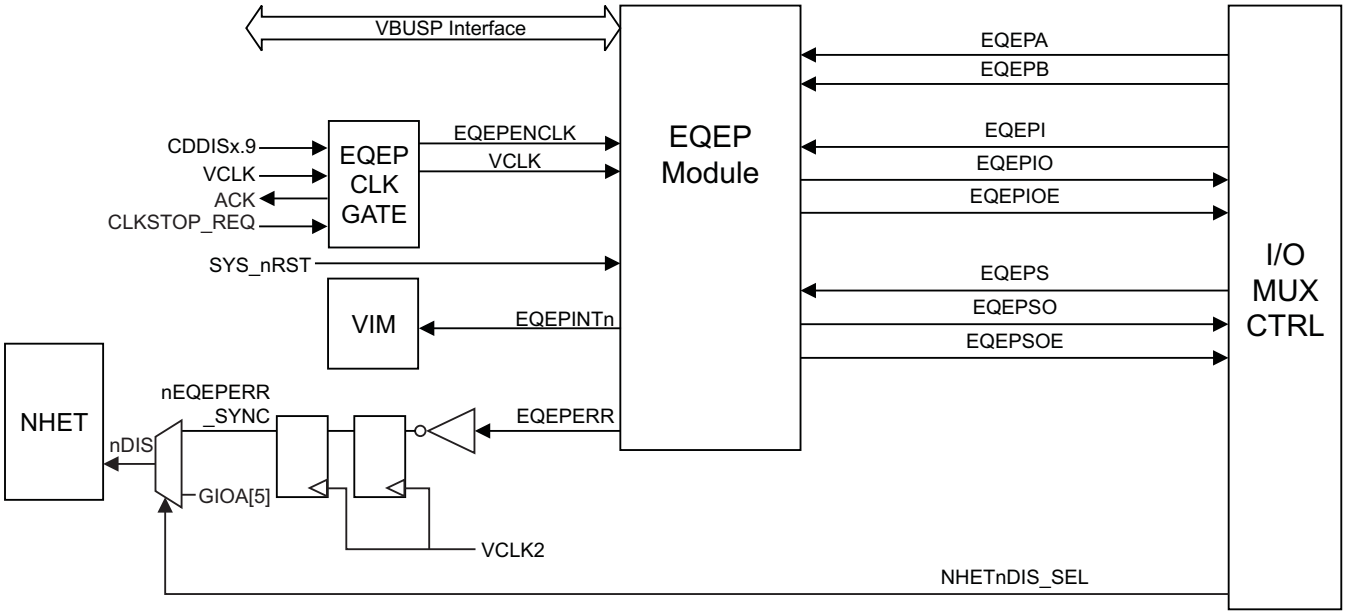

Figure 5-14. eQEP Module Interconnections

5.8.1 Clock Enable Control for eQEPx Modules

The device level control of the eQEP clock is accomplished through the enable/disable of the VCLK clock domain for eQEP only. This is realized using bit 9 of the CLKDDIS register. The eQEP clock source is enabled by default.

5.8.2 Using eQEPx Phase Error

The eQEP module sets the EQEPERR signal output whenever a phase error is detected in its inputs EQEPxA and EQEPxB. This error signal from both the eQEP modules is input to the connection selection multiplexor. As shown in Figure 5-14, the output of this selection multiplexor is inverted and connected to the N2HET module. This connection allows the application to define the response to a phase error indicated by the eQEP modules.

5.8.3 Input Connections to eQEPx Modules

The input connections to each of the eQEP modules can be selected between a double-VCLK-synchronized input or a double-VCLK-synchronized and filtered input, as shown in Table 5-17.

Table 5-17. Device-Level Input Synchronization

Input Signal	Control for Double-Synchronized Connection to eQEPx	Control for Double-Synchronized and Filtered Connection to eQEPx
eQEPA	PINMMR8[0] = 1	PINMMR8[0] = 0 and PINMMR8[1] = 1
eQEPB	PINMMR8[8] = 1	PINMMR8[8] = 0 and PINMMR8[9] = 1
eQEPI	PINMMR8[16] = 1	PINMMR8[16] = 0 and PINMMR8[17] = 1
eQEPS	PINMMR8[24] = 1	PINMMR8[24] = 0 and PINMMR8[25] = 1

5.8.4 Enhanced Quadrature Encoder Pulse (eQEPx) Timing

Table 5-18. eQEPx Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles
$t_{w(INDEXH)}$	QEP Index Input High Time	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles
$t_{w(INDEXL)}$	QEP Index Input Low Time	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles
$t_{w(STROBH)}$	QEP Strobe Input High Time	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low Time	Synchronous	2 $t_{c(VCLK)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK)}$ + filter width		cycles

Table 5-19. eQEPx Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		4 $t_{c(VCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		6 $t_{c(VCLK)}$	cycles

PRODUCT PREVIEW

6 Device and Documentation Support

6.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices.Each device has one of three prefixes: X, P, or null (no prefix) (for example, xRM46L852). These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices/tools.

Device development evolutionary flow:

x Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Fully-qualified production device.

x and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

The figure below illustrates the numbering and symbol nomenclature for the RM42L432 .

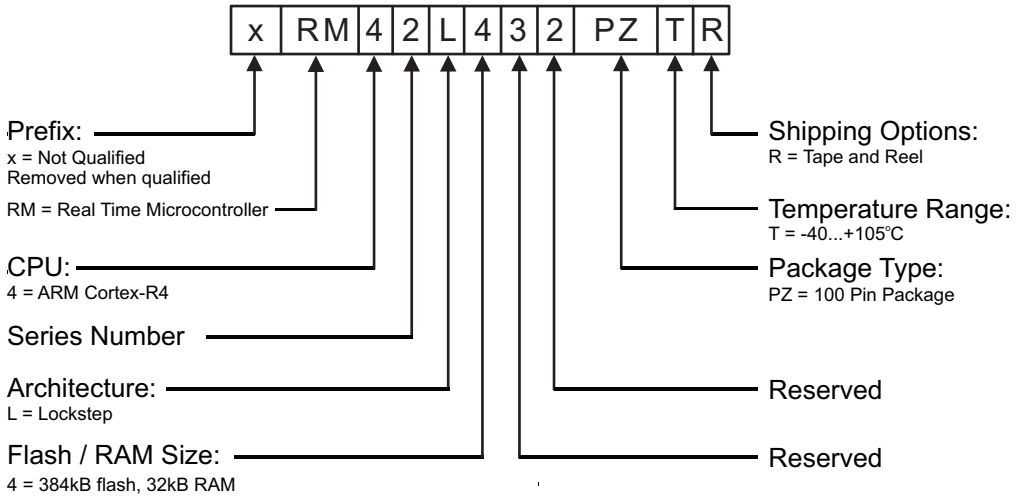

Figure 6-1. Device Numbering Conventions

6.2 Device Identification

6.2.1 Device Identification Code Register

The device identification code register identifies several aspects of the device including the silicon version. The details of the device identification code register are shown in Table 6-1. The device identification code register value for this device is:

- Rev 0 = 0x8048AD05

PRODUCT PREVIEW

Figure 6-2. Device ID Bit Allocation Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CP-15	UNIQUE ID														TECH
R-1	R-00000000100100														R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TECH			I/O VOLTAGE	PERIPH PARITY	FLASH ECC		RAM ECC	VERSION					1	0	1
R-101			R-0	R-1	R-10		R-1	R-00000					R-1	R-0	R-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

PRODUCT PREVIEW

Table 6-1. Device ID Bit Allocation Register Field Descriptions

Bit	Field	Value	Description
31	CP15		Indicates the presence of coprocessor 15
		1	CP15 present
30-17	UNIQUE ID	100100	Silicon version (revision) bits. This bitfield holds a unique number for a dedicated device configuration (die).
16-13	TECH		Process technology on which the device is manufactured.
		0101	F021
12	I/O VOLTAGE		I/O voltage of the device.
		0	I/O are 3.3v
11	PERIPHERAL PARITY		Peripheral Parity
		1	Parity on peripheral memories
10-9	FLASH ECC		Flash ECC
		10	Program memory with ECC
8	RAM ECC		Indicates if RAM memory ECC is present.
		1	ECC implemented
7-3	REVISION	0	Revision of the Device.
2-0	FAMILY ID	101	The platform family ID is always 0b101

6.2.2 Die Identification Registers

The four die ID registers at addresses 0xFFFFE1F0, 0xFFFFE1F4, 0xFFFFE1F8 and FFFFE1FC form a 128-bit dieid with the information as shown in Table Table 6-2.

Table 6-2. Die-ID Registers

Item	# of Bits	Bit Location
X Coord. on Wafer	8	7..0
Y Coord. on Wafer	8	15..8
Wafer #	6	21..16
Lot #	24	45..22
Reserved	82	127..46

PRODUCT PREVIEW

7 Mechanical Data

7.1 Thermal Data

Table 7-1 shows the thermal resistance characteristics for the PQFP - PZ mechanical packages.

Table 7-1. Thermal Resistance Characteristics (S-PQFP Package) [PZ]

PARAMETER	°C/W
$R_{\theta JA}$	48
$R_{\theta JC}$	5

7.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PRODUCT PREVIEW

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
XRM42L432PZT	ACTIVE	LQFP	PZ	100	1	TBD	Call TI	Call TI	

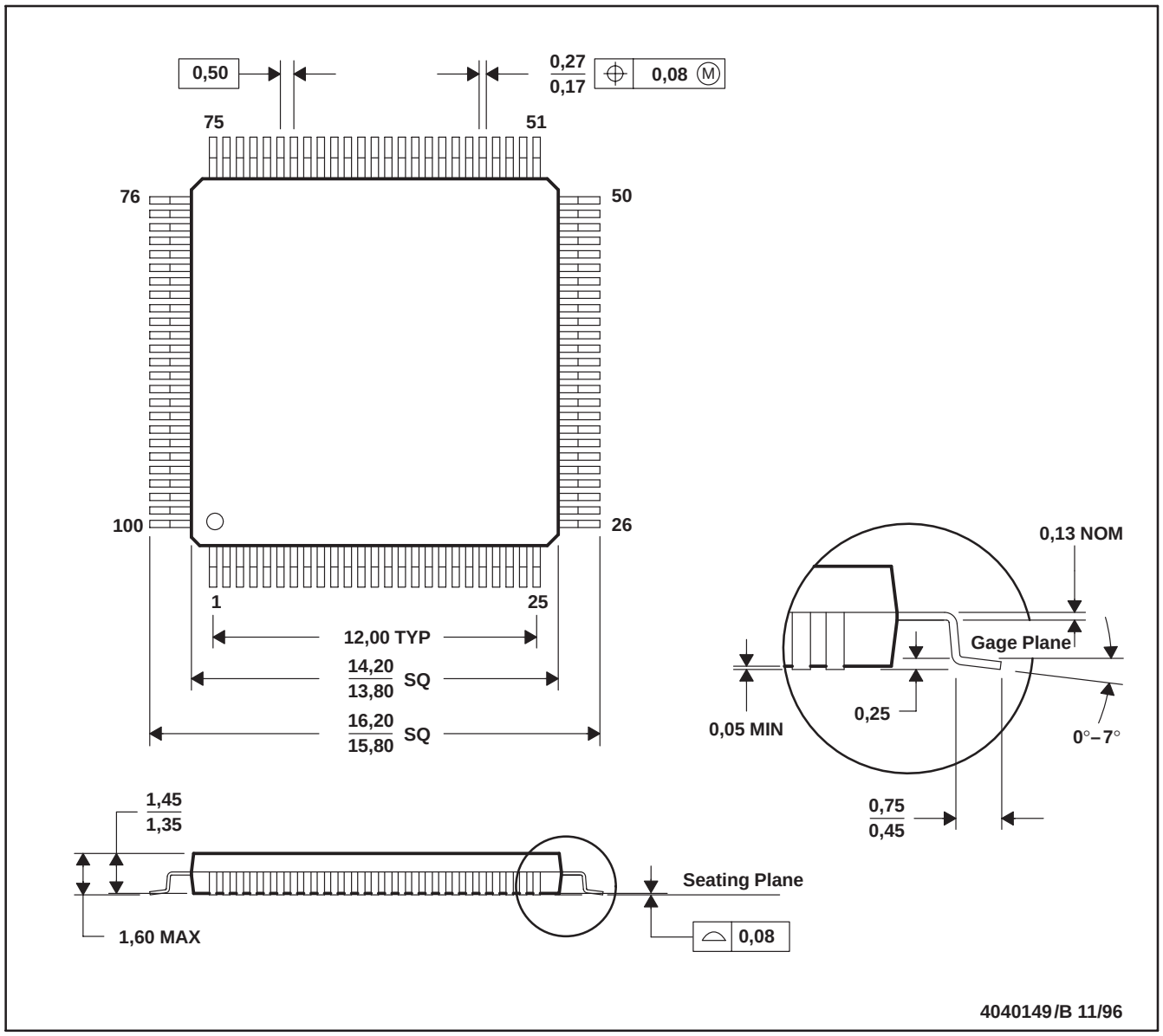
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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