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#### **FEATURES**

- Member of the Texas Instruments Widebus™
   Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 4.8 ns at 3.3 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V<sub>CC</sub>)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- All Outputs Have Equivalent 26- $\Omega$  Series Resistors, So No External Resistors Are Required
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

# DGG, DGV, OR DL PACKAGE (TOP VIEW)

		$\Gamma$		1
1DIR[	1	O	48	1 <u>0E</u>
1B1 [	2		47	] 1A1
1B2 [	3		46	] 1A2
GND[	4		45	GND
1B3 [	5		44	] 1A3
1B4 [	6		43	] 1A4
V <sub>CC</sub> [	7		42	] v <sub>cc</sub>
1B5 [	8		41	] 1A5
1B6 [	9		40	] 1A6
GND [	10		39	] GND
1B7 [	11		38	] 1A7
1B8 [	12		37	] 1A8
2B1 [	13		36	] 2A1
2B2 [	14		35	] 2A2
GND [	15		34	] GND
2B3 [	16		33	] 2A3
2B4 🛛	17		32	] 2A4
V <sub>CC</sub> [	18		31	] v <sub>cc</sub>
2B5 [	19		30	] 2A5
2B6 [	20		29	2A6
GND [	21		28	GND
2B7	22		27	2A7
2B8 [	23		26	] 2A8
2DIR [	24		25	] 2 <del>0E</del>
				J

#### **DESCRIPTION/ORDERING INFORMATION**

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCHR16245A is designed for asynchronous communication between data buses. The control-function implementation minimizes external-timing requirements.

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE	(1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	FBGA – GRD	Tape and reel	74LVCHR16245AGRDR	LR245A
	FBGA – ZRD (Pb-free)	rape and reer	74LVCHR16245AZRDR	LR243A
	SSOP – DL	Topo and roal	SN74LVCHR16245ALR	LVCHR16245A
	330P - DL	Tape and reel	74LVCHR16245ALRG4	LVCHR16245A
	TSSOP – DGG	Tape and reel	SN74LVCHR16245AGR	LVCHR16245A
–40°C to 85°C	1330F - DGG		74LVCHR16245AGRG4	LVCHK 10243A
-40 C to 65 C	TVSOP – DGV	T	SN74LVCHR16245AVR	LDR245A
	TVSOF - DGV	Tape and reel	74LVCHR16245AVRE4	LDR243A
	VFBGA – GQL	Topo and roal	SN74LVCHR16245AKR	LR245A
	VFBGA – ZQL (Pb-free)	Tape and reel	74LVCHR16245AZQLR	LKZ43A

 Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines areavailable at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SCAS582P-NOVEMBER 1996-REVISED DECEMBER 2005



### **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can disable the device so that the buses are effectively isolated.

All outputs, which are designed to sink up to 12 mA, include equivalent 26- $\Omega$  series resistors to reduce overshoot and undershoot.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by  $\overline{\sf OE}$  or DIR.

# GQL OR ZQL PACKAGE (TOP VIEW)

	1 2 3 4 5 6
Α	000000
В	000000
С	000000
D	000000
Ε	()()
F	()()
G	000000
н	000000
J	000000
K	000000

# TERMINAL ASSIGNMENTS<sup>(1)</sup> (56-Ball GQL/ZQL Package)

	(oo ban oddada i donago)										
	1	2	3	4	5	6					
Α	1DIR	NC	NC	NC	NC	1 <del>OE</del>					
В	1B2	1B1	GND	GND	1A1	1A2					
С	1B4	1B3	V <sub>CC</sub>	V <sub>CC</sub>	1A3	1A4					
D	1B6	1B5	GND	GND	1A5	1A6					
Е	1B8	1B7			1A7	1A8					
F	2B1	2B2			2A2	2A1					
	G2B3	2B4	GND	GND	2A4	2A3					
Н	2B5	2B6	V <sub>CC</sub>	V <sub>CC</sub>	2A6	2A5					
J	2B7	2B8	GND	GND	2A8	2A7					
K	2DIR	NC	NC	NC	NC	2 <del>OE</del>					

(1) NC - No internal connection

#### GRD OR ZRD PACKAGE (TOP VIEW)

	_	1	2	3	4	5	6	
Α	$\left( \right.$		$\bigcirc$					_
В		()	()	$\bigcirc$	$\bigcirc$	$\bigcirc$	()	
С		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	()	
D		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
E		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
F		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
G		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
н		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
J		$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	$\bigcirc$	
	\							_

# TERMINAL ASSIGNMENTS<sup>(1)</sup> (54-Ball GRD/ZRD Package)

	1	2	3	4	5	6
Α	1B1	NC	1DIR	1 <del>OE</del>	NC	1A1
В	1B3	1B2	NC	NC	1A2	1A3
С	1B5	1B4	V <sub>CC</sub>	V <sub>CC</sub>	1A4	1A5
D	1B7	1B6	GND	GND	1A6	1A7
E	2B1	1B8	GND	GND	1A8	2A1
F	2B3	2B2	GND	GND	2A2	2A3
G	2B5	2B4	V <sub>CC</sub>	V <sub>CC</sub>	2A4	2A5
Н	2B7	2B6 NC	NC	NC	2A6	2A7
J	2B8	NC	2DIR	2 <del>OE</del>	NC	2A8

(1) NC - No internal connection

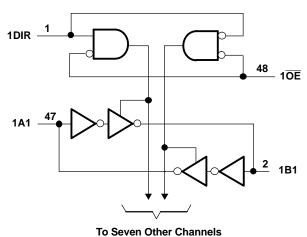


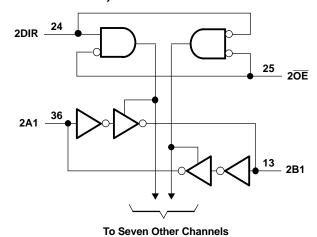
# FUNCTION TABLE<sup>(1)</sup> (EACH 8-BIT SECTION)

CONTRO	L INPUTS	OUTPUT C	IRCUITS	OPERATION
ŌĒ	DIR	A PORT	B PORT	OPERATION
L	L	Enabled	Hi-Z	B data to A bus
L	Н	Hi-Z	Enabled	A data to B bus
Н	Χ	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

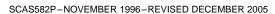
#### **LOGIC DIAGRAM (POSITIVE LOGIC)**





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### SN74LVCHR16245A 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS





### **Absolute Maximum Ratings**(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range		-0.5	6.5	V	
VI	Input voltage range <sup>(2)</sup>	Input voltage range <sup>(2)</sup>			V	
Vo	Voltage range applied to any output in the h	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>			V	
Vo	Voltage range applied to any output in the h	-0.5	V <sub>CC</sub> + 0.5	V		
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA	
Io	Continuous output current	Continuous output current		±50	mA	
	Continuous current through each V <sub>CC</sub> or GN	ND		±100	mA	
		DGG package		70		
		DGV package		58		
$\theta_{JA}$	Package thermal impedance (4)	DL package		63 42		
		GQL/ZQL package				
		GRD/ZRD package		36		
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT	
V	Cumply yeltogo	Operating	1.65	3.6	٧	
V <sub>CC</sub>	Supply voltage	Data retention only	1.5		V	
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>			
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V	
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		
VI	Input voltage		0	5.5	V	
\/	Output walks as	High or low state	0	$V_{CC}$	V	
Vo	Output voltage	3-state	0	5.5	V	
		V <sub>CC</sub> = 1.65 V		-2		
	High level extent expect	V <sub>CC</sub> = 2.3 V		-4	A	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V		-8	_8 mA	
		V <sub>CC</sub> = 3 V				
		V <sub>CC</sub> = 1.65 V		2		
	Lave lavel autout average	V <sub>CC</sub> = 2.3 V		4	A	
l <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		8	mA	
		V <sub>CC</sub> = 3 V		12		
Δt/Δν	Input transition rise or fall rate			10	ns/V	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

<sup>(1)</sup> All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

<sup>(2)</sup> The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



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#### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		V <sub>cc</sub>	MIN	TYP <sup>(1)</sup> MAX	UNIT	
		$I_{OH} = -100 \mu A$		1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			
		$I_{OH} = -2 \text{ mA}$		1.65 V	1.2			
		1	2.3 V	1.7		V		
$V_{OH}$		$I_{OH} = -4 \text{ mA}$	2.7 V	2.2				
		$I_{OH} = -6 \text{ mA}$		3 V	2.4			
		$I_{OH} = -8 \text{ mA}$	2.7 V	2				
		I <sub>OH</sub> = -12 mA		3 V	2			
		I <sub>OL</sub> = 100 μA		1.65 V to 3.6 V		0.2		
		I <sub>OL</sub> = 2 mA	1.65 V		0.45			
		1 - 4 m A		2.3 V		0.7		
$V_{OL}$		I <sub>OL</sub> = 4 mA	2.7 V		0.4	V		
		I <sub>OL</sub> = 6 mA	3 V		0.55			
		I <sub>OL</sub> = 8 mA	2.7 V		0.6			
		I <sub>OL</sub> = 12 mA	3 V		0.8			
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V		3.6 V		±5	μΑ	
		V <sub>I</sub> = 0.58 V	1 CF V	(2)		μΑ		
		V <sub>I</sub> = 1.07 V	1.65 V	(2)				
		V <sub>I</sub> = 0.7 V	0.01/	45				
I <sub>I(hold)</sub>	A or B port	V <sub>I</sub> = 1.7 V	2.3 V	-45				
		V <sub>I</sub> = 0.8 V		2.1/	75			
		V <sub>I</sub> = 2 V		3 V	-75			
		V <sub>I</sub> = 0 to 3.6 V <sup>(3)</sup>		3.6 V		±500		
I <sub>off</sub>	·	$V_I$ or $V_O = 5.5 \text{ V}$		0		±10	μΑ	
I <sub>OZ</sub> <sup>(4)</sup>		$V_O = 0 \text{ V or } (V_{CC} \text{ to } 5.5 \text{ V})$		2.3 V to 3.6 V		±5	μΑ	
1		V <sub>I</sub> = V <sub>CC</sub> or GND	1 - 0	3.6 V		20		
I <sub>CC</sub>		$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(5)}$	$I_0 = 0$	3.6 V		20	μΑ	
$\Delta I_{CC}$		One input at V <sub>CC</sub> – 0.6 V, Other inputs	at V <sub>CC</sub> or GND	2.7 V to 3.6 V		500	μΑ	
Ci	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		3	pF	
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V		12	pF	

<sup>(1)</sup> All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.
(2) This information was not available at the time of publication.

This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

For the total leakage current in an I/O port, please consult the  $I_{I(hold)}$  specification for the input voltage condition 0 V <  $V_I$  <  $V_{CC}$ , and the  $I_{OZ}$  specification for the input voltage conditions  $V_I$  = 0 V or  $V_I$  =  $V_{CC}$  to 5.5 V. The bus-hold current, at input voltages greater than  $V_{CC}$ , is negligible.

This applies in the disabled state only.

### SN74LVCHR16245A 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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### **Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> = 1 ± 0.2		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> = 3 ± 0.3	3.3 V 3 V	UNIT
	(INPUT) (OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>pd</sub>	A or B	B or A	1	12.5	1	9.5	1	5.7	1.5	4.8	ns
t <sub>en</sub>	ŌĒ	A or B	1	15.8	1	12.2	1	7.9	1.5	6.3	ns
t <sub>dis</sub>	ŌĒ	A or B	1	19.2	1	11.9	1	8.3	2.2	7.4	ns

### **Operating Characteristics**

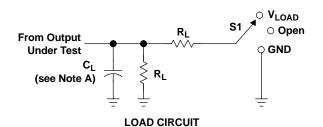
 $T_A = 25^{\circ}C$ 

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	UNIT
_	Power dissipation capacitance	Outputs enabled	f = 10 MHz	(1)	(1)	39	ρF
C <sub>pd</sub>	per transceiver	Outputs disabled	I = IU WIMZ	(1)	(1)	4	μΓ

(1) This information was not available at the time of publication.



#### PARAMETER MEASUREMENT INFORMATION



2.7 V

2.7 V

≤2.5 ns

≤2.5 ns

V<sub>CC</sub>

2.7 V

3.3 V  $\pm$  0.3 V

TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

500  $\Omega$ 

**500** Ω

0.3 V

0.3 V

LOW- AND HIGH-LEVEL ENABLING

**INPUT**  $V_{M}$ **V<sub>LOAD</sub>**  $C_L$  $R_L$  $V_{\Delta}$ ٧ı t<sub>r</sub>/t<sub>f</sub> 1.8 V  $\pm$  0.15 V ≤2 ns 30 pF 0.15 V Vcc V<sub>CC</sub>/2 Vcc 1  $k\Omega$  $\nu_{\text{CC}}$ Vcc **500** Ω  $\textbf{2.5 V} \pm \textbf{0.2 V}$ ≤2 ns V<sub>CC</sub>/2 30 pF 0.15 V

6 V

6 V

50 pF

50 pF

1.5 V

1.5 V

 $V_{I}$ **Timing Input** 0 V  $V_{I}$ Input ٧M  $V_{M}$ **Data Input** 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION SETUP AND HOLD TIMES**  $V_{I}$ ٧ı Output  $V_{M}$ ٧M Input Control 0 V **t**PHL t<sub>PLZ</sub> t<sub>PLH</sub>  $t_{PZL}$ Output V<sub>LOAD</sub>/2  $V_{OH}$ Waveform 1 S1 at V<sub>LOAD</sub> Output  $V_{OL} + V_{C}$  $V_{OL}$ (see Note B) - t<sub>PHZ</sub> t<sub>PHL</sub> **t**PLH t<sub>PZH</sub> Output  $V_{\mathsf{OH}}$  $V_{OH}$ Waveform 2  $V_{OH} - V_{\Delta}$ S1 at GND Output ≈0 V (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES ENABLE AND DISABLE TIMES** 

NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.

**INVERTING AND NONINVERTING OUTPUTS** 

- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

3-Dec-2012

#### **PACKAGING INFORMATION**

Orderable Device		Package Type	_	Pins	Package Qty	Eco Plan	Lead/Ball Finish		Samples
74LVCHR16245AGRDR	OBSOLETE	BGA	<b>Drawing</b> GRD	54		(2) TBD	Call TI	Call TI	(Requires Login)
		MICROSTAR JUNIOR							
74LVCHR16245AGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVCHR16245ALRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVCHR16245AVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVCHR16245AVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74LVCHR16245AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
74LVCHR16245AZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
SN74LVCHR16245AGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVCHR16245AKR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	
SN74LVCHR16245ALR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVCHR16245AVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.





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TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVCHR16245AZQLR	BGA MI CROSTA R JUNI OR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
74LVCHR16245AZRDR	BGA MI CROSTA R JUNI OR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1
SN74LVCHR16245AGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVCHR16245ALR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVCHR16245AVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

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\*All dimensions are nominal

All difficusions are norminal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVCHR16245AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
74LVCHR16245AZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	333.2	345.9	28.6
SN74LVCHR16245AGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVCHR16245ALR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74LVCHR16245AVR	TVSOP	DGV	48	2000	367.0	367.0	38.0

### ZQL (R-PBGA-N56)

#### PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

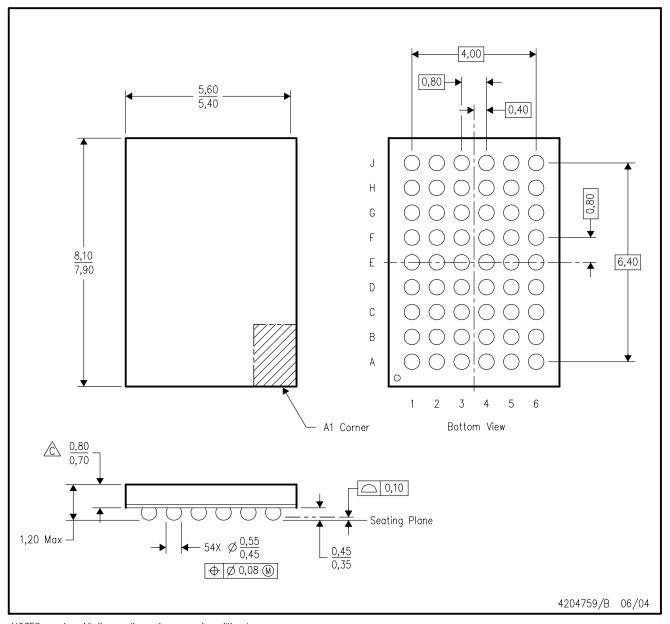
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

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## GRD (R-PBGA-N54)

### PLASTIC BALL GRID ARRAY



 $\hbox{NOTES:} \quad \hbox{A. All linear dimensions are in millimeters.}$ 

B. This drawing is subject to change without notice.

Falls within JEDEC MO-205 variation DD.

D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.



## ZRD (R-PBGA-N54)

### PLASTIC BALL GRID ARRAY



 $\hbox{NOTES:} \quad \hbox{A. All linear dimensions are in millimeters.}$ 

- B. This drawing is subject to change without notice.
- Falls within JEDEC MO-205 variation DD.
- D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).



#### DGV (R-PDSO-G\*\*)

#### **24 PINS SHOWN**

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

## GQL (R-PBGA-N56)

### PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



#### DL (R-PDSO-G\*\*)

#### **48 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

#### DGG (R-PDSO-G\*\*)

#### PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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